

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

"LOHWILL" MLB SCHEMATIC

LAST_MODIFICATION = 2016-10-23 12:22:45 PROTO1A : PRELIMINARY TEST


| REV | ECN | DESCRIPTION OF REVISION | CK APPD | DATE |
|-----|------------|-------------------------|---------|------------|
| 9 | 0006941568 | ENGINEERING RELEASED | | 2016-10-23 |

| PAGE | CSA | CONTENTS | SYNC | DATE |
|------|-----|-------------------------------|----------------|------------|
| 1 | 1 | Table of Contents | | |
| 2 | 2 | BOM Configuration | SHART_J44 | 11/27/2012 |
| 3 | 3 | BOM Configuration | J79_JACK | 04/07/2016 |
| 4 | 4 | PD Parts | LDUNN_J44 | 01/13/2013 |
| 5 | 5 | CPU GFX | J130_DEV_MLB_U | 04/29/2015 |
| 6 | 6 | CPU MISC/JTAG/CFG/RSVD | J130_DEV_MLB_U | 04/28/2015 |
| 7 | 7 | CPU LPDDR3 Interface | J52_MLB | 05/12/2015 |
| 8 | 8 | CPU & PCH Power | J79_JSHAO | 03/14/2016 |
| 9 | 9 | CPU & PCH Grounds | J79_ALFRED | 05/12/2015 |
| 10 | 10 | CPU Core Decoupling | J79_JSHAO | 08/28/2015 |
| 11 | 11 | CPU GT Decoupling | J79_JSHAO | 08/28/2015 |
| 12 | 12 | PCH Decoupling | J79_JSHAO | 03/14/2016 |
| 13 | 13 | PCH Audio/LPC/SPI/SMBus | J130_MLB | 02/22/2016 |
| 14 | 14 | PCH Power Management | J130_MLB | 05/04/2016 |
| 15 | 15 | PCH PCIE/USB/CLKS | J130_MLB | 06/23/2015 |
| 16 | 16 | PCH SPI/UART/GPIO | J130_MLB | 12/08/2015 |
| 17 | 18 | CPU/PCH Merged XDP | J130_MLB | 12/08/2015 |
| 18 | 19 | Chipset Support 1 | J79_GREG | 09/09/2015 |
| 19 | 20 | Chipset Support 2 | J79_GREG | 07/05/2016 |
| 20 | 22 | LPDDR3 VREF Margining | J52_MLB | 05/12/2015 |
| 21 | 23 | LPDDR3 DRAM Channel A (00-31) | J52_MLB | 05/12/2015 |
| 22 | 24 | LPDDR3 DRAM Channel A (32-63) | J52_MLB | 05/12/2015 |
| 23 | 25 | LPDDR3 DRAM Channel B (00-31) | J52_MLB | 05/12/2015 |
| 24 | 26 | LPDDR3 DRAM Channel B (32-63) | J52_MLB | 05/12/2015 |
| 25 | 27 | LPDDR3 DRAM Termination | J52_MLB | 05/12/2015 |
| 26 | 28 | USB-C HIGH SPEED 1 | J79_GREG | 07/27/2015 |
| 27 | 29 | USB-C HIGH SPEED 2 | J79_GREG | 09/09/2015 |
| 28 | 30 | USB-C Support | J79_GREG | 08/08/2016 |
| 29 | 31 | USB-C PORT CONTROLLER A | J79_GREG | 08/08/2016 |
| 30 | 32 | USB-C PORT CONTROLLER B | J79_GREG | 02/28/2016 |
| 31 | 33 | USB-C CONNECTOR A | J79_GREG | 07/05/2016 |
| 32 | 34 | USB-C CONNECTOR B | J79_GREG | 03/24/2016 |
| 33 | 35 | TBT 5V REGULATOR | J79_JSHAO | 12/18/2015 |
| 34 | 36 | Display Mux | J79_GREG | 02/28/2016 |
| 35 | 37 | WIFI/BT: MODULE 1 | J79_METE | 05/17/2016 |
| 36 | 38 | WIFI/BT: MODULE 2 | J79_METE | 03/02/2016 |
| 37 | 39 | Camera/DFR 1 | J80_MLB_BAFFIN | 07/22/2016 |
| 38 | 40 | Camera/DFR 2 | J79_ANDREW | 03/22/2016 |
| 39 | 41 | Camera/DFR 3 | J79_ANDREW | 04/25/2016 |
| 40 | 42 | Berkelium - 1 | J79_ANDREW | 03/14/2016 |
| 41 | 43 | Berkelium - 2 | J79_ANDREW | 02/01/2016 |
| 42 | 44 | T208 Support | J79_ANDREW | 07/01/2016 |
| 43 | 45 | Connectors&ESD | J79_GAREN | 11/21/2015 |
| 44 | 46 | Empty | J79_DAYU | 05/26/2015 |
| 45 | 47 | Empty | J79_DAYU | 05/26/2015 |
| 46 | 48 | Empty | J79_DAYU | 05/12/2015 |
| 47 | 49 | MESA | J79_ANDREW | 01/06/2016 |
| 48 | 50 | SMC | J79_JACK | 04/11/2016 |
| 49 | 51 | SMC Shared Support | J79_JACK | 04/14/2016 |
| 50 | 52 | SMC Project Support | J79_JACK | 04/11/2016 |
| 51 | 53 | SMBus Connections | J79_JACK | 03/31/2016 |
| 52 | 54 | Power Sensors: High Side | J79_JACK | 12/07/2015 |
| 53 | 55 | Power Sensors: Load Side | J79_JACK | 04/03/2016 |
| 54 | 56 | Power Sensors: Extended | J79_JACK | 01/08/2016 |
| 55 | 57 | Power Sensors: Extended 2 | J79_JACK | 05/10/2016 |
| 56 | 58 | Thermal Sensors | J79_JACK | 09/24/2015 |
| 57 | 59 | Power Sensors:Extended 3 | J79_JACK | 04/14/2016 |
| 58 | 60 | Fans | J79_JACK | 08/21/2015 |
| 59 | 61 | SPI Debug Connector | J52_MLB | 05/12/2015 |
| 60 | 62 | HDA Bridge | J79_JCURCIO | 03/24/2016 |

| PAGE | CSA | CONTENTS | SYNC | DATE |
|------|-----|--------------------------------|-------------------------|------------|
| 61 | 63 | AUDIO JACK CODEC | J79_JCURCIO | 05/13/2016 |
| 62 | 64 | Left Speaker Amps & Conn | J79_JCURCIO | 11/18/2015 |
| 63 | 65 | Right Speaker Amps & Conn | J79_JCURCIO | 12/03/2015 |
| 64 | 66 | AUDIO JACK CONNECTOR | J79_JCURCIO | 12/18/2015 |
| 65 | 69 | DC-In & Battery Connectors | J79_JSHAO | 12/03/2015 |
| 66 | 70 | PBUS Supply & Battery Charger | J79_JSHAO | 12/03/2015 |
| 67 | 71 | CORE & SA IMVP IC | J79_JSHAO | 03/02/2016 |
| 68 | 72 | CORE & SA IMVP POWER BLOCK | J79_JSHAO | 12/03/2015 |
| 69 | 73 | Empty | J79_SILUCHEN | 04/02/2015 |
| 70 | 74 | GT & GTX IMVP POWER BLOCK | J79_JSHAO | 09/25/2015 |
| 71 | 75 | Empty | J79_SILUCHEN | 03/27/2015 |
| 72 | 76 | Power - 5V 3.3V Supply | J79_JSHAO | 03/23/2016 |
| 73 | 77 | Power - EPIO EDRAM Supply | J79_JSHAO | 04/12/2016 |
| 74 | 78 | PMIC-1 & Power Control | J79_JSHAO | 09/09/2015 |
| 75 | 79 | PMIC-1 1.2V 0.6V VCCIO | J79_JSHAO | 12/03/2015 |
| 76 | 80 | PMIC-1 1V 1.8V VCCPH | J79_JSHAO | 12/03/2015 |
| 77 | 81 | PMIC-1 Aliases & TPs | J79_SILUCHEN | 07/17/2015 |
| 78 | 82 | Power FETs | J79_JSHAO | 03/14/2016 |
| 79 | 84 | LCD Backlight Driver | J79_RUENJOU | 09/09/2015 |
| 80 | 85 | eDP Display Connector | J79_RUENJOU | 09/12/2015 |
| 81 | 86 | S3X CORE PCIE | J79_RUENJOU | 08/20/2015 |
| 82 | 87 | S3X POWER | J79_RIO | 06/18/2015 |
| 83 | 88 | S3X GND | J79_RIO | 06/18/2015 |
| 84 | 89 | Connector | J79_RUENJOU | 09/09/2015 |
| 85 | 90 | NAND VR, I2C ROM, TEMP SENSORS | J79_RUENJOU | 09/12/2015 |
| 86 | 91 | ANI[3:0] | J79_RUENJOU | 09/25/2015 |
| 87 | 92 | ANI[7:4] | J79_RUENJOU | 09/25/2015 |
| 88 | 93 | PICCOLO PMIC | J79_RUENJOU | 09/24/2015 |
| 89 | 94 | SSD NAND VR | J79_JSHAO | 12/18/2015 |
| 90 | 95 | Empty | J14 | 10/23/2012 |
| 91 | 96 | LIFEBOAT | J79_RUENJOU | 09/09/2015 |
| 92 | 110 | USB-C HIGH SPEED 1 | J79_GREG | 07/28/2015 |
| 93 | 111 | USB-C HIGH SPEED 2 | J79_GREG | 08/28/2015 |
| 94 | 112 | USB-C Support | J79_GREG | 07/05/2016 |
| 95 | 113 | USB-C PORT CONTROLLER A | J79_GREG | 02/28/2016 |
| 96 | 114 | USB-C PORT CONTROLLER B | J79_GREG | 02/28/2016 |
| 97 | 115 | USB-C CONNECTOR A | J79_GREG | 07/05/2016 |
| 98 | 116 | USB-C CONNECTOR B | J79_GREG | 03/24/2016 |
| 99 | 117 | TBT 5V REGULATOR | J79_JSHAO | 12/18/2015 |
| 100 | 120 | Power Aliases - 1 | J79_ALFRED | 06/17/2015 |
| 101 | 121 | Power Aliases - 2 | J79_ALFRED | 06/18/2015 |
| 102 | 122 | Signal Aliases | SHART_J44 | 11/19/2012 |
| 103 | 123 | LPDDR3 Bit & Byte Swizzle | AHARTMAN_J52 | 10/29/2013 |
| 104 | 124 | ICT FCT 1 | YHARTANTO_J44 | 12/18/2012 |
| 105 | 125 | ICT FCT 2 | YHARTANTO_J44 | 12/18/2012 |
| 106 | 127 | Desense Capacitors | YHARTANTO_J44 | 01/09/2013 |
| 107 | 129 | Empty | J79_RIO | 06/18/2015 |
| 108 | 130 | PCB Rule Definitions | YHARTANTO_J44 | 12/14/2012 |
| 109 | 131 | CPU Constraints | YHARTANTO_J44 | 01/13/2013 |
| 110 | 132 | PCH Constraints | YHARTANTO_J44 | 01/08/2013 |
| 111 | 133 | Memory Constraints | YHARTANTO_J44 | 01/02/2013 |
| 112 | 134 | TBT DP HDMI Constraints | J79_JACK | 05/19/2015 |
| 113 | 135 | PCIE Constraints | J79_JACK | 05/19/2015 |
| 114 | 136 | USB Constraints | J79_JACK | 05/21/2015 |
| 115 | 137 | SMC Constraints | YHARTANTO_J44 | 01/02/2013 |
| 116 | 138 | Camera Constraints | YHARTANTO_J44 | 01/09/2013 |
| 117 | 139 | Sensors & Audio Constraints | YHARTANTO_J44 | 01/04/2013 |
| 118 | 140 | References | J79_RUENJOU_CONSTRAINTS | 06/11/2015 |
| 119 | 145 | Alternates BOM Table | J80_MLB | 12/12/2015 |

Schematic / PCB #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------|---------------|----------|------------|
| 051-00777 | 1 | SCHEM,MLB,Lohwill | SCH | CRITICAL | |
| 820-00923 | 1 | PCBF,MLB,Lohwill | PCB | CRITICAL | xTN20JE19 |

| | | | |
|---|-----------------|-------------------|------|
| DRAWING TITLE | | SCHEM,MLB,Lohwill | |
|  Apple Inc. | GRANTING NUMBER | 051-00777 | STEP |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1. TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 1.1 NOT TO REPRODUCE OR COPY IT 1.11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1.111 ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 1 OF 145 | |
| | SHEET | 1 OF 119 | |

BOM Groups

Table with BOM GROUP and BOM OPTIONS columns. Rows include Lohwill_COMMON, Lohwill_COMMON1, Lohwill_COMMON2, Lohwill_COMMON3, Lohwill_PROGPARTS, Lohwill_DEVEL:ENG, Lohwill_DEVEL:DVT, and Lohwill_DEVEL:PVT.

Module Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists various components like CPU, memory, and storage.

Programmables (All Builds)

Table listing EFI ROM, SMC ROM, TBT ROMs, and WIFI/BT ROM with columns for part number, quantity, description, reference, criticality, and option.

Variable BOM Groups Development/Base BOMs

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Shows development and base BOM configurations.

Main DRAM Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists DRAM components like Micron and Samsung.

Main DRAM SPD Straps

Table with columns: BOM GROUP and BOM OPTIONS. Lists SPD strap configurations for different DRAM types.

NAND Parts

Table with columns: PART NUMBER, QTY, DESCRIPTION, REFERENCE DES, CRITICAL, BOM OPTION. Lists NAND flash components.

NAND Straps

Table with columns: BOM GROUP and BOM OPTIONS. Lists NAND strap configurations for different capacities and types.

Strategic Silicon

Table with columns: PART#, STRATEGIC VALUE, COMMENT. Lists strategic silicon components and their values.

Table with columns: PART#, STRATEGIC VALUE, COMMENT. Lists strategic silicon components and their values.

CPU DRAM CFG Chart

Chart showing configurations for DIE REV, SPEED, and CAPACITY across different CFG options.

Table with columns: VENDOR, CFG 1, CFG 0. Lists vendors like HYNIX, MICRON, SAMSUNG, and N/A.

BOM Configuration header with Apple logo, drawing number (051-00777), revision (9.0.0), and page information (2 OF 145).

NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED

BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|---------------------------------|--|
| 685-00055 | COMMON PARTS,MLB,X362 | X362_COMMON |
| 985-00070 | DEV,MLB,X362 | X362_DEVEL:DVT |
| 639-01870 | MLB,2.9G,SAM-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_256G |
| 639-01871 | MLB,2.9G,SAM-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_256G |
| 639-01872 | MLB,2.9G,MIC-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_256G |
| 639-01873 | MLB,2.9G,MIC-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_256G |
| 639-01984 | MLB,2.9G,SAM-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_512G |
| 639-01985 | MLB,2.9G,SAM-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_512G |
| 639-01986 | MLB,2.9G,MIC-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_512G |
| 639-01987 | MLB,2.9G,MIC-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_512G |
| 639-02517 | MLB,2.9G,SAM-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_1T |
| 639-02518 | MLB,2.9G,SAM-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_1T |
| 639-02519 | MLB,2.9G,MIC-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_1T |
| 639-02520 | MLB,2.9G,MIC-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_1T |
| 639-01874 | MLB,3.1G,SAM-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_256G |
| 639-01875 | MLB,3.1G,SAM-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_256G |
| 639-01876 | MLB,3.1G,MIC-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_256G |
| 639-01877 | MLB,3.1G,MIC-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_256G |
| 639-01883 | MLB,3.1G,SAM-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_512G |
| 639-01884 | MLB,3.1G,SAM-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_512G |
| 639-01885 | MLB,3.1G,MIC-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_512G |
| 639-01886 | MLB,3.1G,MIC-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_512G |
| 639-01887 | MLB,3.1G,SAM-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_1T |
| 639-01888 | MLB,3.1G,SAM-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_1T |
| 639-01889 | MLB,3.1G,MIC-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_1T |
| 639-01890 | MLB,3.1G,MIC-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_1T |
| 639-02221 | MLB,3.3G,SAM-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_256G |
| 639-02222 | MLB,3.3G,SAM-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_256G |
| 639-02223 | MLB,3.3G,MIC-8G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_256G |
| 639-02224 | MLB,3.3G,MIC-16G,SAND-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_256G |
| 639-01891 | MLB,3.3G,SAM-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_512G |
| 639-01892 | MLB,3.3G,SAM-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_512G |
| 639-01893 | MLB,3.3G,MIC-8G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_512G |
| 639-01894 | MLB,3.3G,MIC-16G,SAND-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_512G |
| 639-01895 | MLB,3.3G,SAM-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_1T |
| 639-01896 | MLB,3.3G,SAM-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_1T |
| 639-01897 | MLB,3.3G,MIC-8G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_1T |
| 639-01898 | MLB,3.3G,MIC-16G,SAND-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_1T |

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|---------------------------------|--|
| 639-01988 | MLB,NO CPU,X362 | BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,SAND_512G |
| 639-01989 | MLB,CPU SOCKET,X362 | BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_16G_SAMSUNG_2133,SAND_512G |
| 639-02521 | MLB,2.9G,SAM-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_256G |
| 639-02522 | MLB,2.9G,SAM-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_256G |
| 639-02523 | MLB,2.9G,MIC-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_256G |
| 639-02524 | MLB,2.9G,MIC-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_256G |
| 639-02525 | MLB,2.9G,SAM-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_512G |
| 639-02526 | MLB,2.9G,SAM-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_512G |
| 639-02527 | MLB,2.9G,MIC-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_512G |
| 639-02528 | MLB,2.9G,MIC-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_512G |
| 639-02529 | MLB,2.9G,SAM-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_1T |
| 639-02530 | MLB,2.9G,SAM-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_1T |
| 639-02531 | MLB,2.9G,MIC-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_1T |
| 639-02532 | MLB,2.9G,MIC-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_1T |
| 639-02533 | MLB,3.1G,SAM-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_256G |
| 639-02534 | MLB,3.1G,SAM-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_256G |
| 639-02535 | MLB,3.1G,MIC-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_256G |
| 639-02536 | MLB,3.1G,MIC-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_256G |
| 639-02537 | MLB,3.1G,SAM-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_512G |
| 639-02538 | MLB,3.1G,SAM-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_512G |
| 639-02539 | MLB,3.1G,MIC-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_512G |
| 639-02540 | MLB,3.1G,MIC-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_512G |
| 639-02541 | MLB,3.1G,SAM-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_1T |
| 639-02542 | MLB,3.1G,SAM-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_1T |
| 639-02543 | MLB,3.1G,MIC-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_1T |
| 639-02544 | MLB,3.1G,MIC-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_1T |
| 639-02545 | MLB,3.3G,SAM-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_256G |
| 639-02546 | MLB,3.3G,SAM-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_256G |
| 639-02547 | MLB,3.3G,MIC-8G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_256G |
| 639-02548 | MLB,3.3G,MIC-16G,TOSH-256G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_256G |
| 639-02549 | MLB,3.3G,SAM-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_512G |
| 639-02550 | MLB,3.3G,SAM-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_512G |
| 639-02551 | MLB,3.3G,MIC-8G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_512G |
| 639-02552 | MLB,3.3G,MIC-16G,TOSH-512G,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_512G |
| 639-02553 | MLB,3.3G,SAM-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_1T |
| 639-02554 | MLB,3.3G,SAM-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_1T |
| 639-02555 | MLB,3.3G,MIC-8G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_1T |
| 639-02556 | MLB,3.3G,MIC-16G,TOSH-1T,X362 | BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_1T |

Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|-------------------------------------|
| 152S00367 | 152S00266 | | ALL | Text note to be updated |
| 152S00368 | 152S00269 | | ALL | Text note to be updated |
| 152S00370 | 152S00270 | | ALL | Text note to be updated |
| 353S4068 | 353S4070 | | ALL | Text note to be updated |
| 353S00772 | 353S4070 | | ALL | Text note to be updated |
| 138S00086 | 138S0884 | | ALL | Text note to be updated |
| 107S0248 | 107S0250 | | ALL | TFT alt to Cyntec |
| 152S00434 | 152S1829 | | ALL | Text note to be updated |
| 371S00019 | 371S0463 | | ALL | Rohm alt to Rohm |
| 353S00107 | 353S3239 | ANY | ALL | Onsemi alt to Intersil |
| 353S00231 | 353S3987 | | ALL | NXP alt to TI |
| 333S00025 | 333S00055 | POP_4GBIT | ALL | MICRON SSD POP ALT for HYNIX |
| 333S00026 | 333S00056 | POP_8GBIT | ALL | MICRON SSD POP ALT for HYNIX |
| 333S00107 | 333S00055 | POP_4GBIT | ALL | HYNIX SSD POP REPLACEMENT for HYNIX |
| 333S00108 | 333S00056 | POP_8GBIT | ALL | HYNIX SSD POP REPLACEMENT for HYNIX |

| | | | | |
|-----------|-----------|--|-----|-------------------------|
| 138S0701 | 138S0689 | | ALL | Text note to be updated |
| 138S00012 | 138S0771 | | ALL | Text note to be updated |
| 138S0772 | 138S00013 | | ALL | Text note to be updated |
| 152S00401 | 152S0529 | | ALL | Text note to be updated |
| 152S00344 | 152S1683 | | ALL | Text note to be updated |
| 152S00331 | 152S00283 | | ALL | Text note to be updated |
| 152S2034 | 152S00190 | | ALL | Text note to be updated |
| 197S0613 | 197S0612 | | ALL | Text note to be updated |
| 311S00121 | 311S0398 | | ALL | Text note to be updated |
| 371S0713 | 371S0558 | | ALL | Text note to be updated |
| 371S00074 | 371S0602 | | ALL | Text note to be updated |

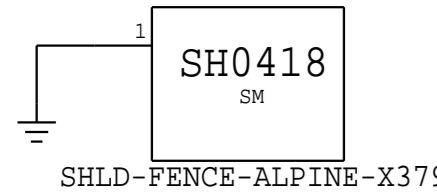
| | | |
|------------------------------------|--|------------------------------|
| DRAWING NUMBER 051-00777 | | STEP D |
| REVISION 9.0.0 | | BRANCH dvt-fab09-0 |
| PAGE 3 OF 145 | | SHEET 3 OF 119 |

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
I NOT TO REPRODUCE OR COPY IT
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
I ALL RIGHTS RESERVED

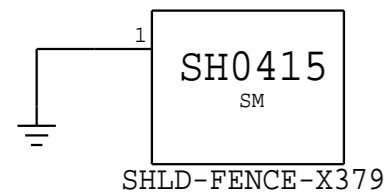
BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

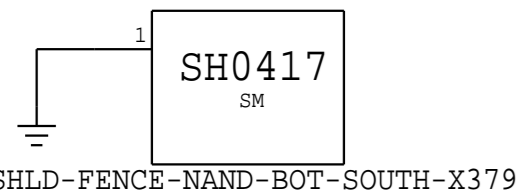
ALPINE RIDGE - LIO (U2800) - 806-06077



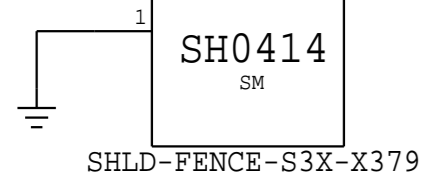
LPDDR3 (U2300 ~ U2600) - 806-06167



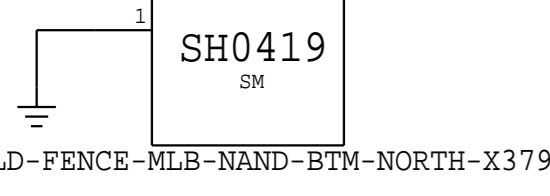
NAND - BOTTOM SOUTH (U9120) - 806-05945



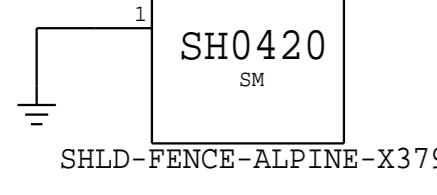
S3X (U8600) - 806-06023



NAND - BOTTOM NORTH (U9200) - 806-06265

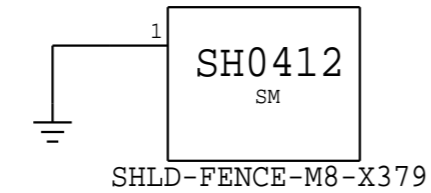


ALPINE RIDGE - RIO (UB000) - 806-06077

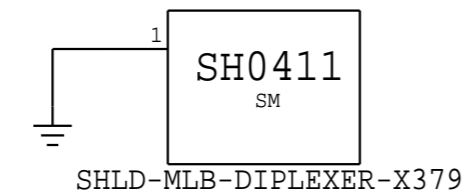


Shield Cans - TOP SIDE

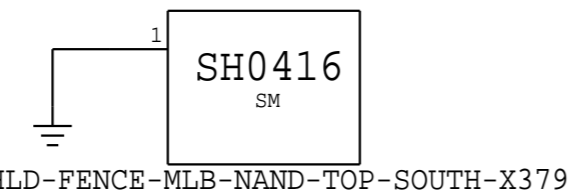
T208 (U3900) - 806-06264



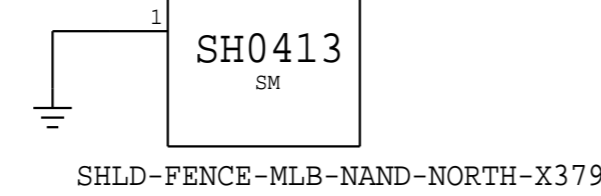
DIPLEXERS - 806-06266



NAND - TOP SOUTH (U9100) - 806-06262

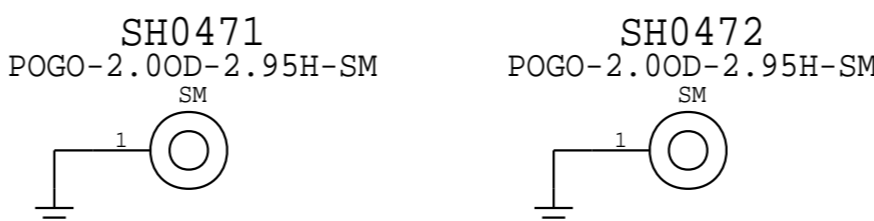


NAND - TOP NORTH (9220) - 806-06258

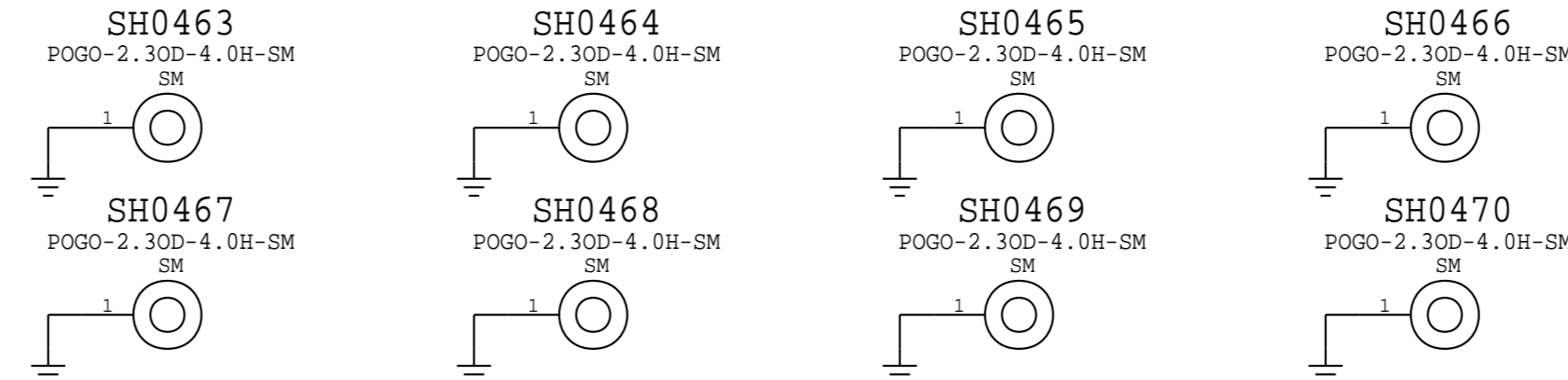


POGO PINS

LIO and RIO -2X (870-5071)

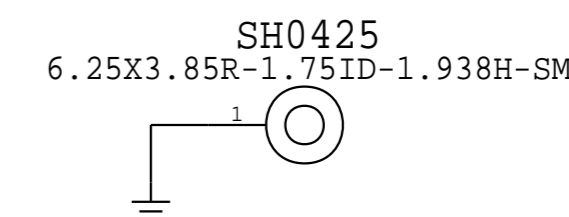


AROUND THE FAN AND CENTER - 8X (870-01518)

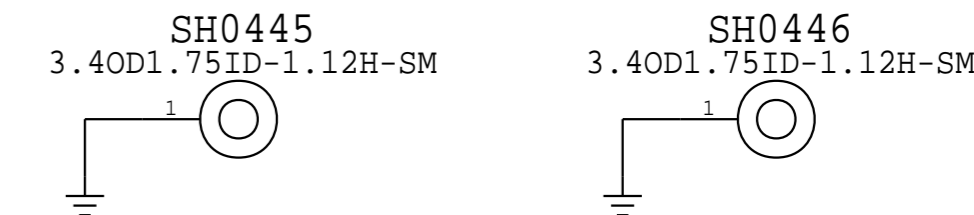


Cowling Bosses - BOTTOM SIDE

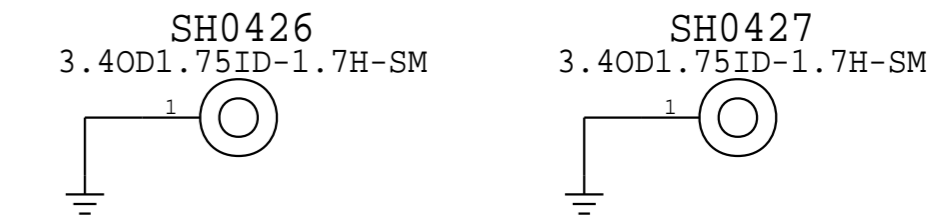
DFR TOUCH CONN (J4402) - 860-00414



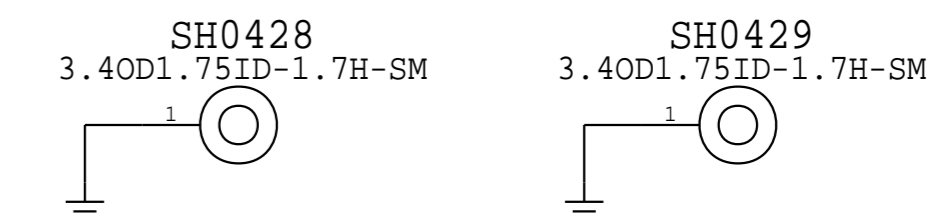
USB-C CONN - LIO (J3300) - 860-00392



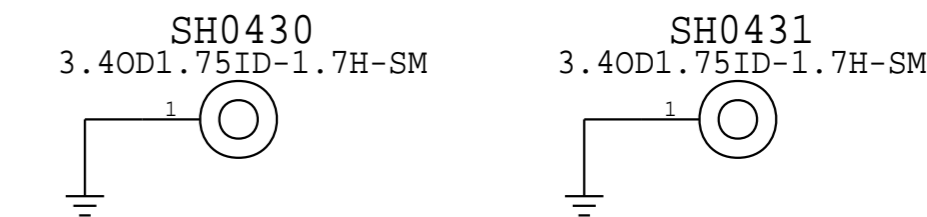
DFR DISPLAY CONN (J4401) - 860-00412



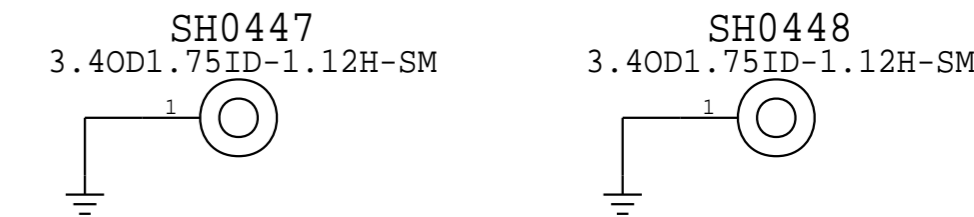
IPD CONN (J4501) - 860-00412



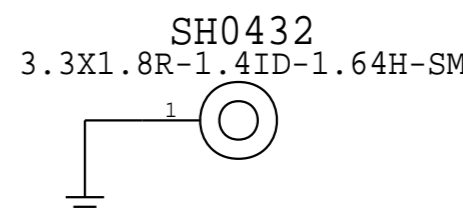
KBD CONN (J4500) - 860-00412



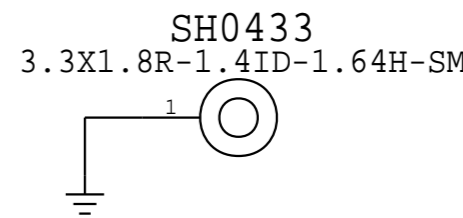
USB-C CONN - RIO (JB500) - 860-00392



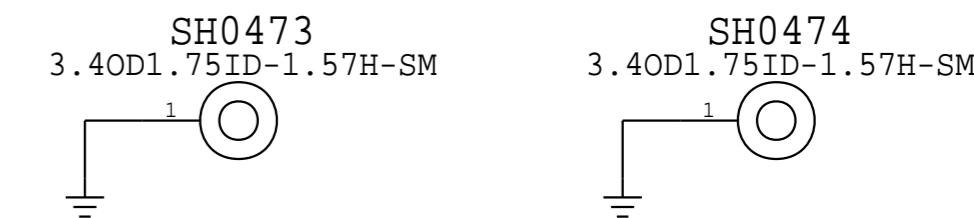
AUDIO JACK CONN (J6600) - 860-00399



MESA CONN (J4900) - 860-00399

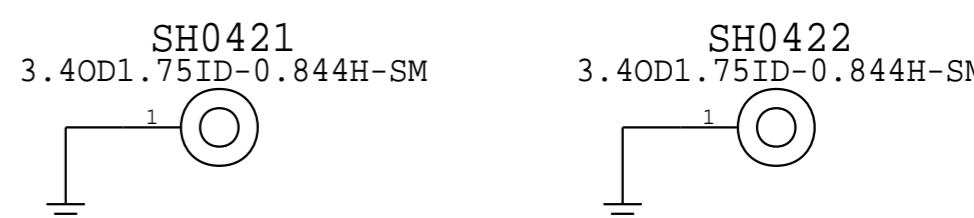


LIFEBOAT CONN (J9600) - 860-00413

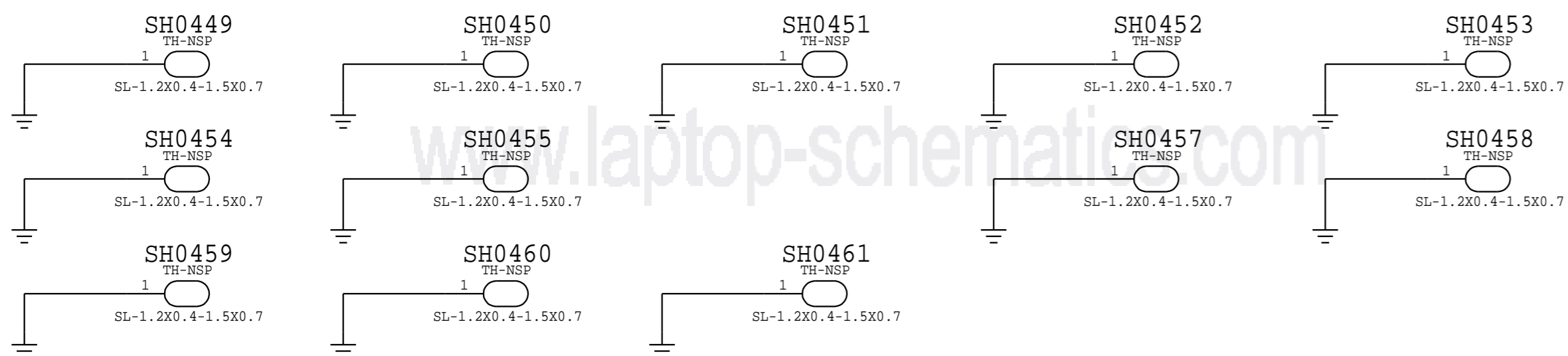


Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415

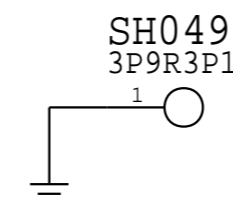


Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

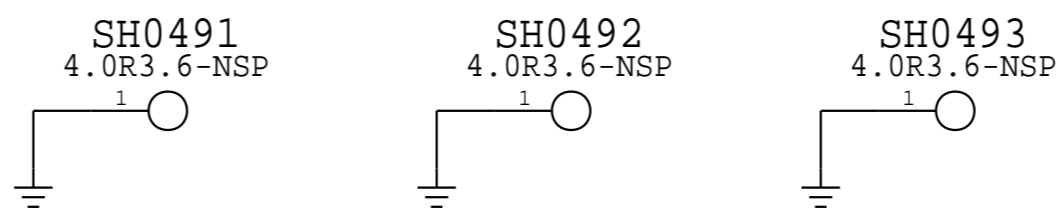


Thermal Stage Mounting Holes

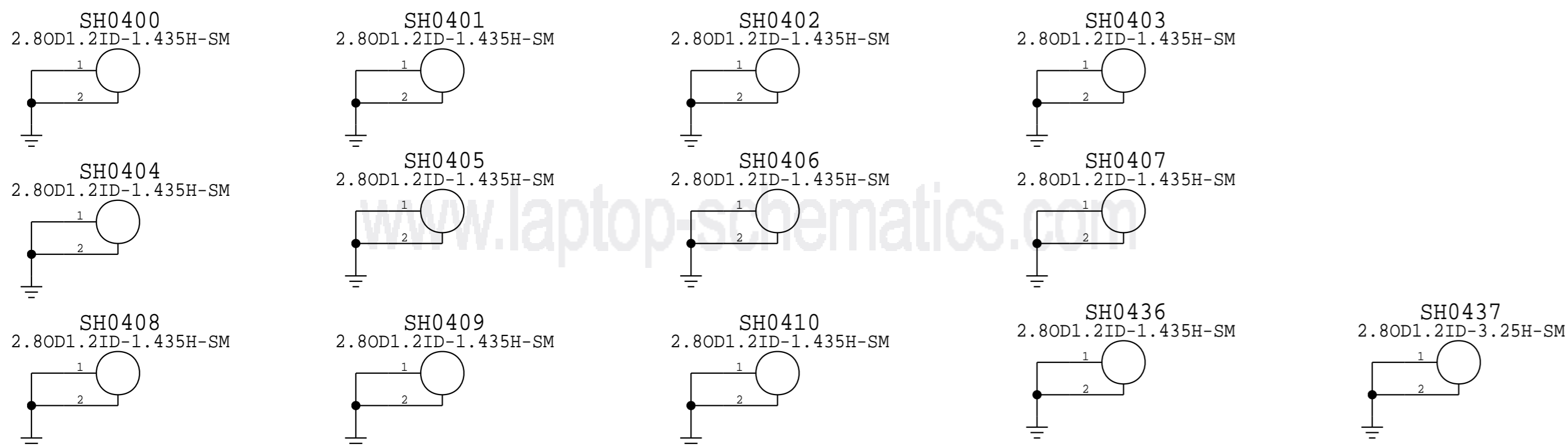
Plated Through Hole - 3.15mm - APN 998-0845



Plated Through Hole - 3.6mm - APN 998-03850



TOP Rubber Mount Standoffs - 12X - (860-00430)



Bottom Rubber Mount Standoffs - 1X - (860-00476)

| | | | |
|---|------------|----------------------|-------------|
| SYNC_MASTER=LDUNN_J44 | | SYNC_DATE=01/13/2013 | |
| PAGE TITLE | | | |
| PD Parts | | | |
| | Apple Inc. | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 4 OF 145 |
| | | SHEET | 4 OF 119 |

D

D

C

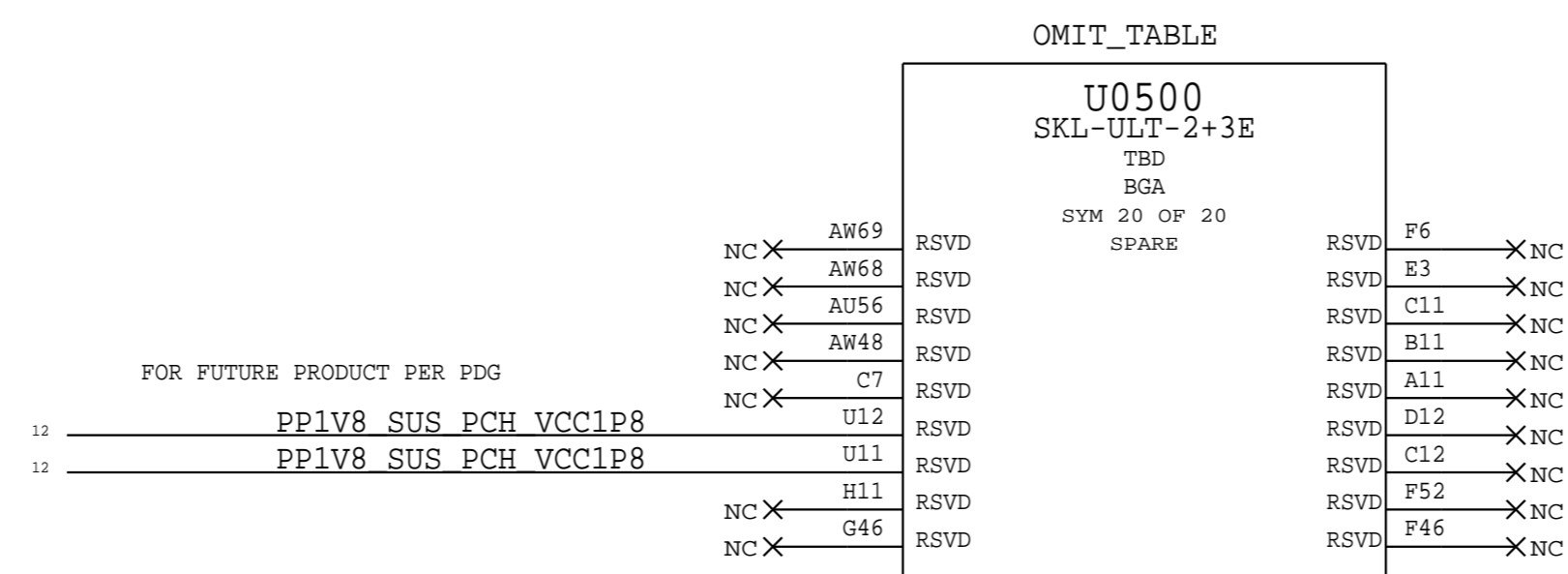
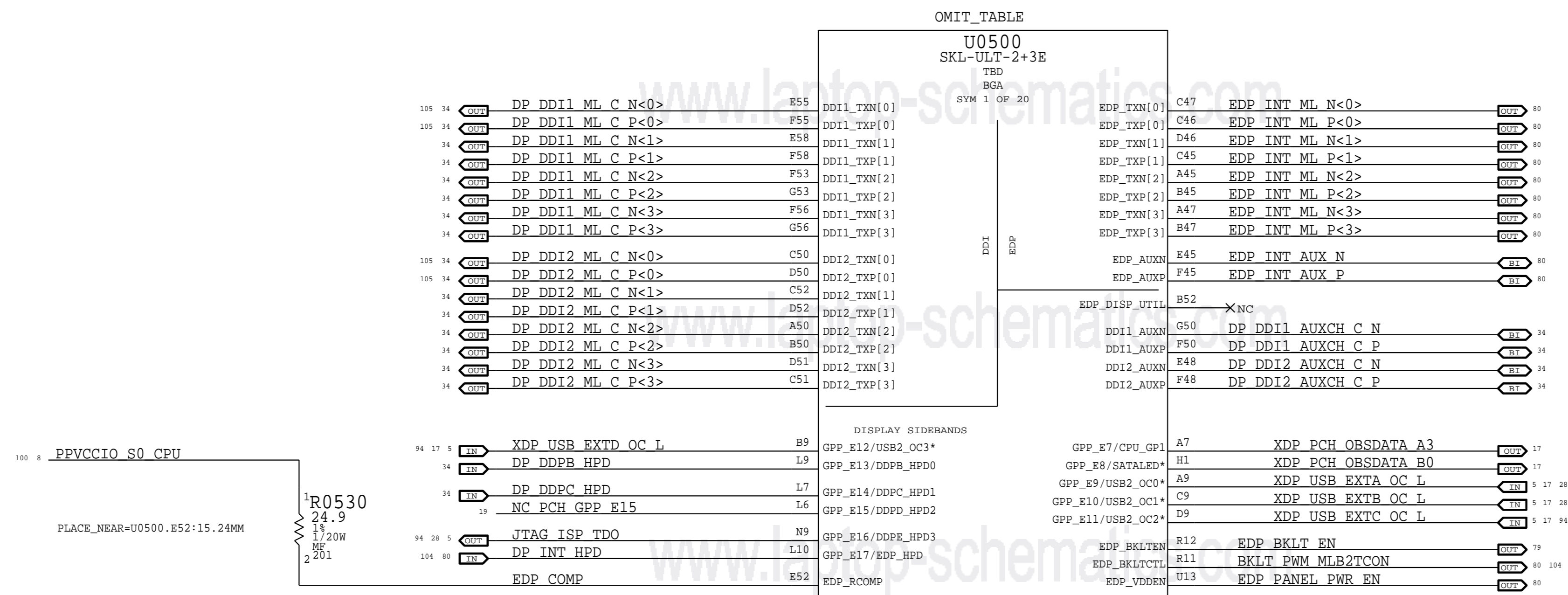
C

B

B

A

A



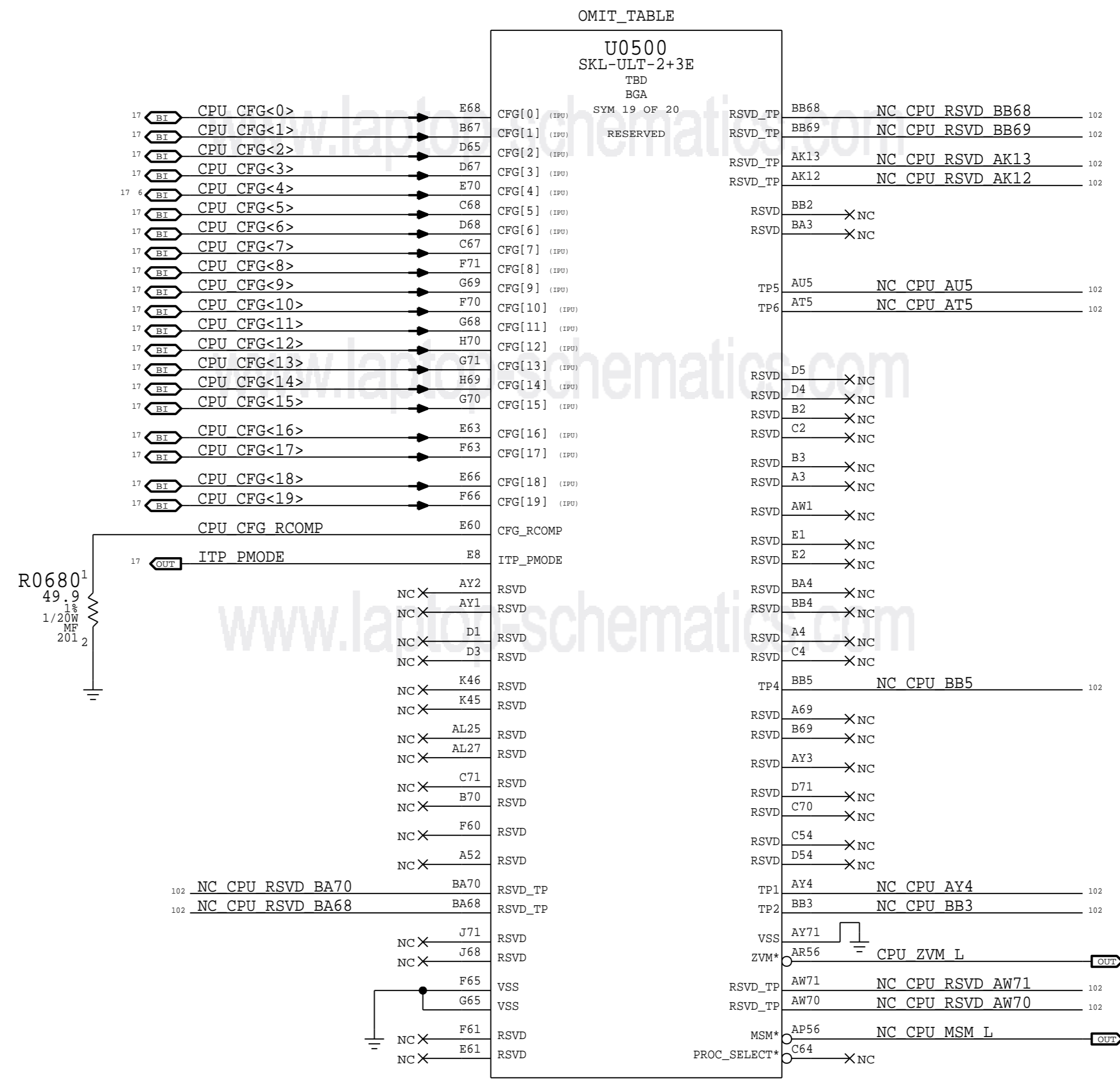
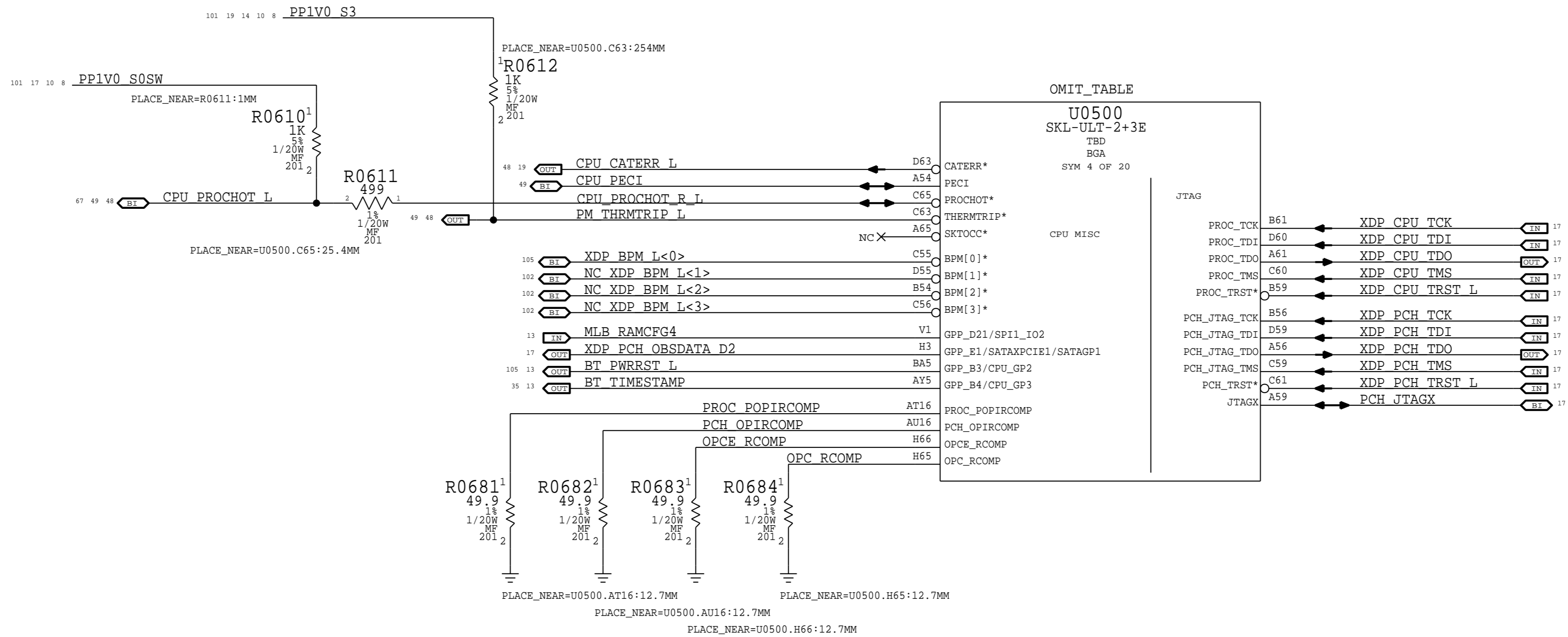
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Tue Apr 28 20:32:21 2015

CPU GFX

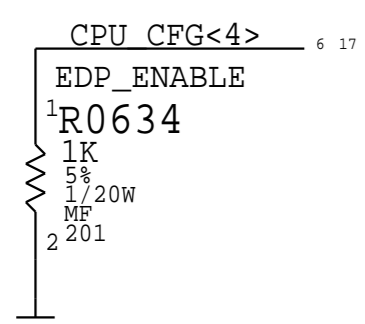
Apple Inc.

DRWGING NUMBER: 051-00777
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 5 OF 145
SHEET: 5 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1V ALL RIGHTS RESERVED



CFG4> :eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED



BOM_COST_GROUP=CPU & CHIPSET

| | |
|---|--|
| DESIGN: X502/DEV_MLB_U | |
| LAST CHANGE: Mon Apr 27 22:56:39 2015 | |
| PAGE TITLE CPU MISC/JTAG/CFG/RSVD | |
| | DRAWING NUMBER: 051-00777 REVISION: 9.0.0 BRANCH: dvt-fab09-0 PAGE: 6 OF 145 SHEET: 6 OF 119 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 11 ALL RIGHTS RESERVED | |

D

D

C

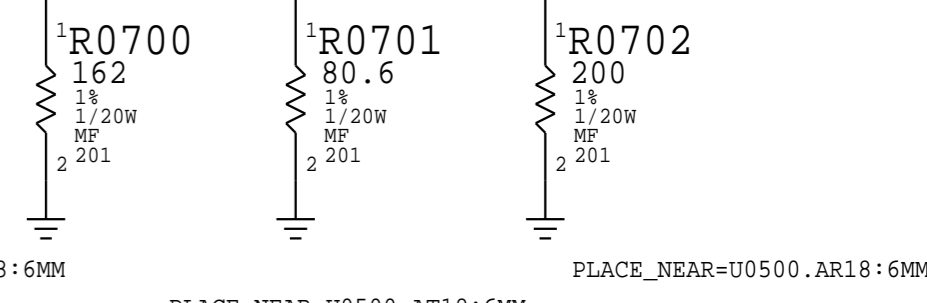
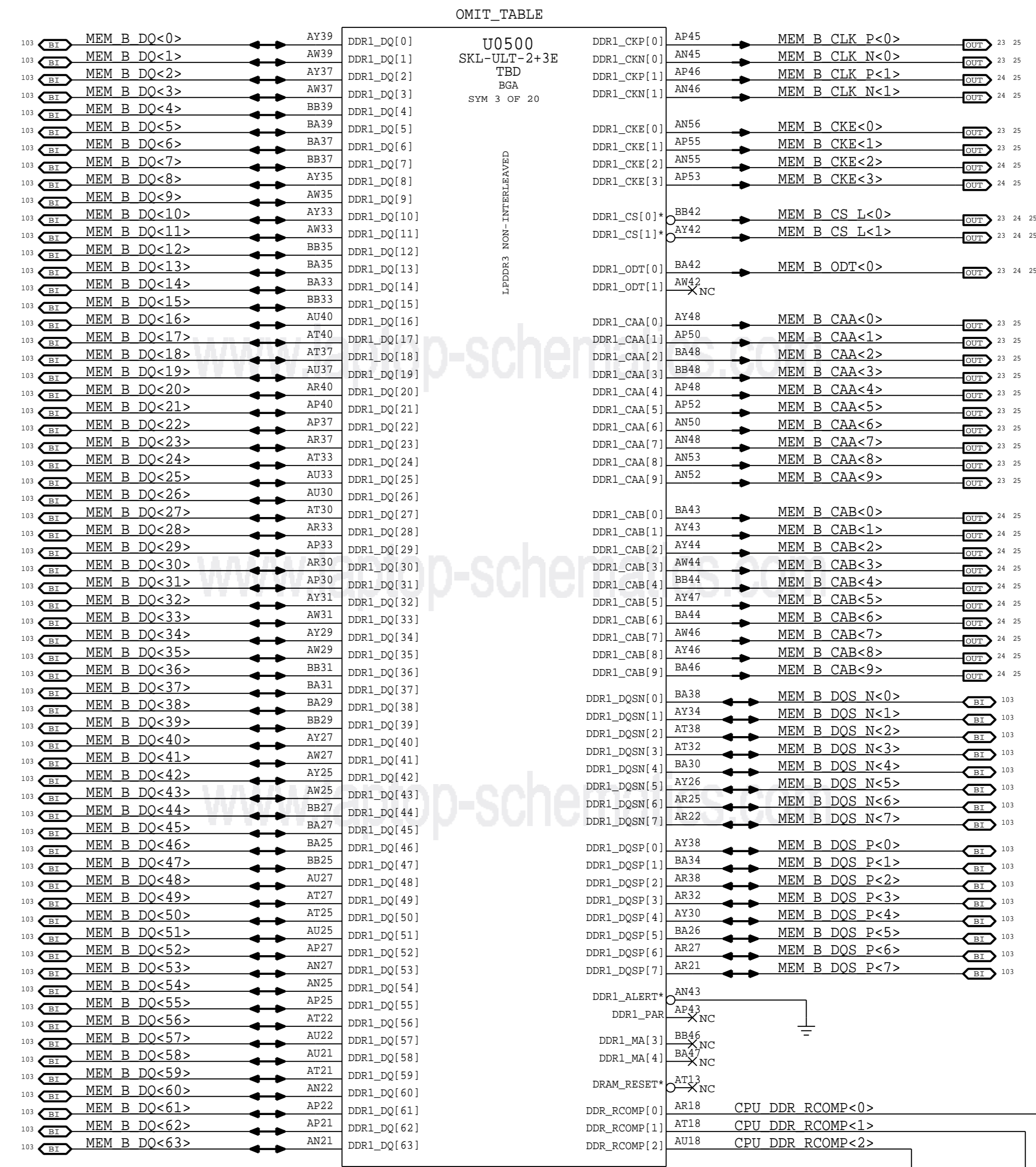
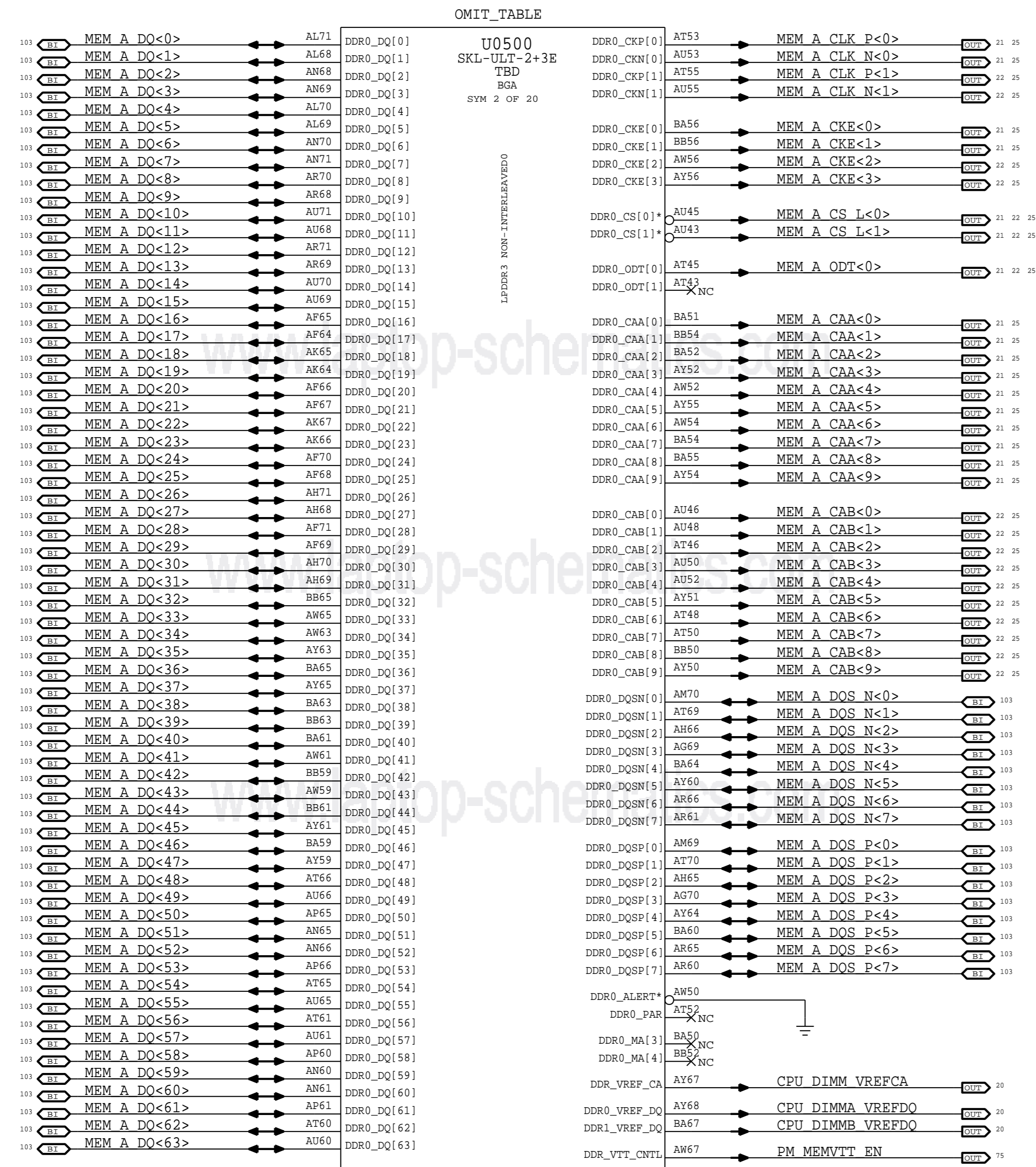
C

B

B

A

A



SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE CPU LPDDR3 Interface

| | | | | |
|---|----------------|-----------|-------------|---|
| Apple Inc. | DRAWING NUMBER | 051-00777 | STEP | D |
| | REVISION | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | 7 OF 145 | |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | SHEET | 7 OF 119 | |

D

D

C

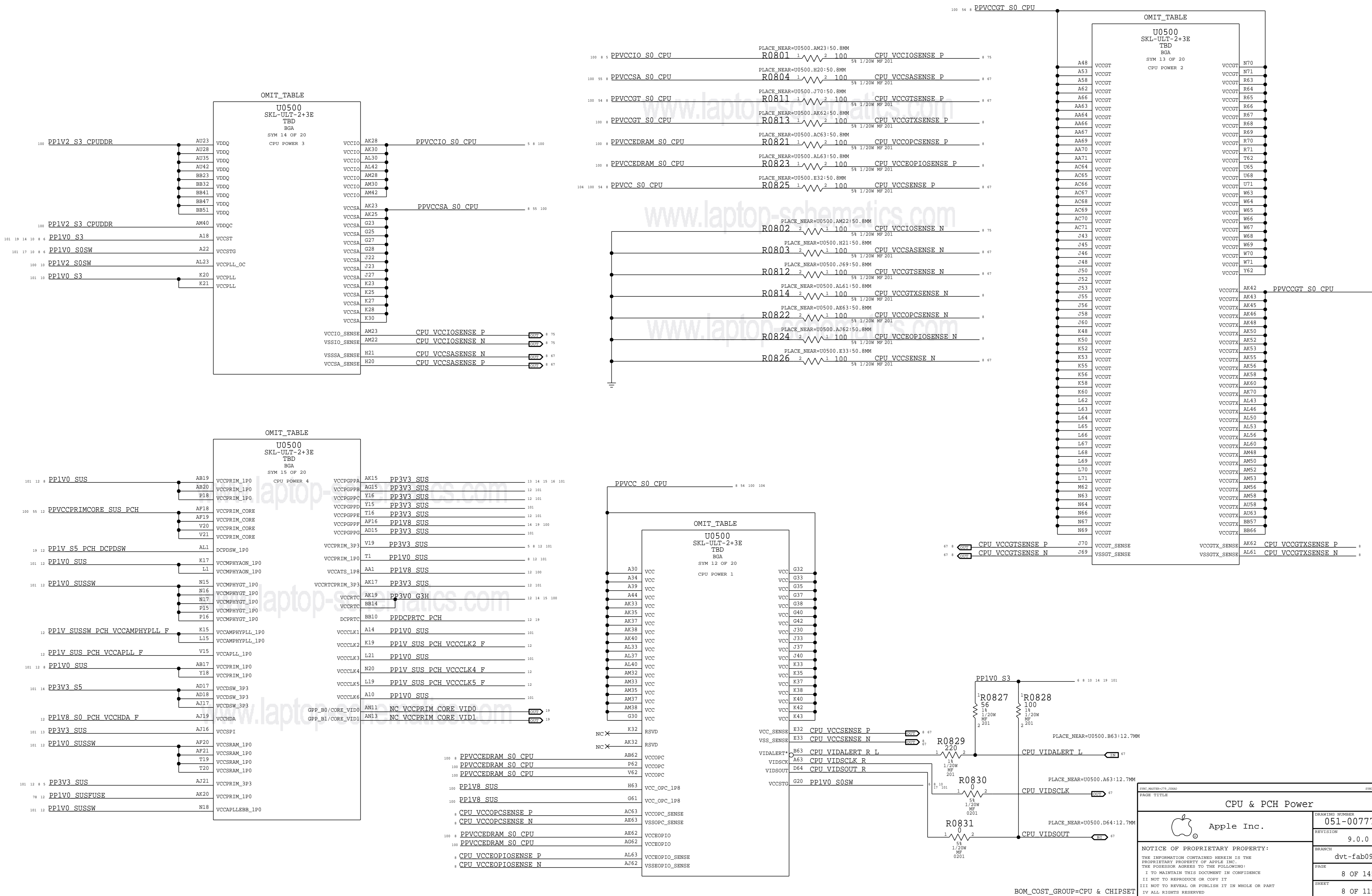
C

B

B

A

A



CPU & PCH Power

Apple Inc.

| | | | |
|----------------|-----------|----------|-------------|
| DRAWING NUMBER | 051-00777 | STEP | D |
| REVISION | 9.0.0 | BRANCH | dvt-fab09-0 |
| PAGE | | 8 OF 145 | |
| SHEET | | 8 OF 119 | |

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1111 ALL RIGHTS RESERVED

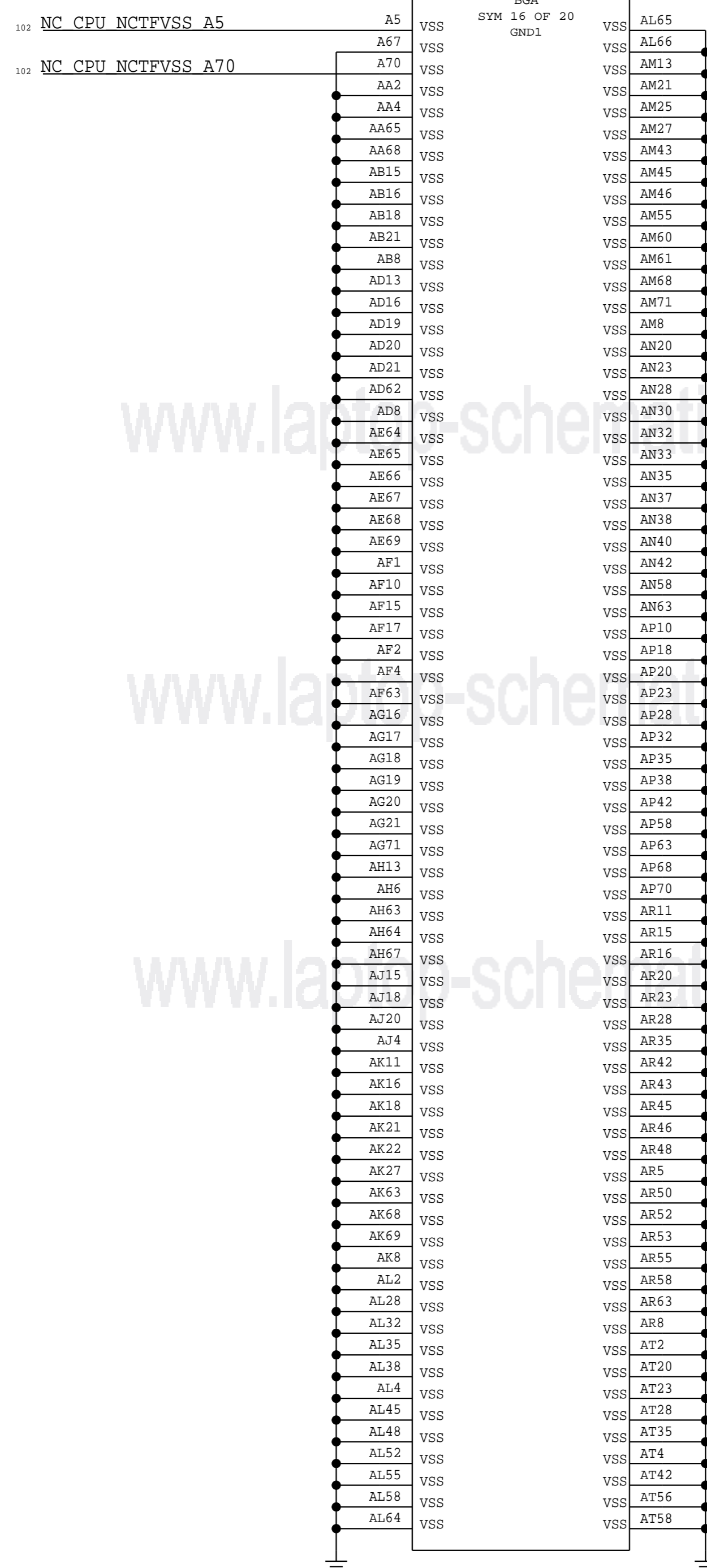
BOM_COST_GROUP=CPU & CHIPSET

OMIT_TABLE

U0500
SKL-ULT-2+3E

TBD
BGA

SYM 16 OF 20
GND1

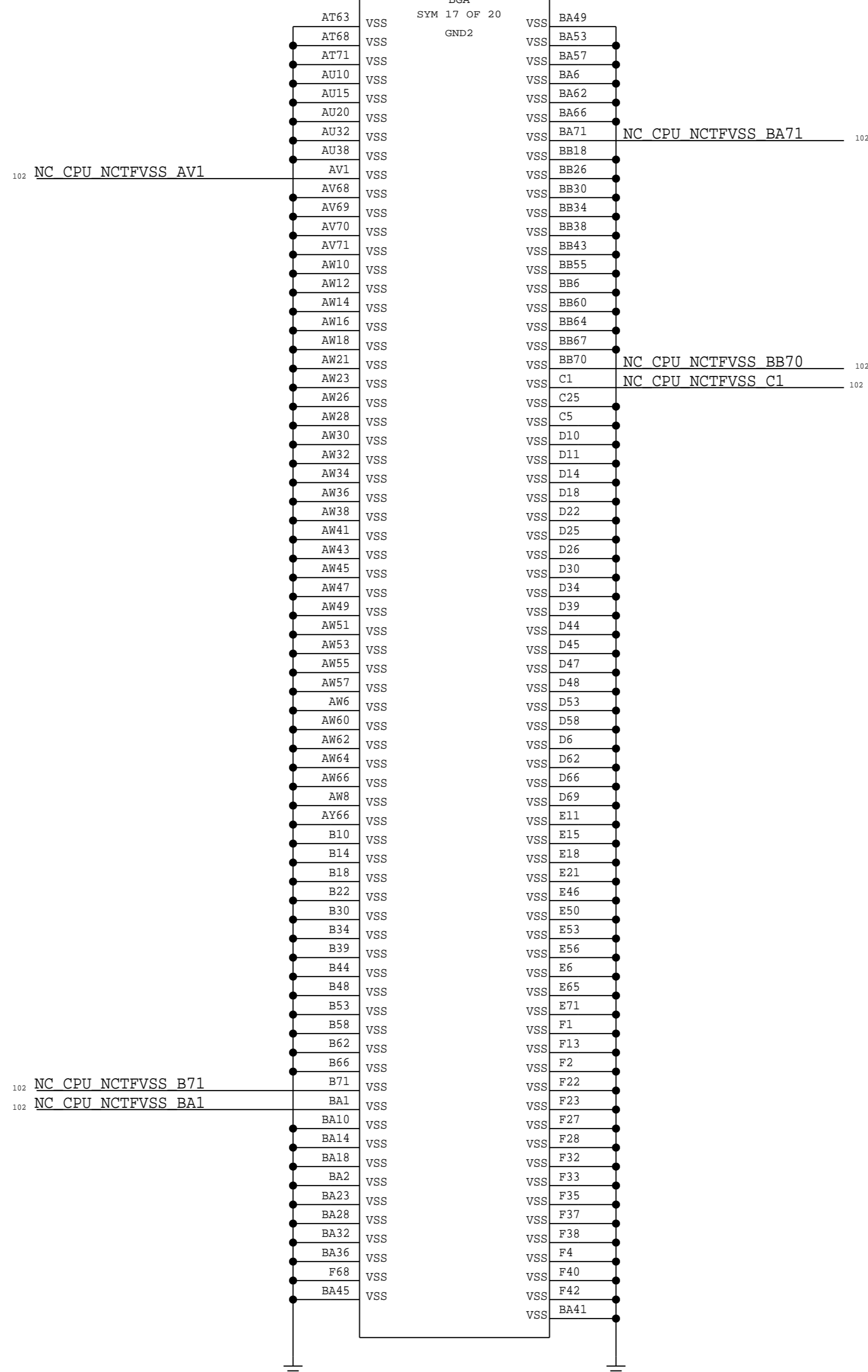


OMIT_TABLE

U0500
SKL-ULT-2+3E

TBD
BGA

SYM 17 OF 20
GND2

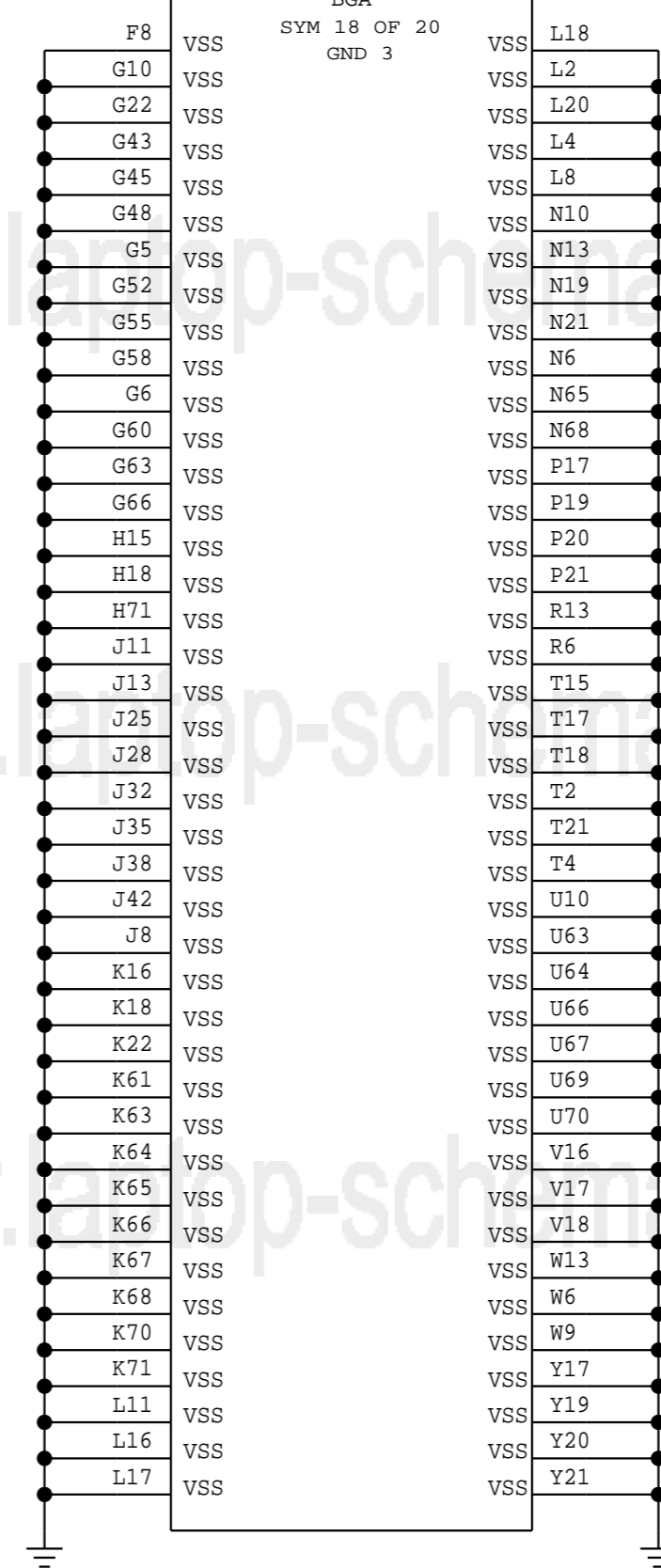


OMIT_TABLE

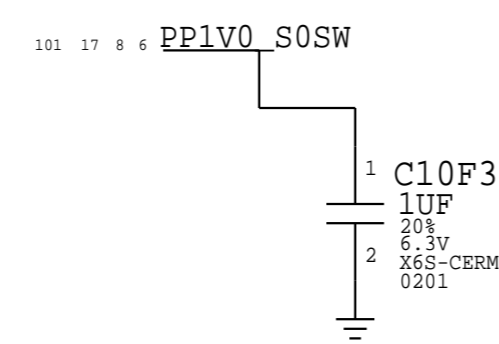
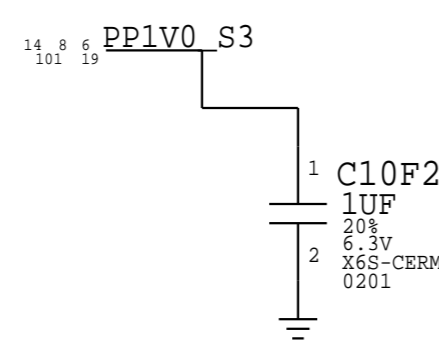
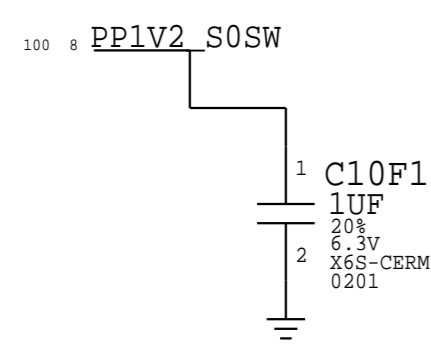
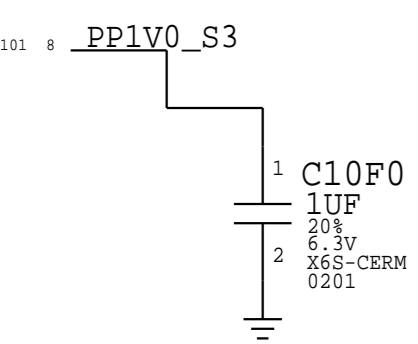
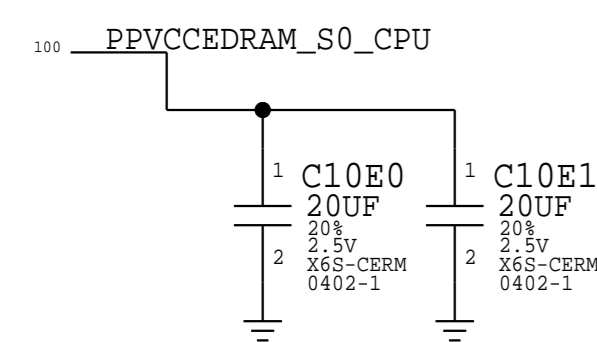
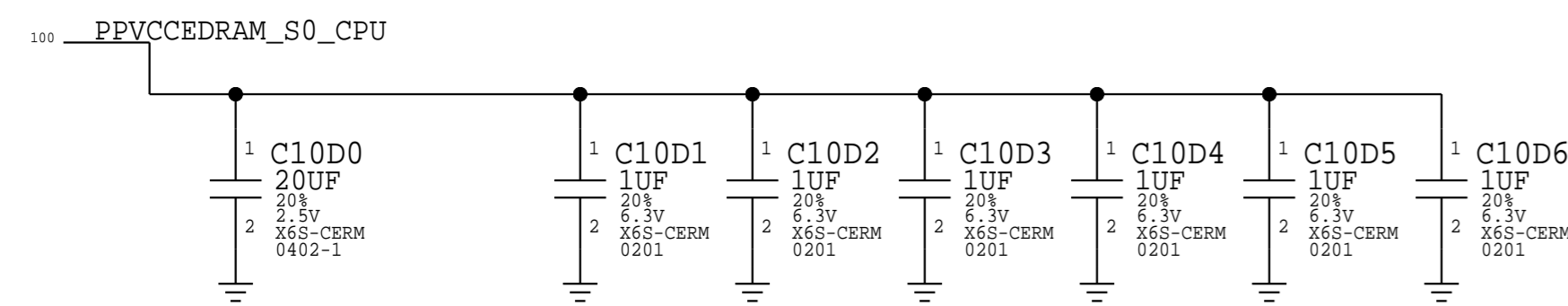
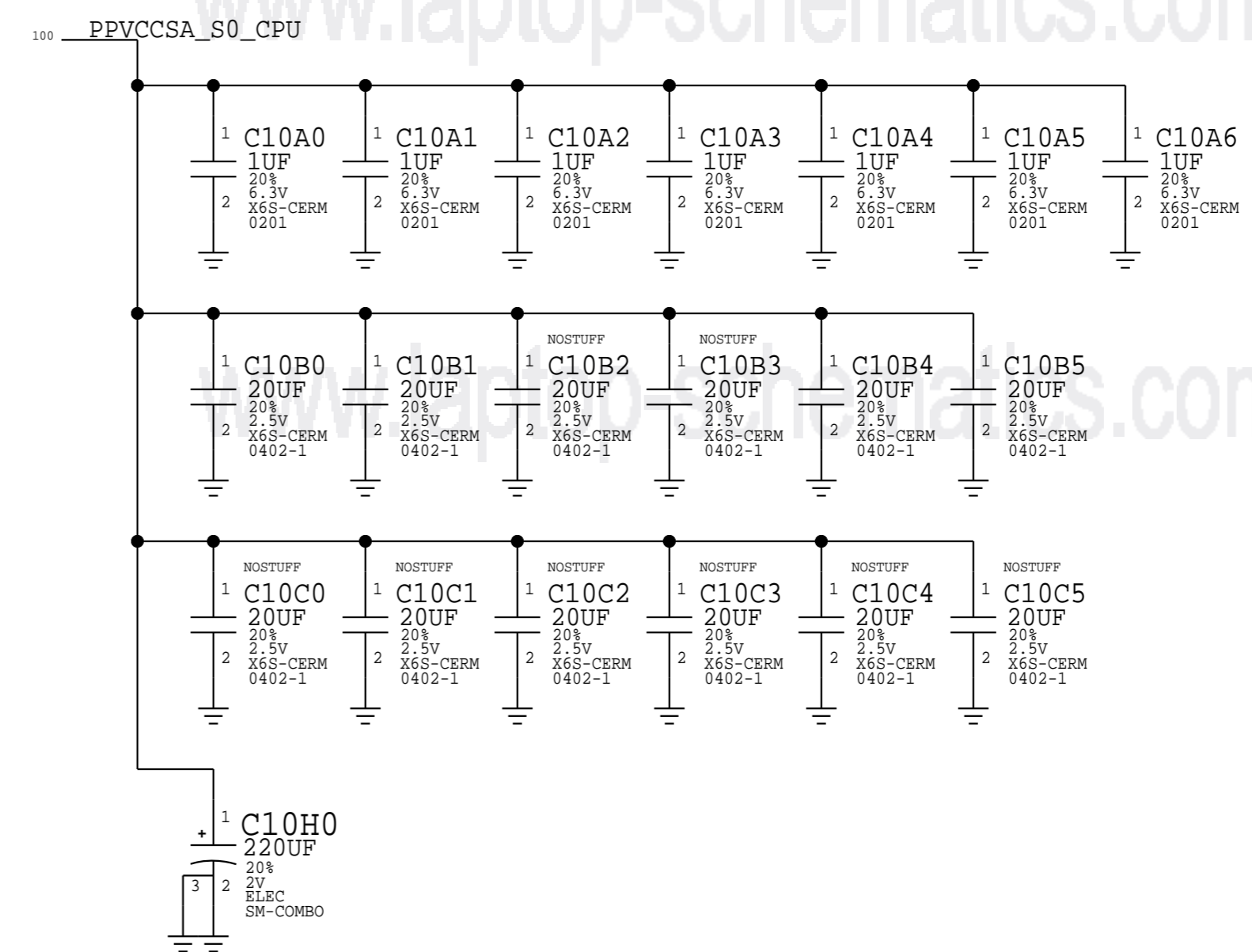
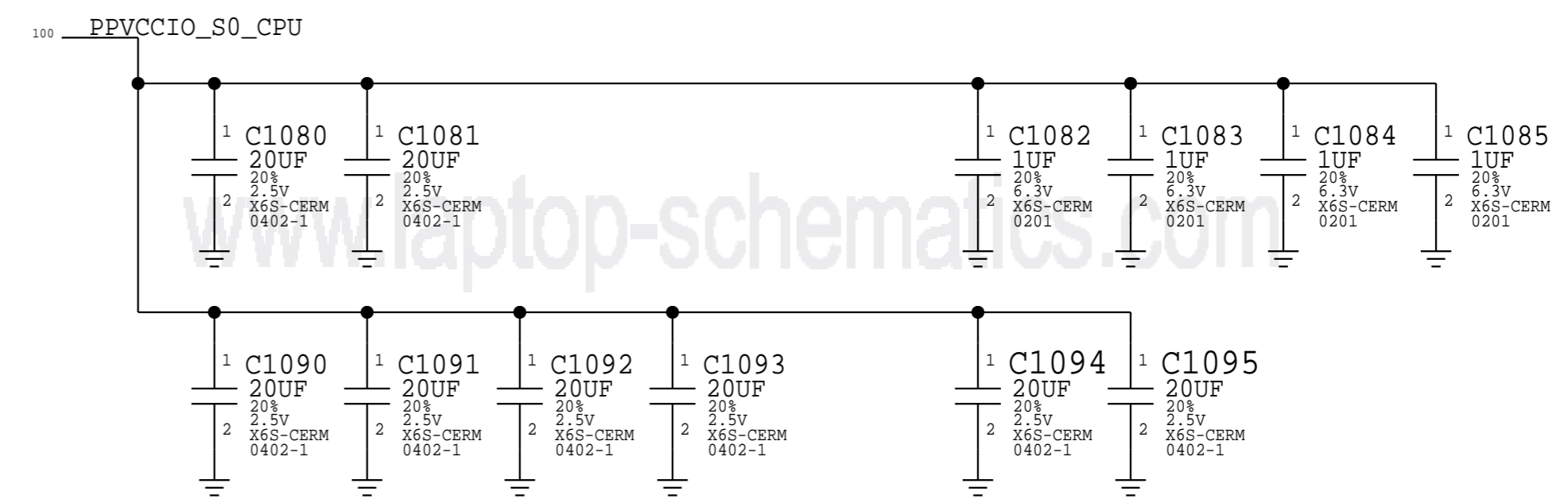
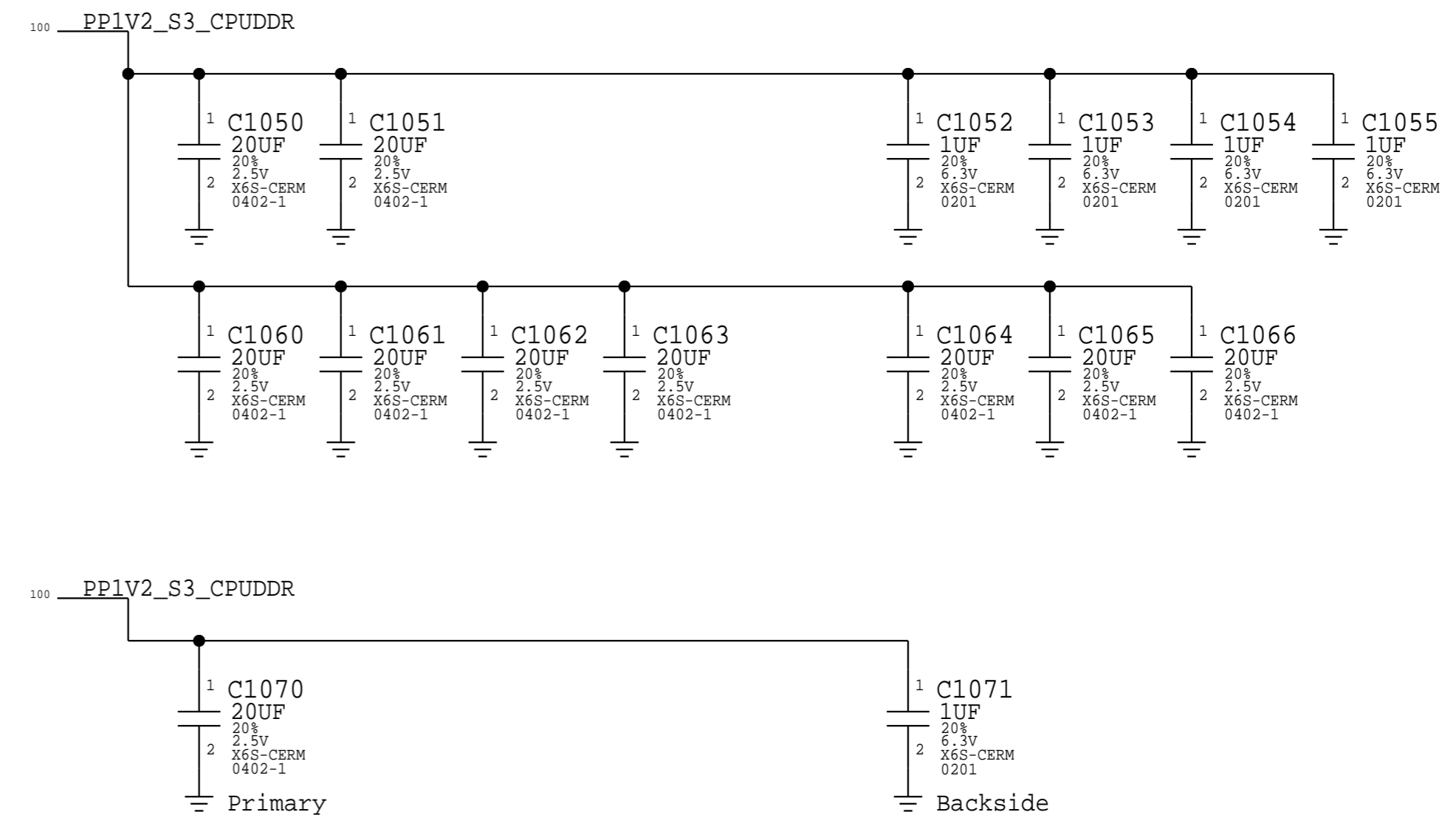
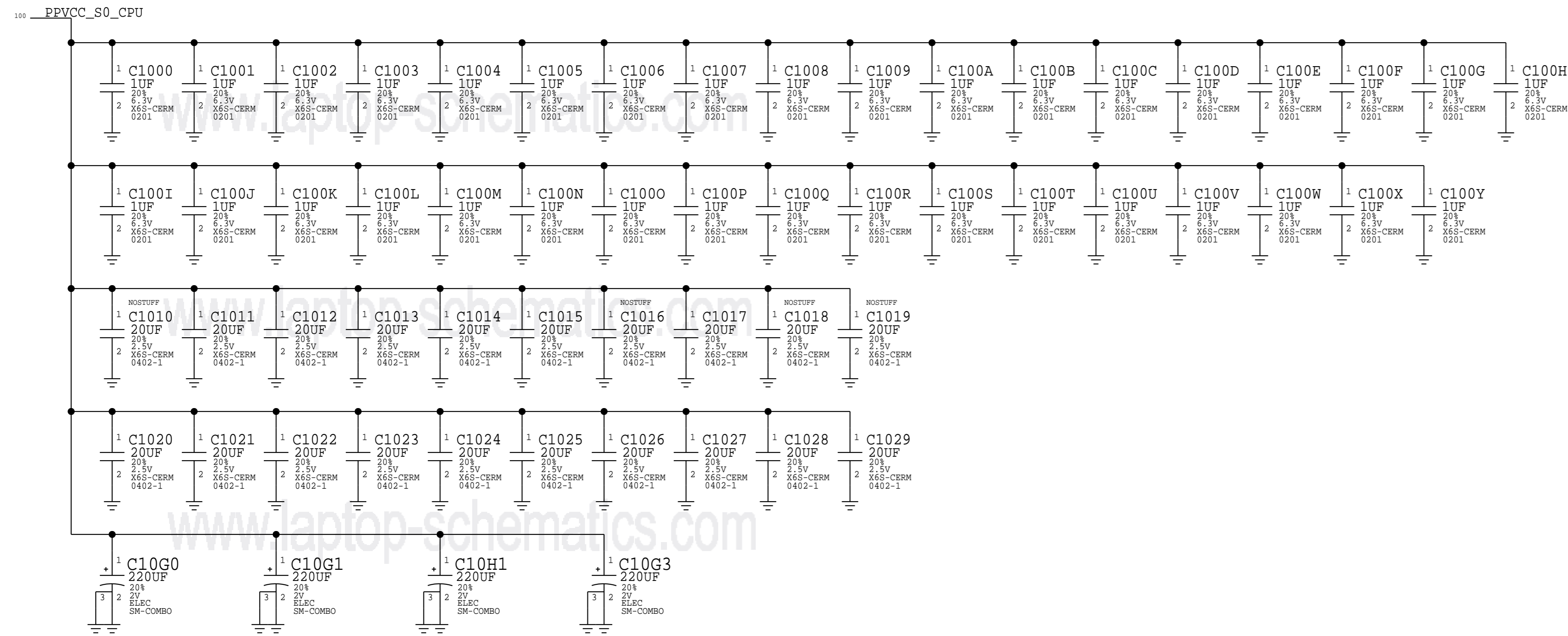
U0500
SKL-ULT-2+3E

TBD
BGA

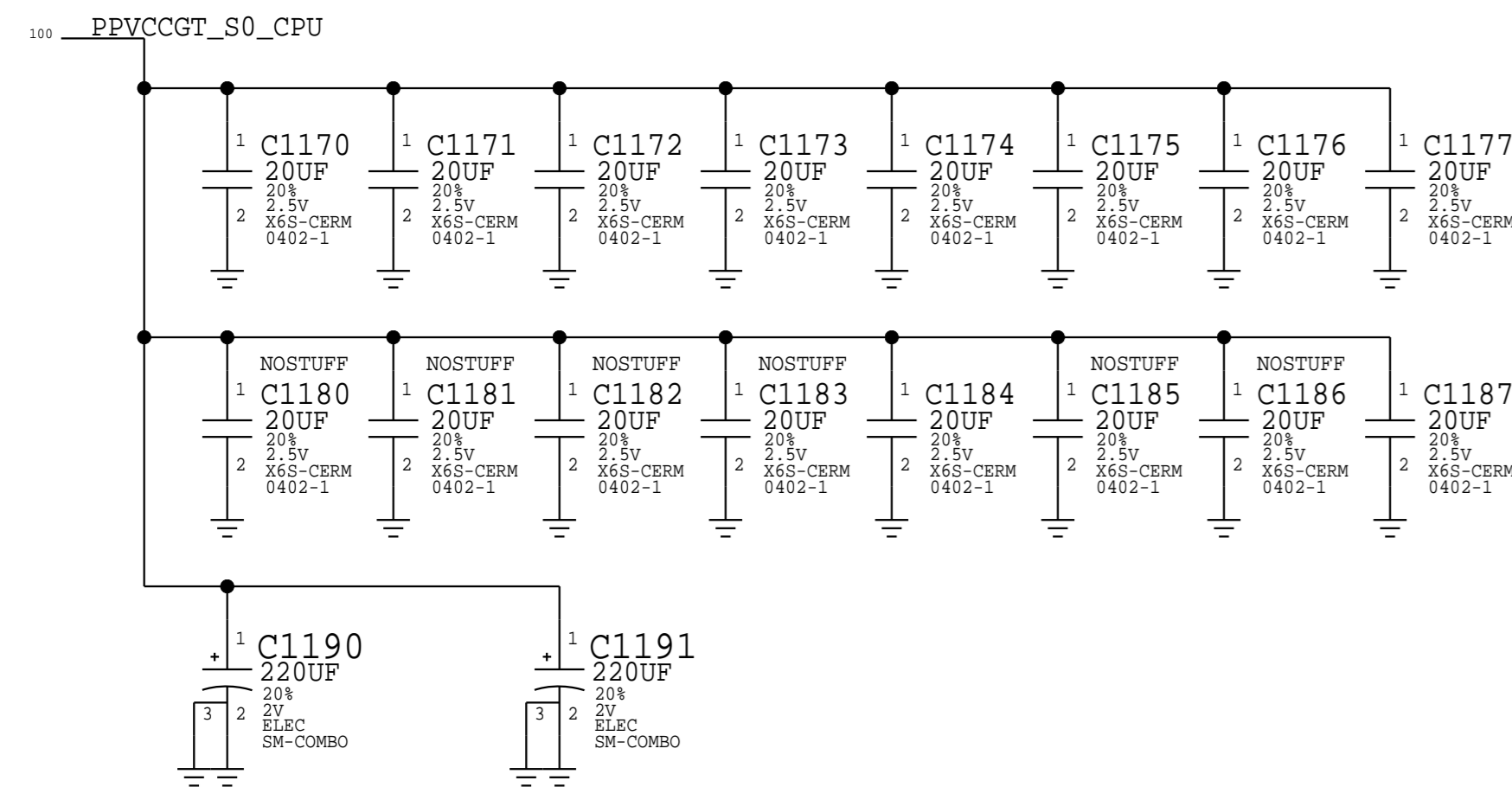
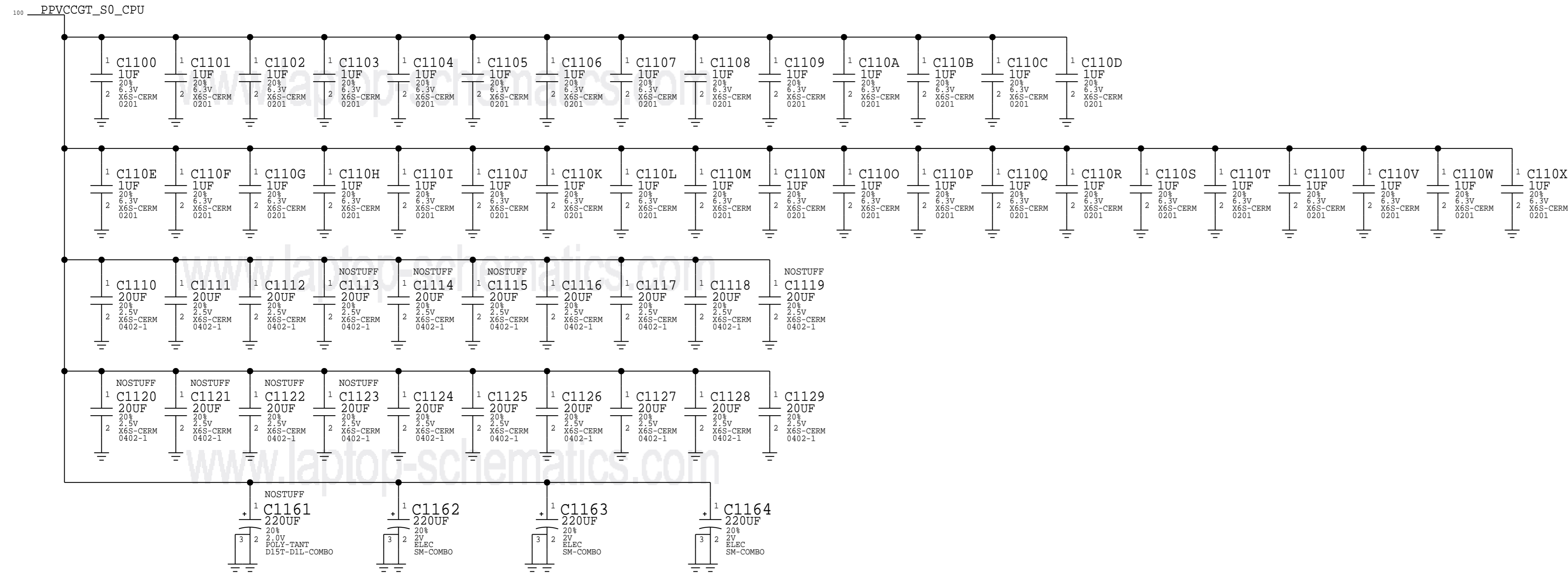
SYM 18 OF 20
GND 3



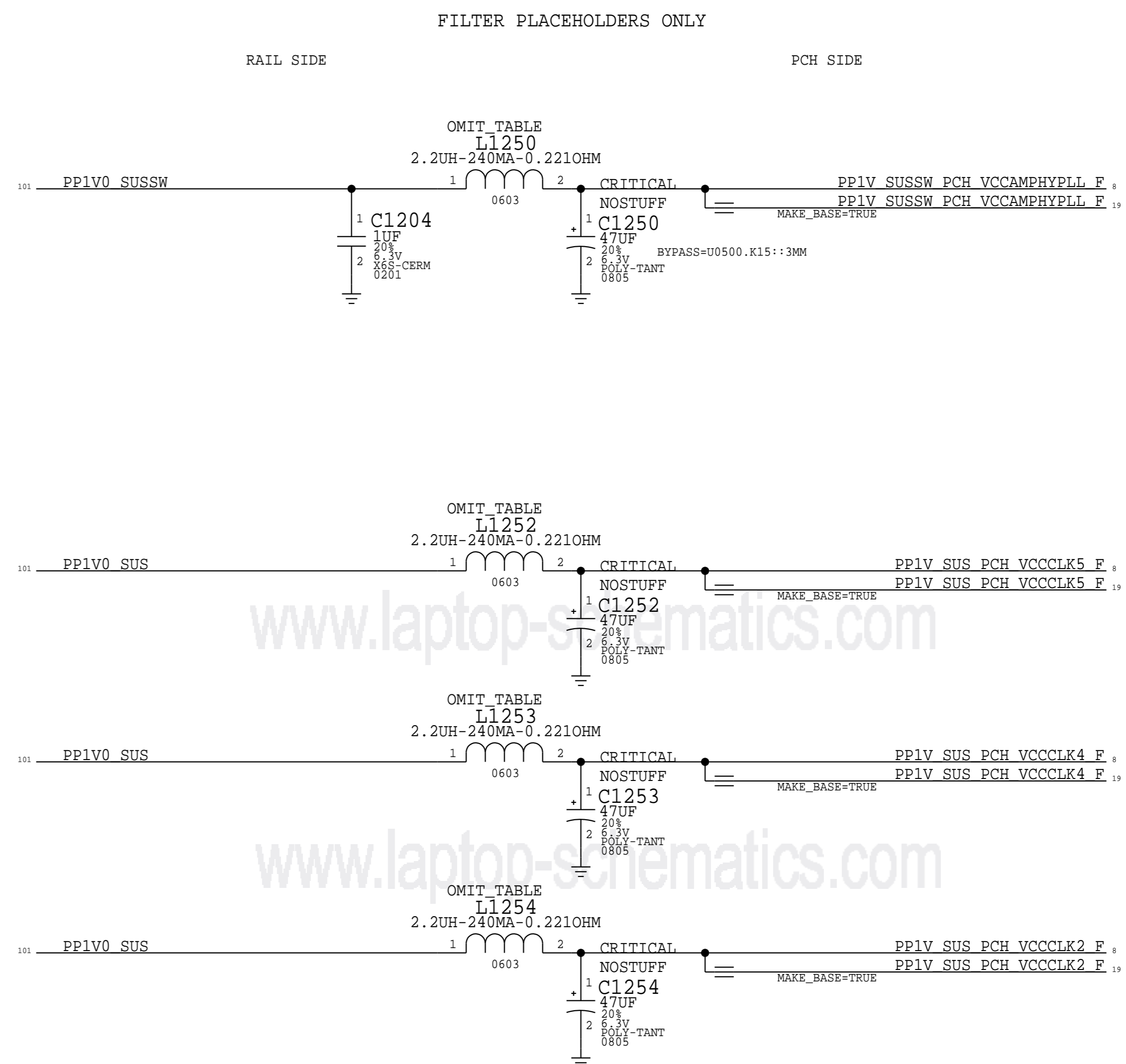
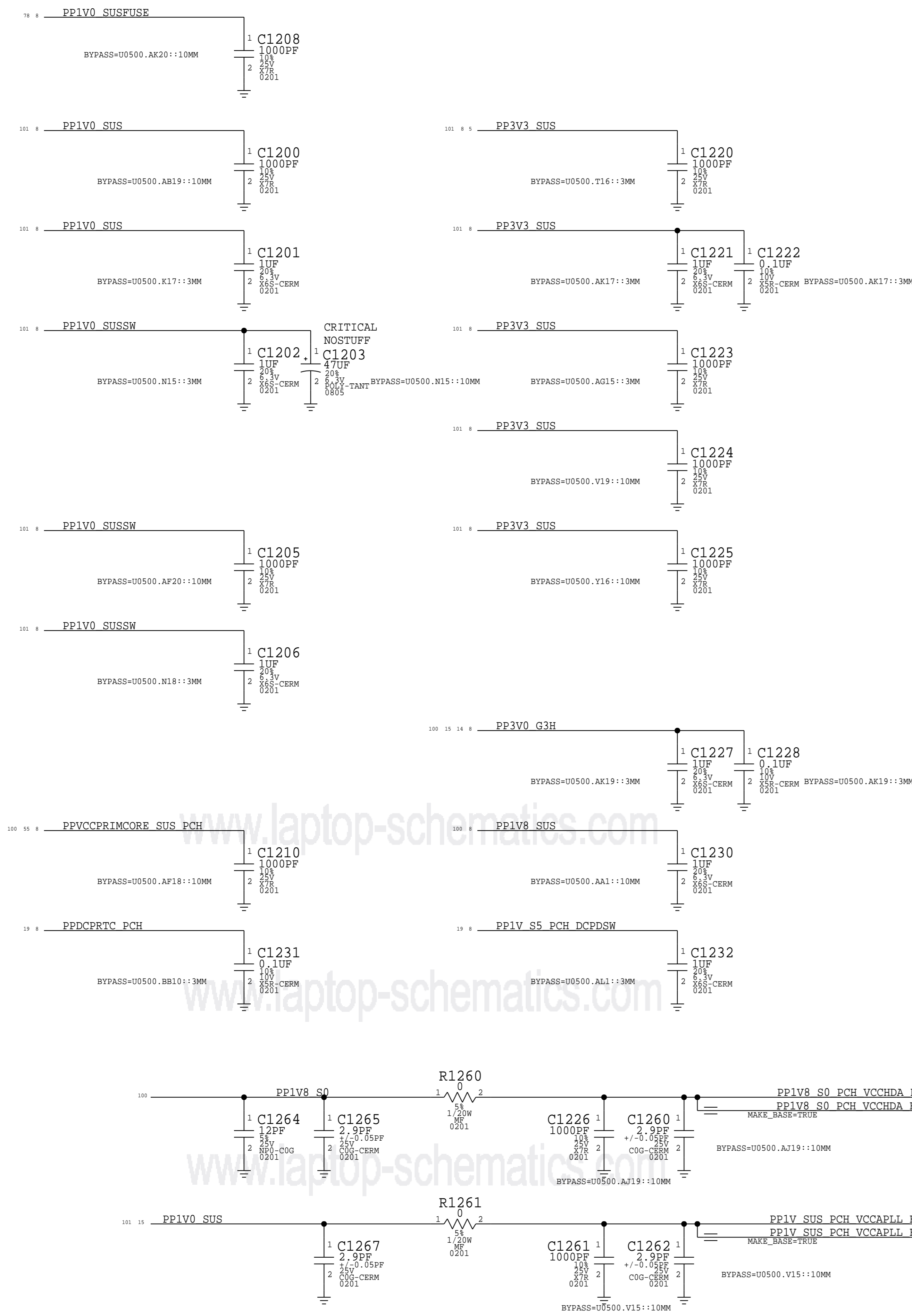
| | | | |
|--|----------------|----------------------|-------------|
| EYNC_MASTER=J79_ALFRED | | EYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| CPU & PCH Grounds | | | |
| | DRAWING NUMBER | 051-00777 | STEP |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 9 OF 145 |
| | | SHEET | 9 OF 119 |



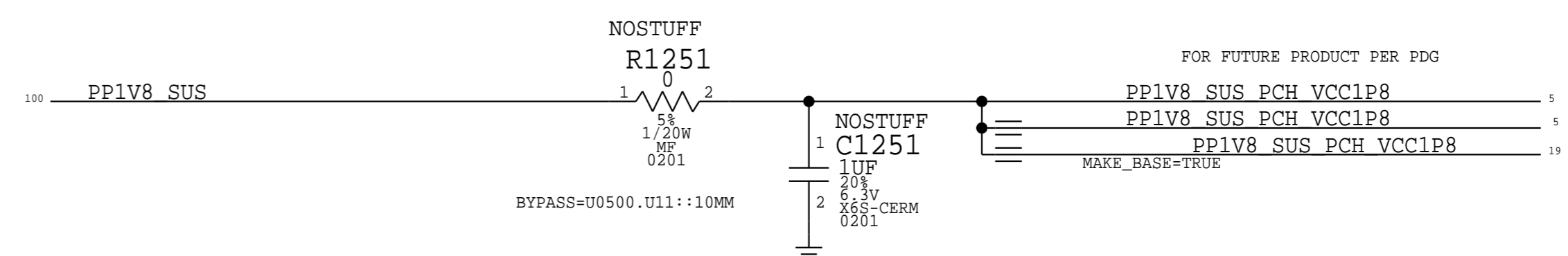
| | | | |
|---|----------------|----------------------|--------|
| SYNC_MASTER=J79_JSHAO | | SYNC_DATE=08/28/2015 | |
| PAGE TITLE CPU Core Decoupling | | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 | STEP D |
| | REVISION | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 111 NOT TO REPRODUCE OR PUBLISH IT IN WHOLE OR PART 112 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 113 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 10 OF 145 | |
| | SHEET | 10 OF 119 | |



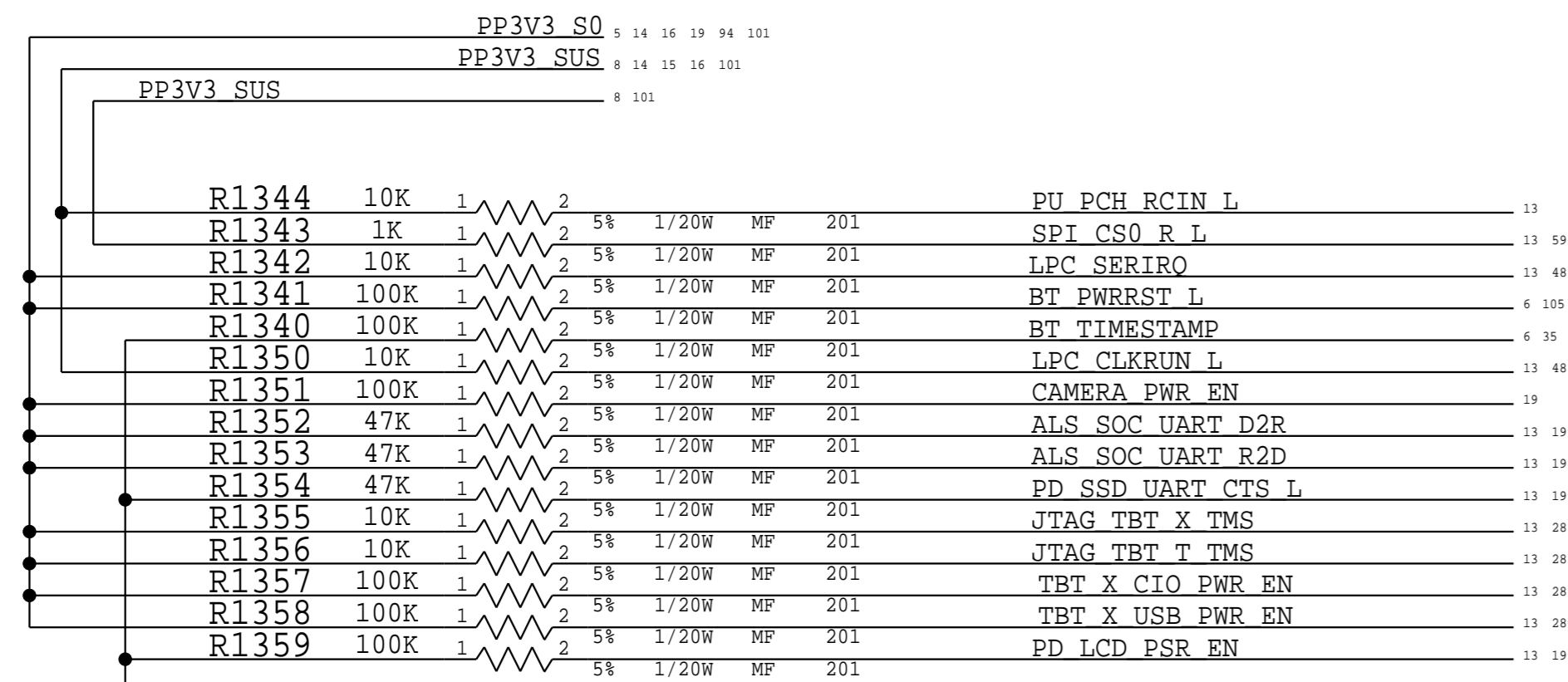
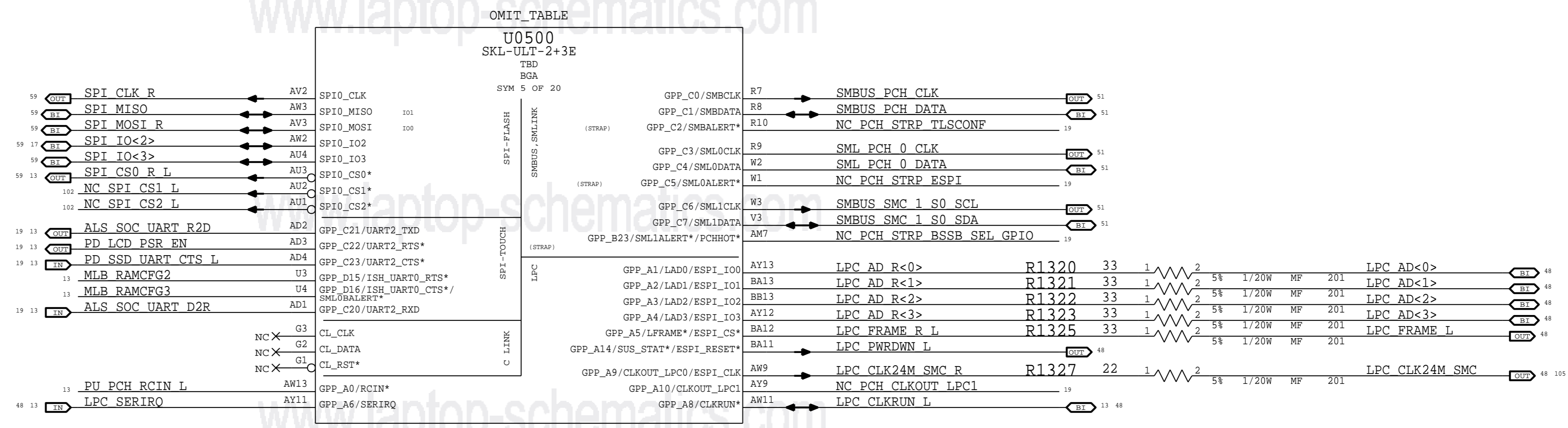
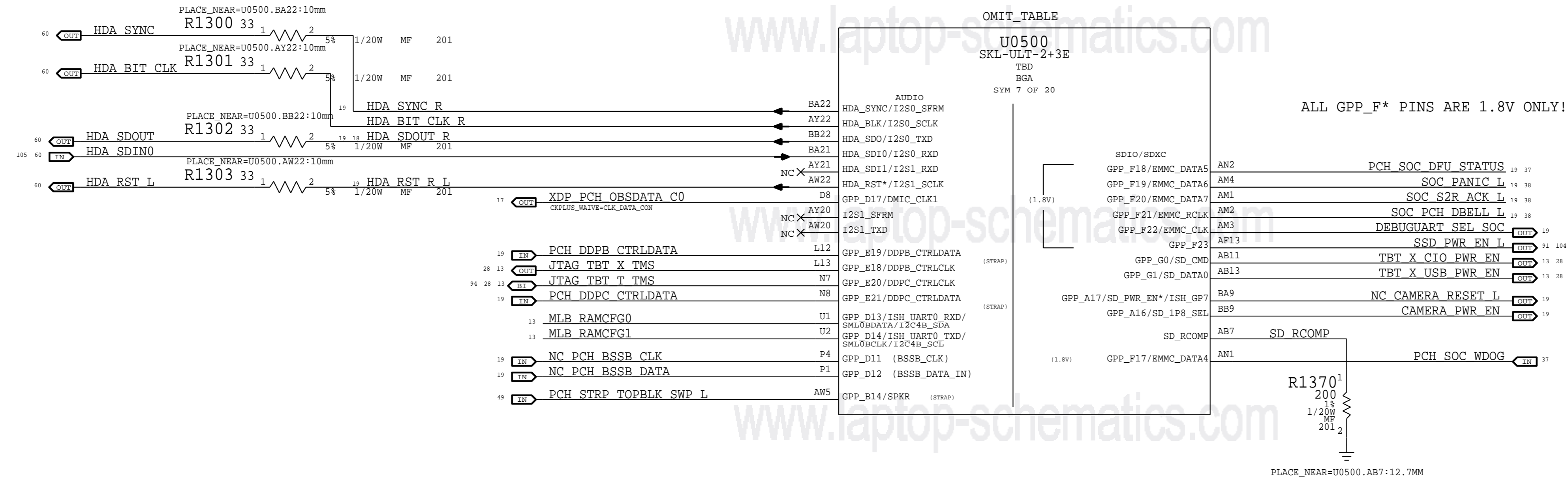
| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=J79_JSHAO | | SYNC_DATE=08/28/2015 | |
| PAGE TITLE | | | |
| CPU GT Decoupling | | | |
| | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 11 OF 145 |
| | | SHEET | 11 OF 119 |



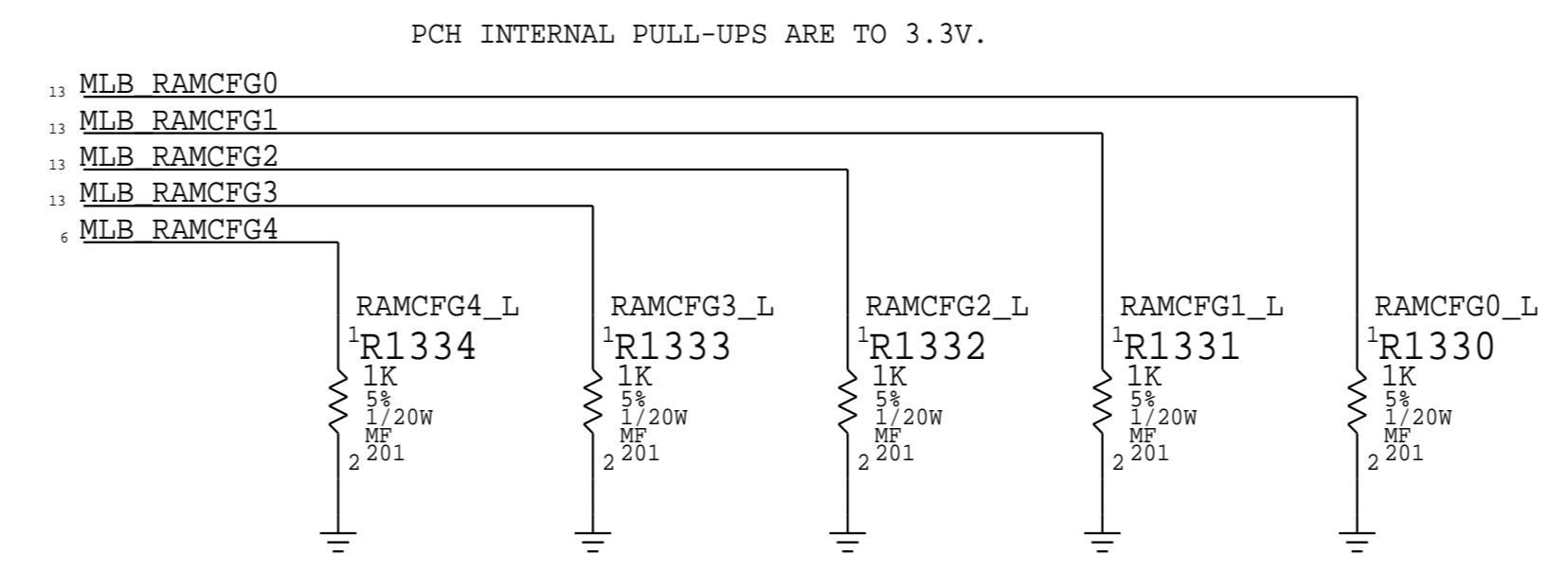
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------------|----------------------------|----------|------------|
| 113S0022 | 4 | RES, MF, 1A MAX, 0OHM, 5%, 0603 | L1250, L1252, L1253, L1254 | | |



| | | | |
|---|--|----------------|--------|
| PAGE TITLE | | PCH Decoupling | |
| DRAWING NUMBER | | 051-00777 | SIZE D |
| REVISION | | 9.0.0 | |
| BRANCH | | dvt-fab09-0 | |
| PAGE | | 12 OF 145 | |
| SHEET | | 12 OF 119 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED | | | |



MEMORY CONFIGURATION STRAPS.

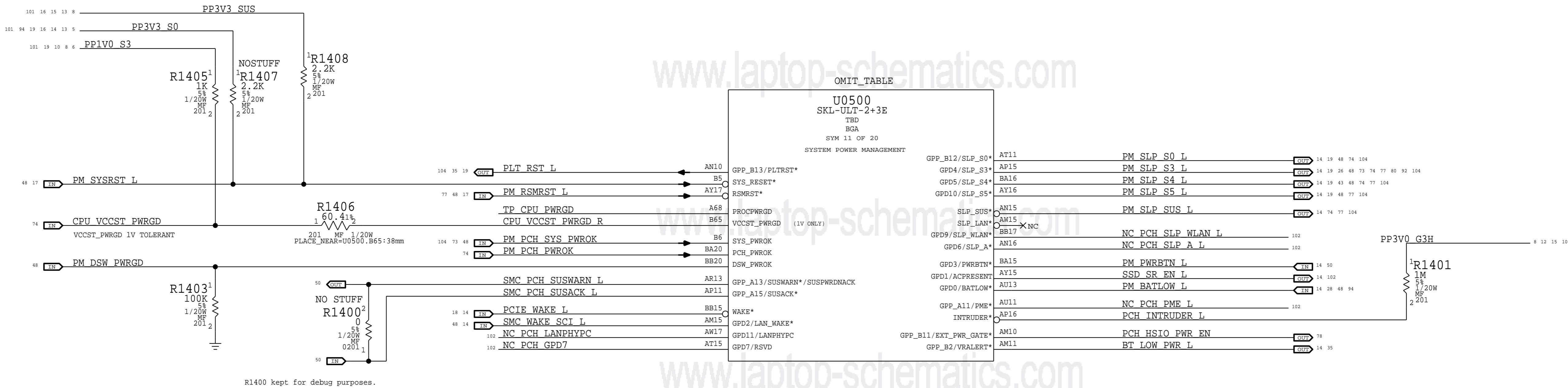


| BOM GROUP | BOM OPTIONS |
|-------------|---|
| RAMCFG_SLOT | RAMCFG4_L, RAMCFG3_L, RAMCFG2_L, RAMCFG1_L, RAMCFG0_L |

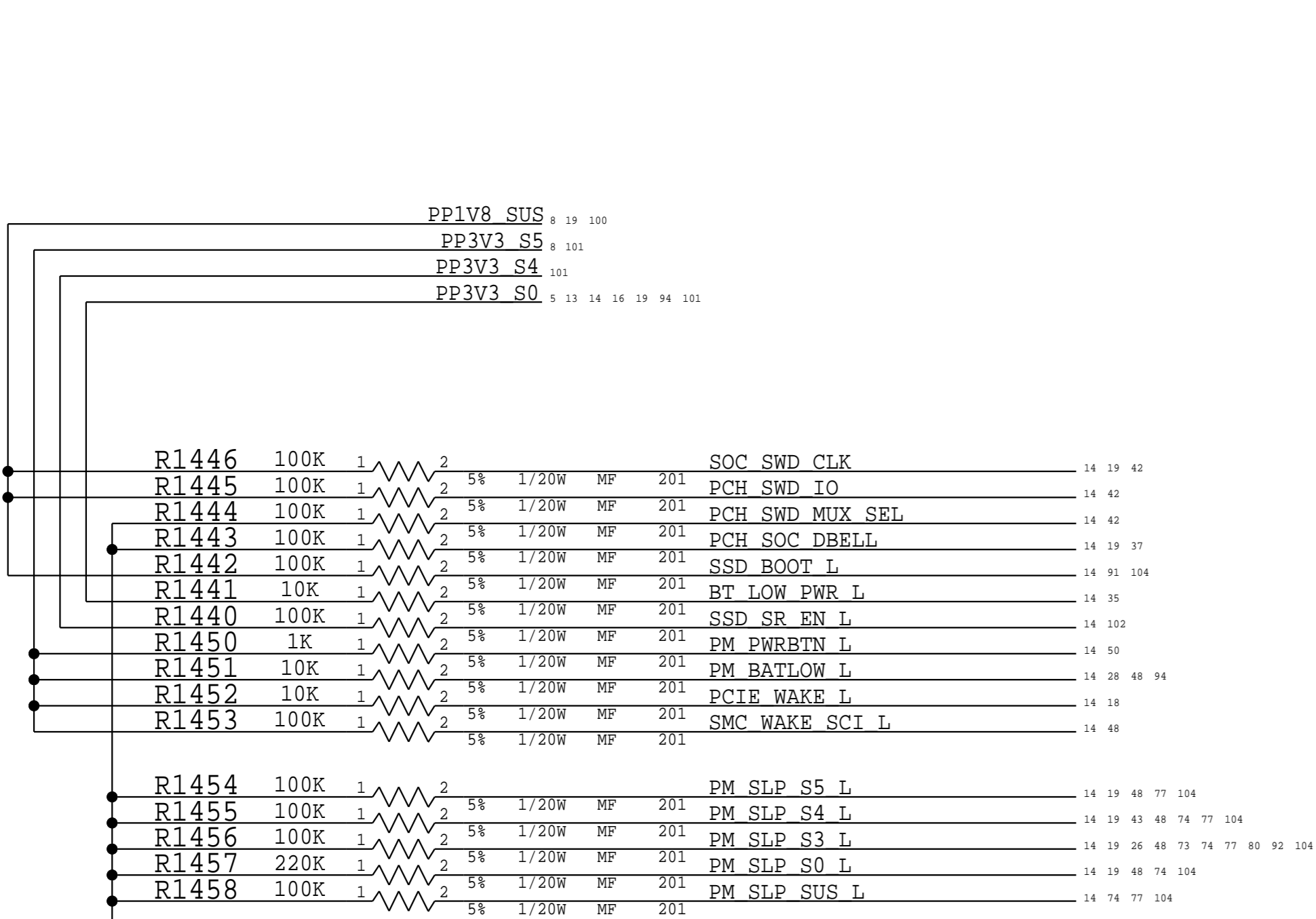
BOM_COST_GROUP=CPU & CHIPSET

| | | | |
|--|--|--------------------------------------|--------------------|
| DESIGN: X502/MLB | | LAST CHANGE: Tue Feb 2 13:18:21 2016 | |
| PAGE TITLE PCH Audio/LPC/SPI/SMBus | | | |
| Apple Inc. | | DRAWING NUMBER 051-00777 | SIZE D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 11V ALL RIGHTS RESERVED | | REVISION 9.0.0 | SHEET 13 OF 119 |
| | | BRANCH dvt-fab09-0 | PAGE 13 OF 145 |

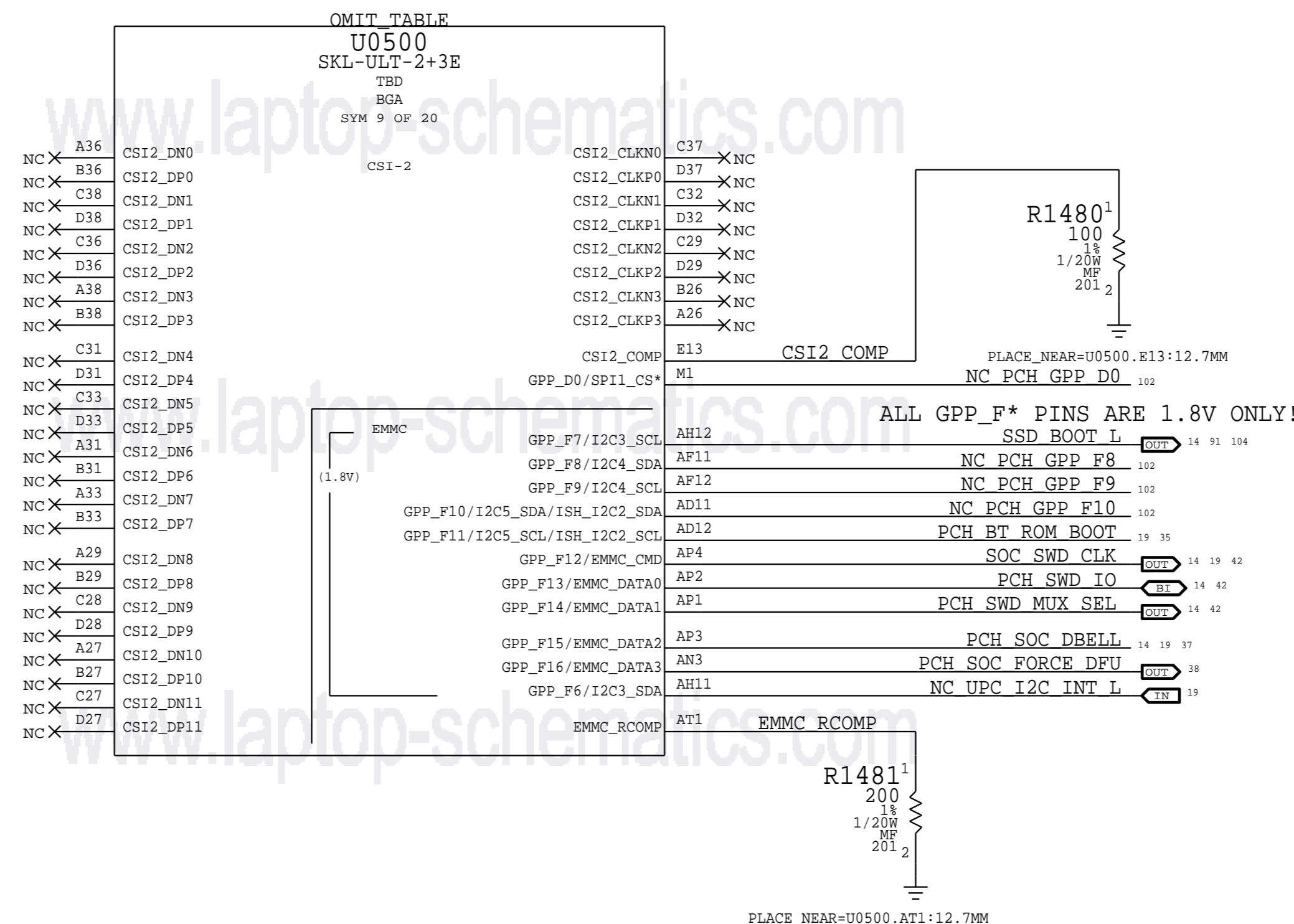
PCH Reset Button



R1400 kept for debug purposes.



NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED. THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE. THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.



DESIGN: X502/MLB
 LAST CHANGE: Tue May 3 17:45:28 2016

PAGE TITLE: PCH Power Management

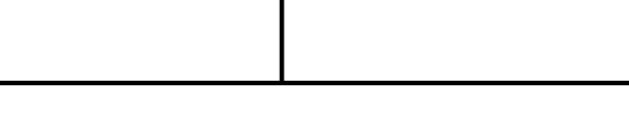
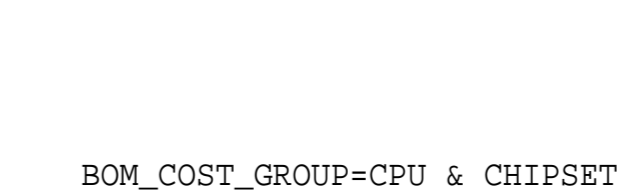
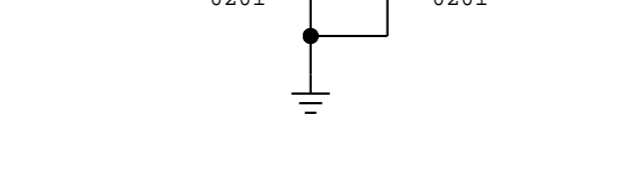
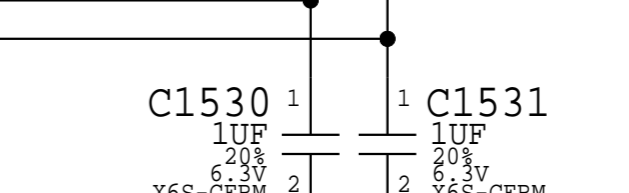
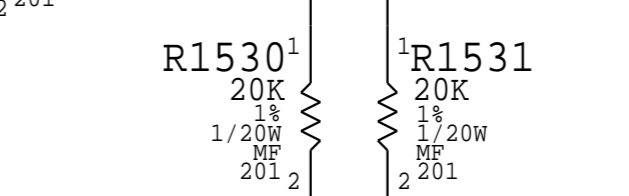
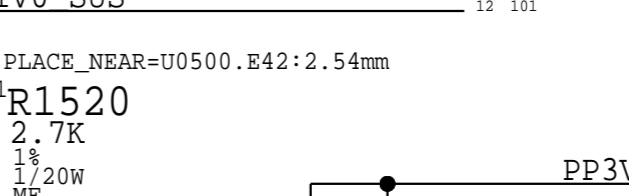
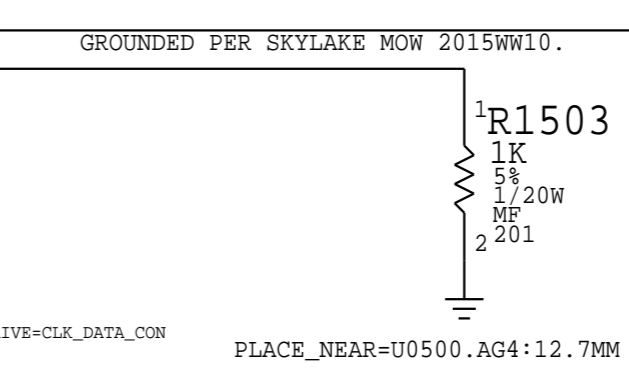
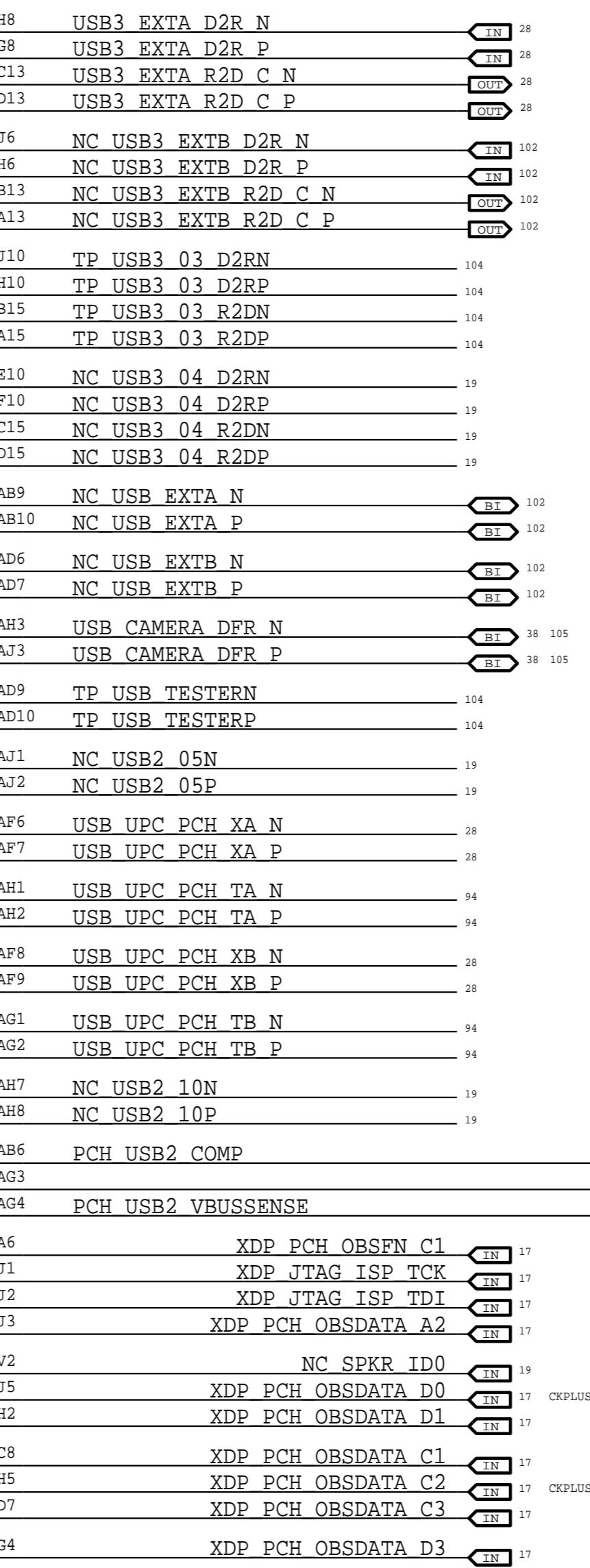
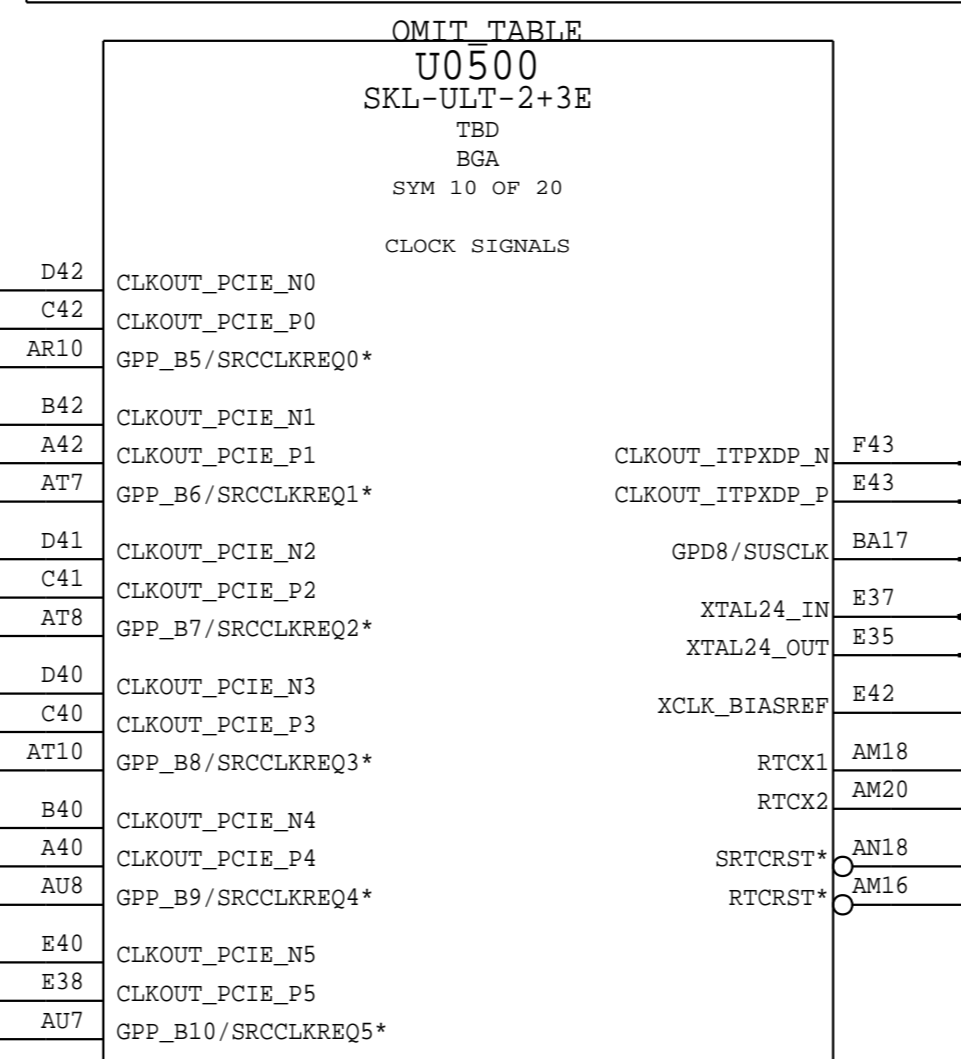
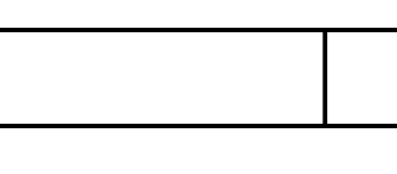
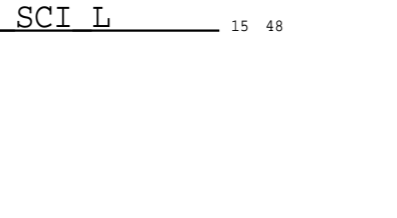
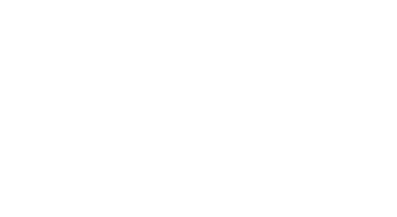
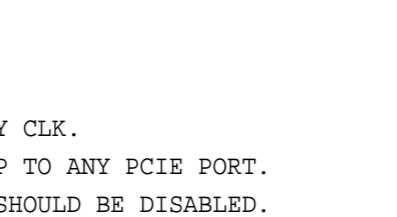
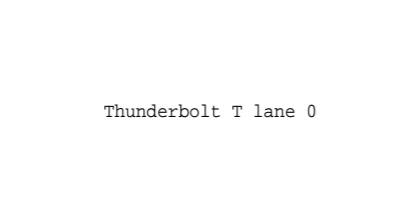
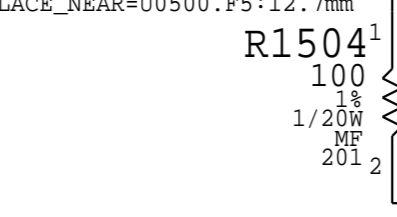
Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 1V ALL RIGHTS RESERVED

| | | | |
|----------------|-----------|--------|-------------|
| DRAWING NUMBER | 051-00777 | SIZE | D |
| REVISION | 9.0.0 | BRANCH | dvt-fab09-0 |
| PAGE | 14 OF 145 | SHEET | 14 OF 119 |

PCIe Port Assignments:

SSD LANE 0
SSD LANE 1
SSD LANE 2
SSD LANE 3
Thunderbolt X lane 0
Thunderbolt X lane 1
Thunderbolt X lane 2
Thunderbolt X lane 3
AirPort
CAMERA
Thunderbolt T lane 0
Thunderbolt T lane 1



DESIGN: X502/MLB
LAST CHANGE: Thu Jun 18 20:05:18 2015

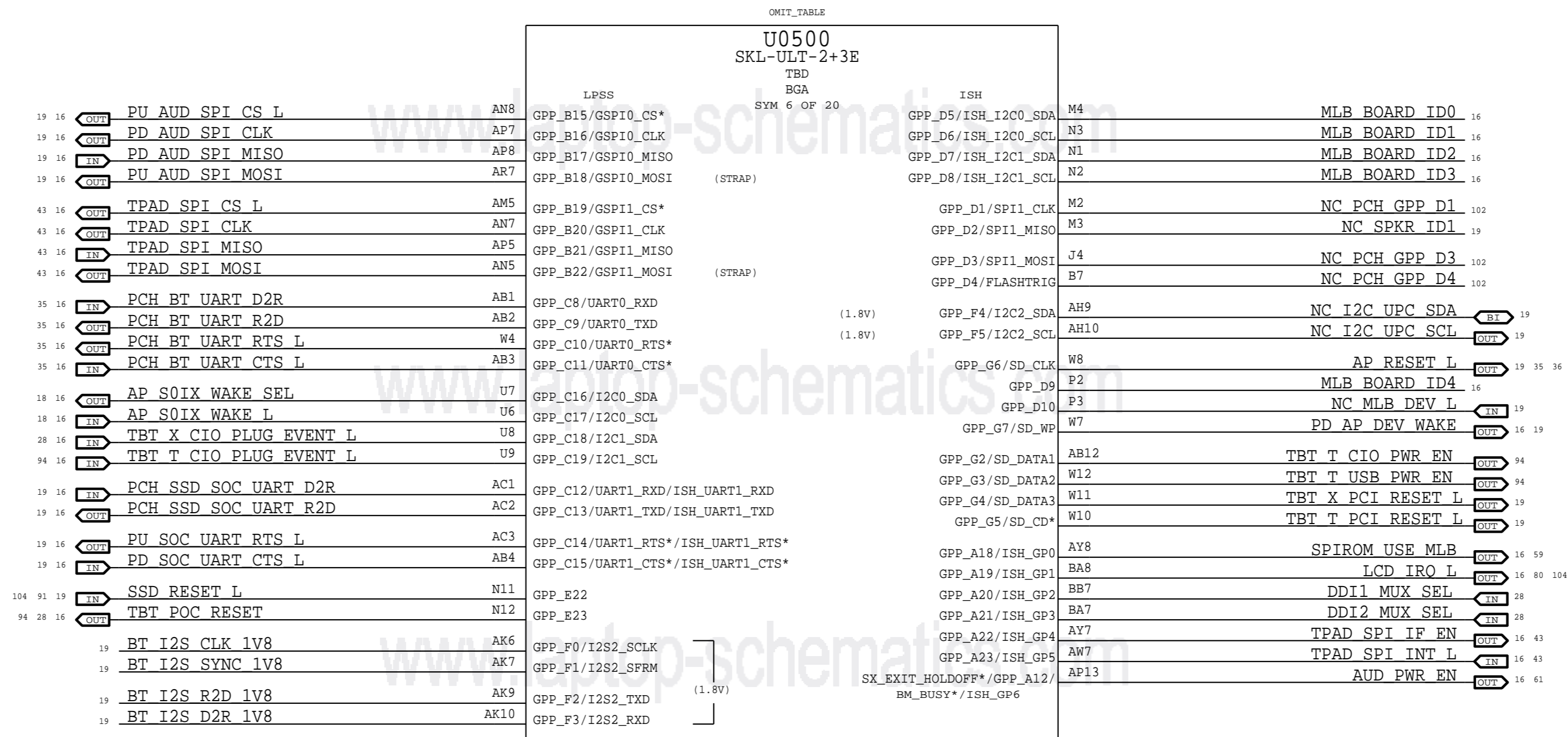
PAGE TITLE
PCH PCIe/USB/CLKS

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
11 ALL RIGHTS RESERVED

| | | | |
|------------------|-----------|------|---|
| BRANCHING NUMBER | 051-00777 | STEP | D |
| REVISION | 9.0.0 | | |
| PAGE | 15 OF 145 | | |
| SHEET | 15 OF 119 | | |

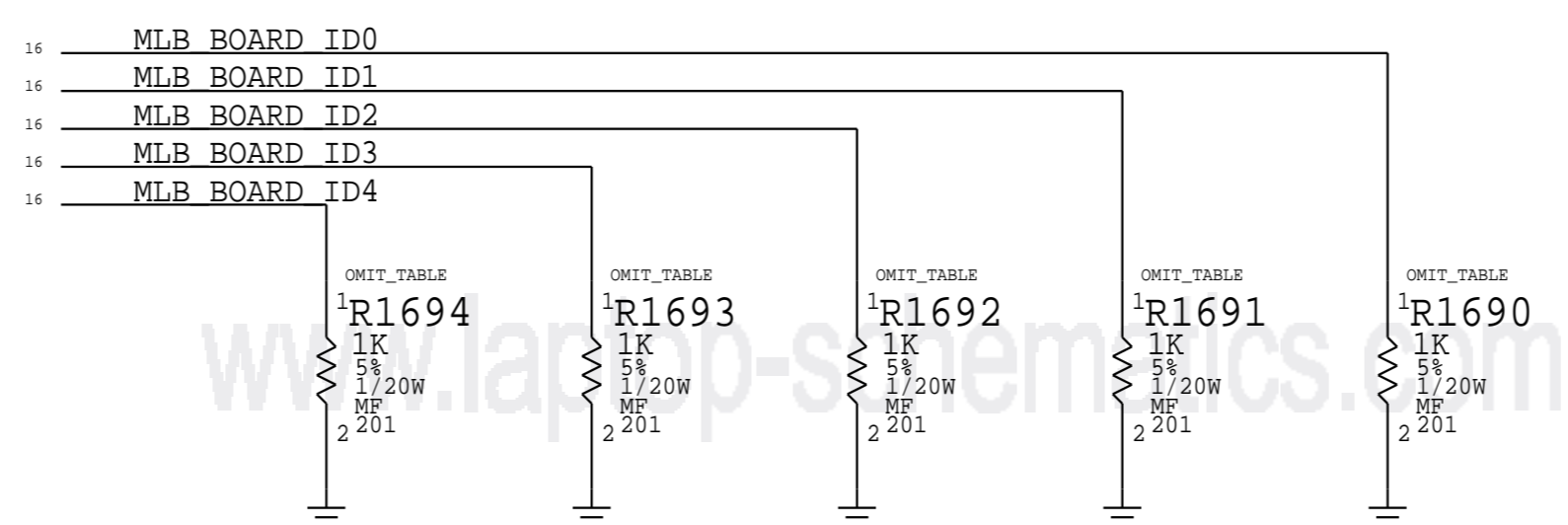
BOM_COST_GROUP=CPU & CHIPSET

ALL GPP_F* PINS ARE 1.8V ONLY!

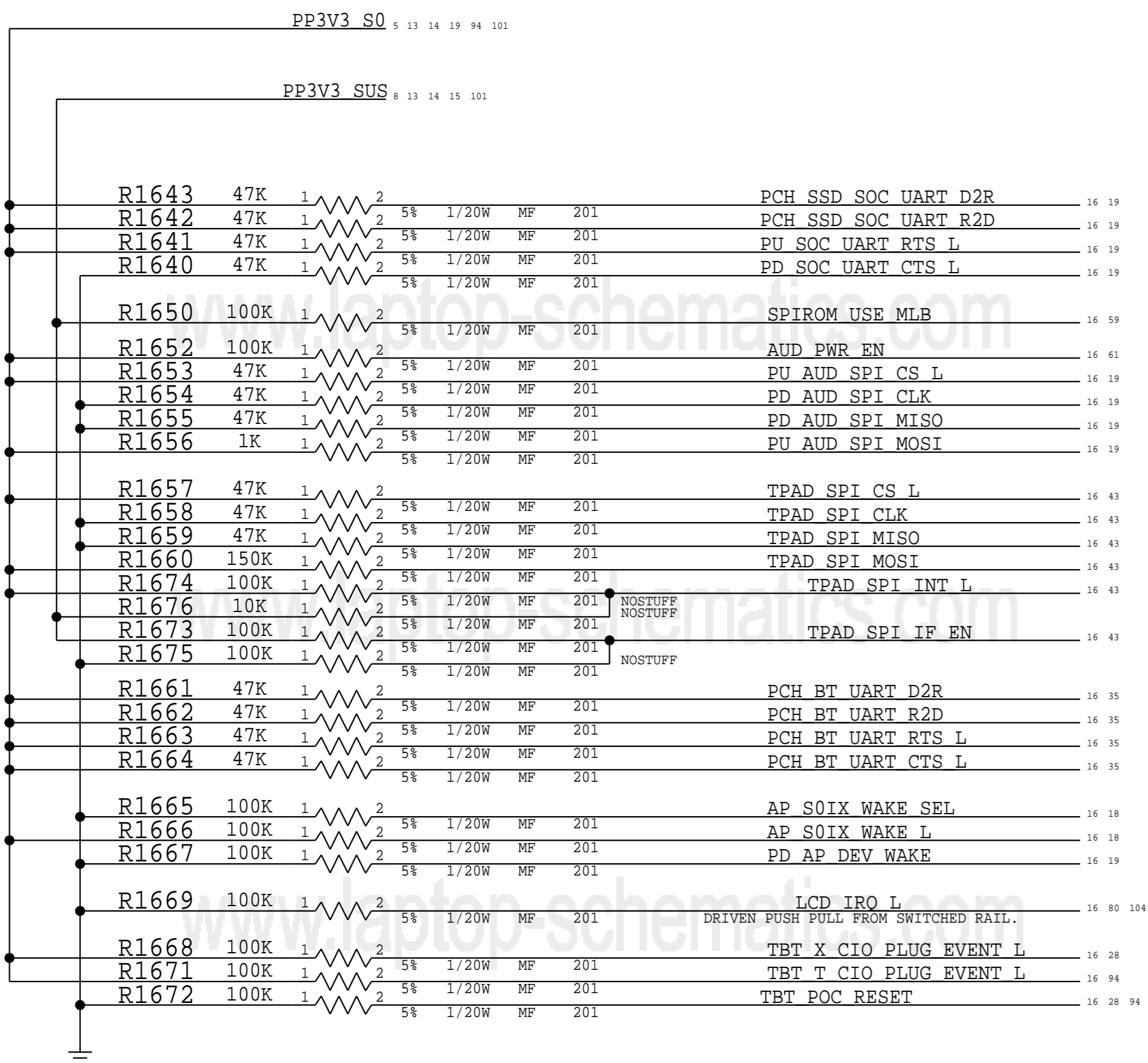


MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION | CODE |
|----------|-----|--------------------------------|-------------------------|-------------|---------|
| 117S0006 | 0 | RES.MF,1/20W/1K OHM,5,0201,SMD | | BOARD_ID:0 | <11111> |
| 117S0006 | 1 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1690 | BOARD_ID:1 | <11110> |
| 117S0006 | 1 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1691 | BOARD_ID:2 | <11101> |
| 117S0006 | 2 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1691,R1690 | BOARD_ID:3 | <11100> |
| 117S0006 | 1 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1692 | BOARD_ID:4 | <11011> |
| 117S0006 | 2 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1692,R1690 | BOARD_ID:5 | <11010> |
| 117S0006 | 2 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1692,R1691 | BOARD_ID:6 | <11001> |
| 117S0006 | 3 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1692,R1691,R1690 | BOARD_ID:7 | <11000> |
| 117S0006 | 1 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1693 | BOARD_ID:8 | <10111> |
| 117S0006 | 2 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1693,R1690 | BOARD_ID:9 | <10110> |
| 117S0006 | 2 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1693,R1691 | BOARD_ID:10 | <10101> |
| 117S0006 | 3 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1693,R1691,R1690 | BOARD_ID:11 | <10100> |
| 117S0006 | 1 | RES.MF,1/20W/1K OHM,5,0201,SMD | R1694 | BOARD_ID:16 | <01111> |



BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
 LAST CHANGE: Wed Oct 28 12:50:22 2015

PAGE TITLE: PCH SPI/UART/GPIO

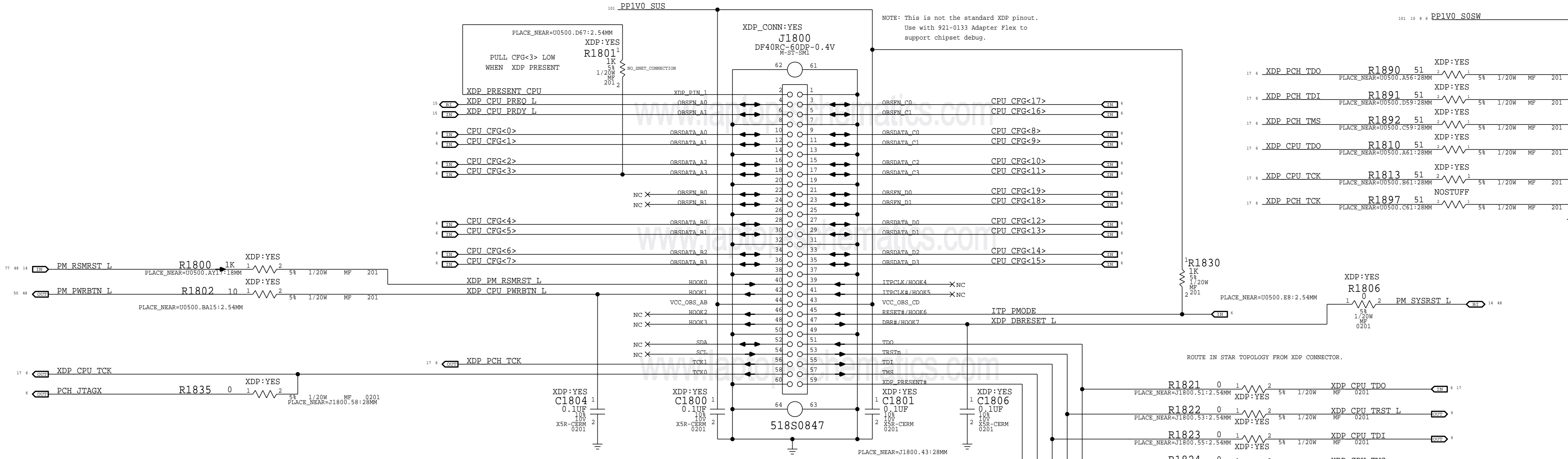
Apple Inc.

DRAWING NUMBER: 051-00777
 REVISION: 9.0.0
 BRANCH: dvt-fab09-0
 PAGE: 16 OF 145
 SHEET: 16 OF 119

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 111 NOT TO REPRODUCE OR COPY IT
 112 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 113 ALL RIGHTS RESERVED

Primary / Merged (CPU/PCH) Micro2-XDP

101 PP1V0 SUS



NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to support chipset debug.

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture. The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation. They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals

Non-XDP Signals

| | | | | |
|--------------------|----------------|--------------------|-------|-----|
| XDP JTAG ISP TCK | MAKE_BASE=TRUE | XDP JTAG ISP TCK | IN | 105 |
| XDP JTAG ISP TDI | MAKE_BASE=TRUE | XDP JTAG ISP TDI | IN | 105 |
| XDP_PCH_OBSDATA_A2 | | TP1870 | TP-P6 | |
| XDP_PCH_OBSDATA_A3 | | TP1871 | TP-P6 | |
| XDP_PCH_OBSDATA_B0 | | TP1872 | TP-P6 | |
| XDP_PCH_OBSDATA_C0 | | TP1873 | TP-P6 | |
| XDP_PCH_OBSDATA_C1 | | TP1874 | TP-P6 | |
| XDP_PCH_OBSDATA_C2 | | TP1875 | TP-P6 | |
| XDP_PCH_OBSDATA_C3 | | TP1876 | TP-P6 | |
| XDP_PCH_OBSDATA_D0 | | TP1877 | TP-P6 | |
| XDP_PCH_OBSDATA_D1 | | TP1878 | TP-P6 | |
| XDP_PCH_OBSDATA_D2 | | TP1879 | TP-P6 | |
| XDP_PCH_OBSDATA_D3 | | TP1880 | TP-P6 | |
| XDP_PCH_OBSFN_C1 | | TP1881 | TP-P6 | |
| XDP_USB_EXT_A_OC_L | MAKE_BASE=TRUE | XDP_USB_EXT_A_OC_L | IN | 105 |
| XDP_USB_EXT_B_OC_L | MAKE_BASE=TRUE | XDP_USB_EXT_B_OC_L | IN | 105 |
| XDP_USB_EXT_C_OC_L | MAKE_BASE=TRUE | XDP_USB_EXT_C_OC_L | IN | 105 |
| XDP_USB_EXT_D_OC_L | MAKE_BASE=TRUE | XDP_USB_EXT_D_OC_L | IN | 105 |

Unused GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

DESIGN: X502/MLB
LAST CHANGE: Thu Oct 22 19:53:09 2015

CPU/PCH Merged XDP



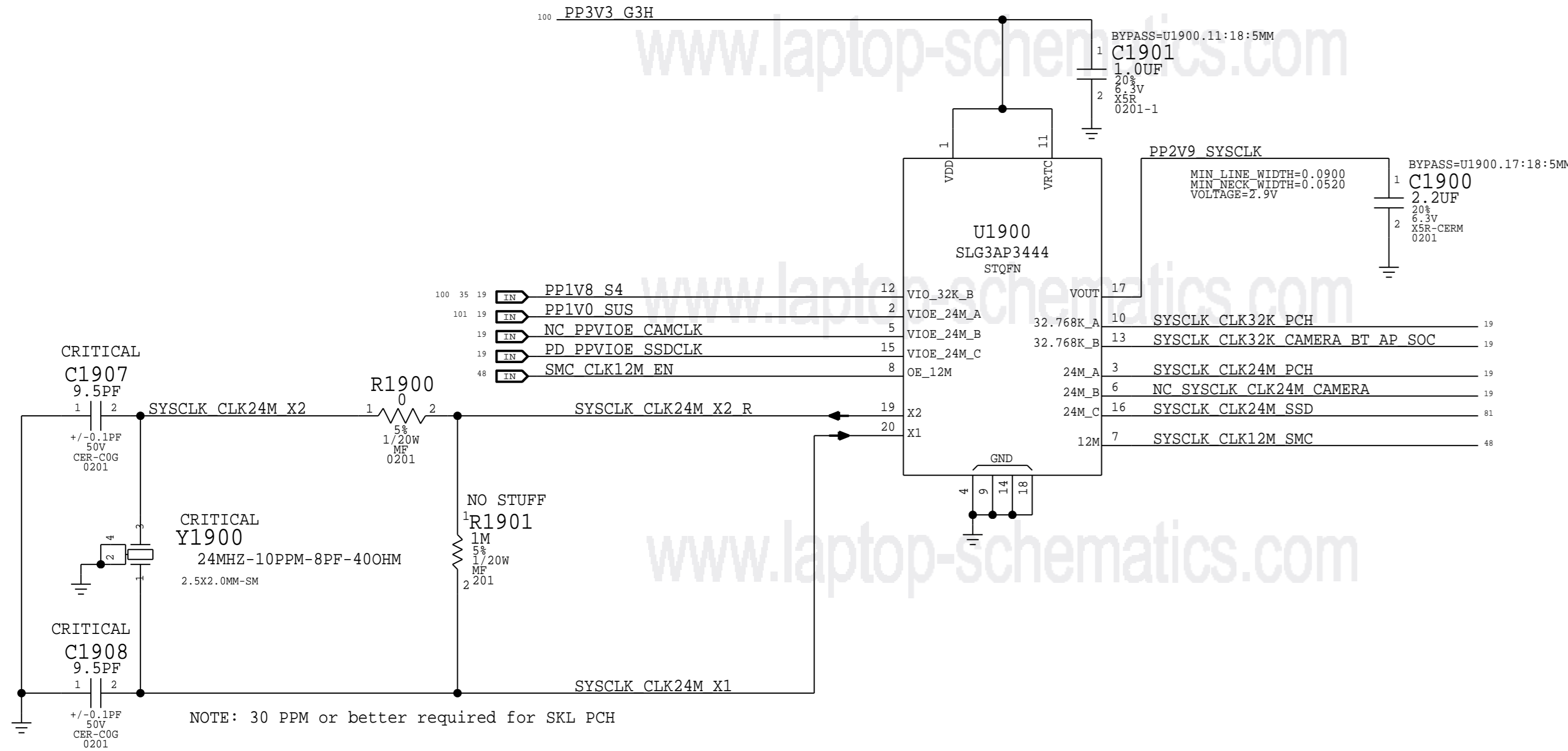
Apple Inc.

| | | | |
|----------------|-------------|------|---|
| DRAWING NUMBER | 051-00777 | STEP | D |
| REVISION | 9.0.0 | | |
| BRANCH | dvt-fab09-0 | | |
| PAGE | 18 OF 145 | | |
| SHEET | 17 OF 119 | | |

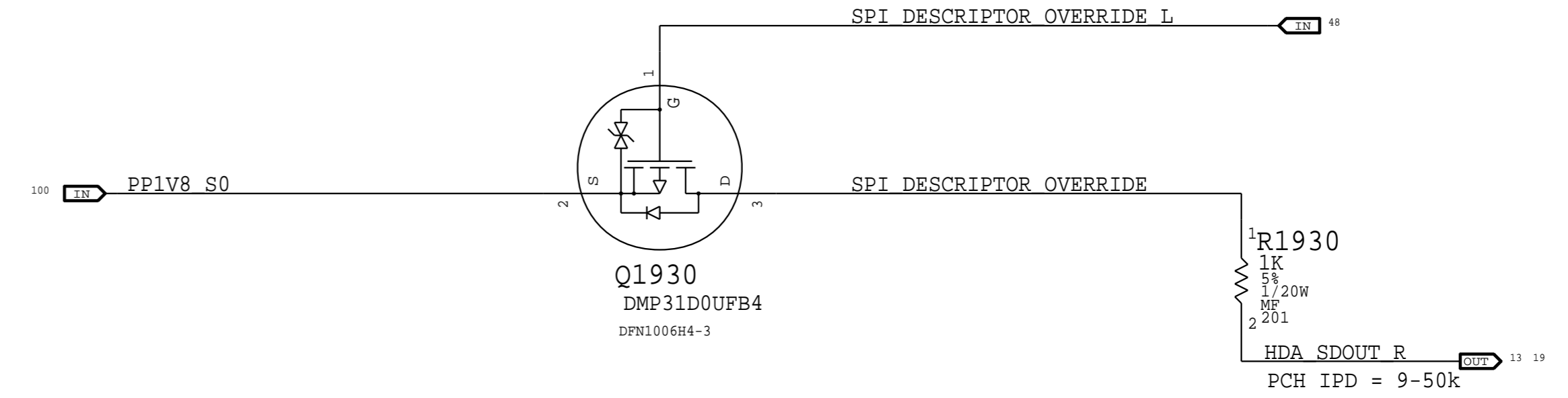
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1111 ALL RIGHTS RESERVED

BOM_COST_GROUP=DEBUG

System 32kHz / 12MHz / 24MHz Clock Generator

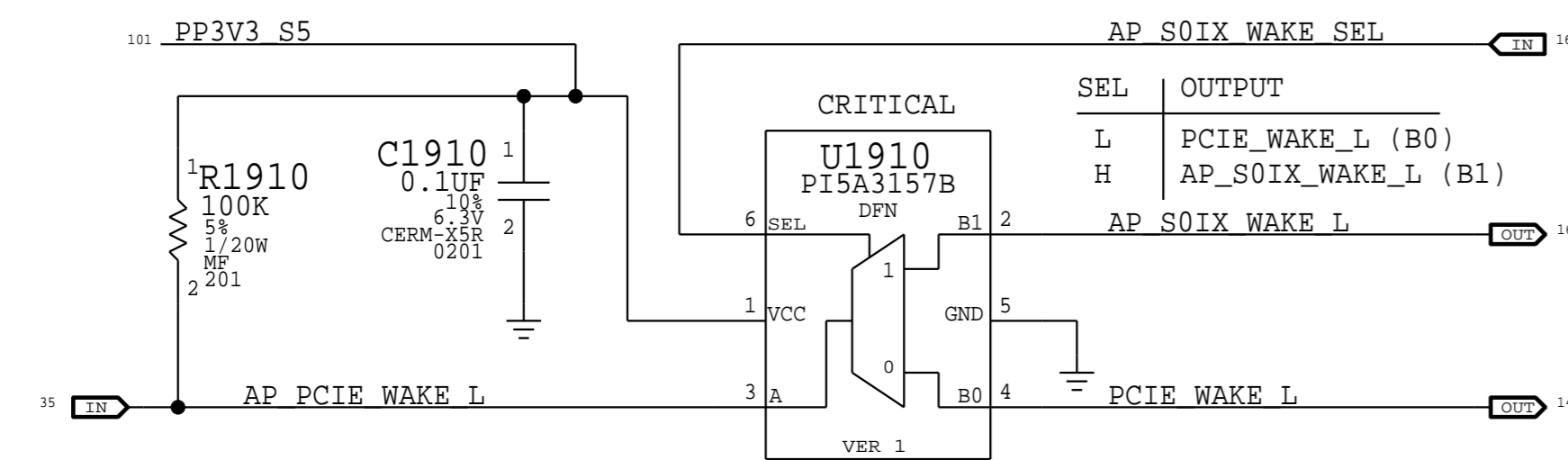


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. ***** Circuit does not support HDA voltage >3.3V.

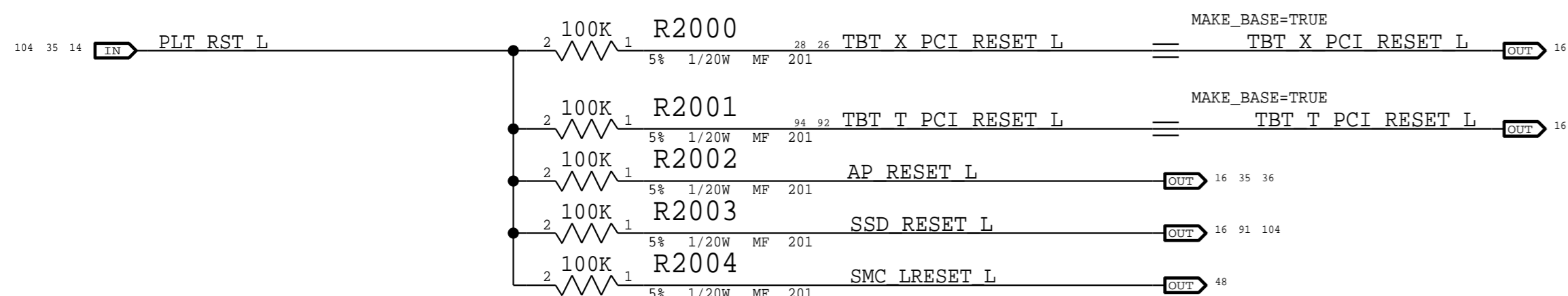
PCIe Wake Muxing



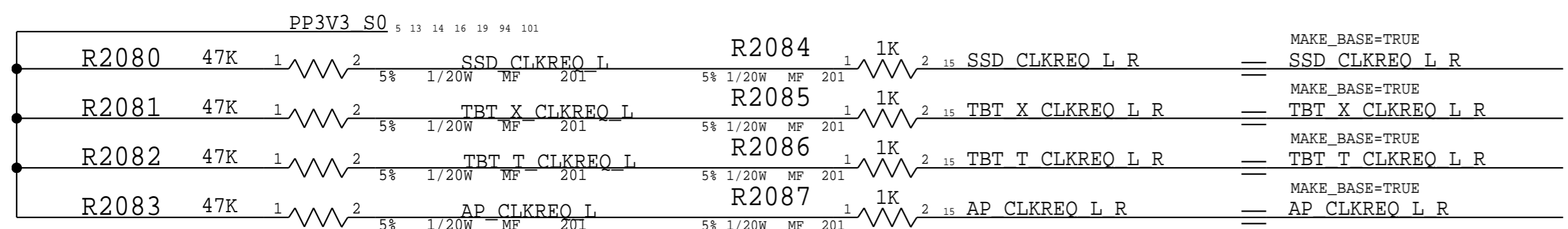
| | | | |
|--|----------------|-------------------|-------------|
| PAGE TITLE | | Chipset Support 1 | |
| Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 19 OF 145 |
| | | SHEET | 18 OF 119 |

Platform Reset Connections

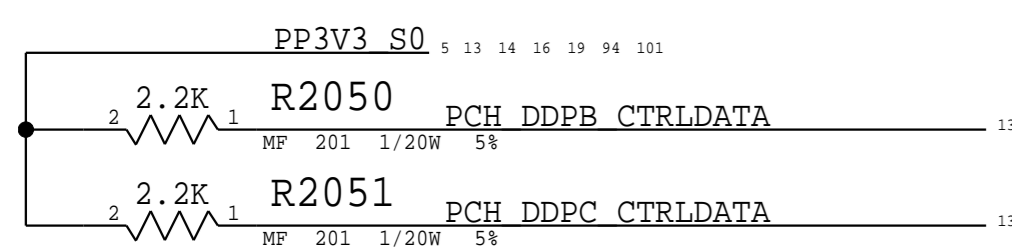
Unbuffered



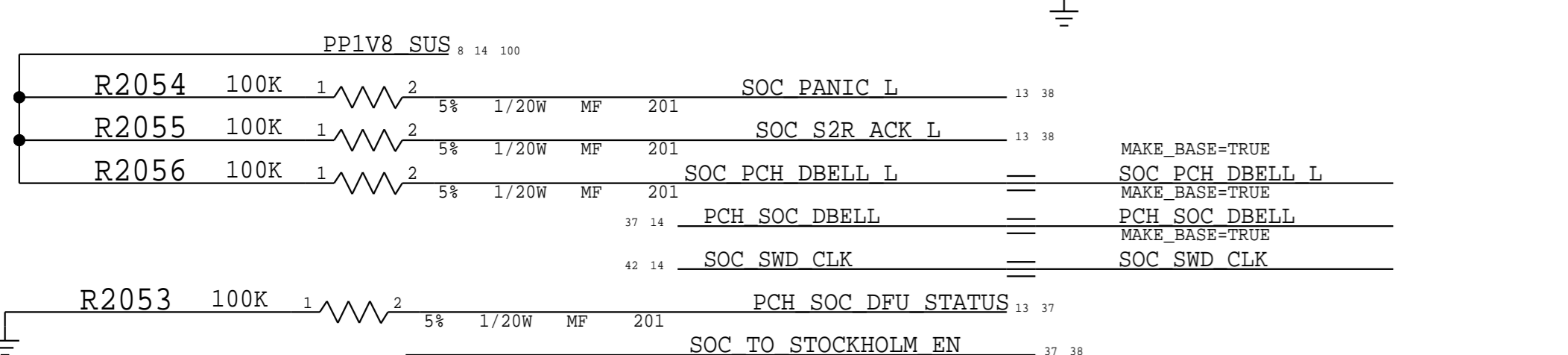
PCIE CLKREQS



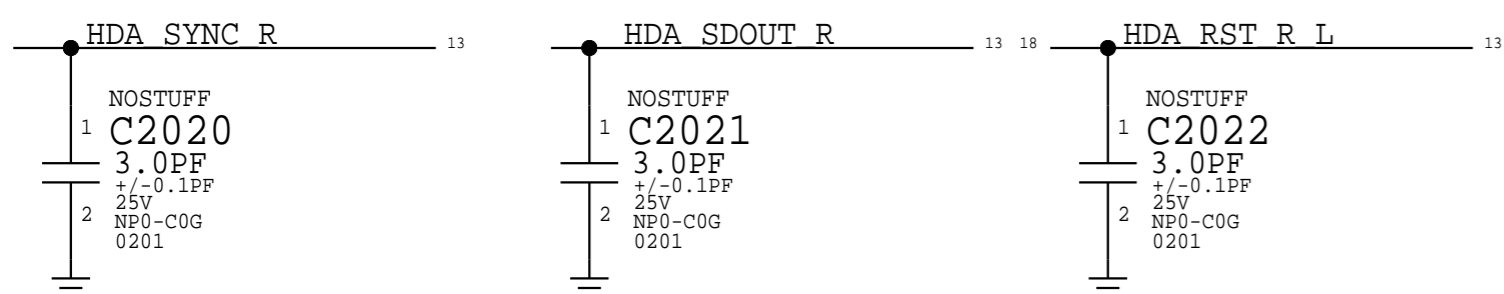
ENABLE DDPB DDPD INTERFACES



T208 PCH GPIO PUs/PDs & ALIASES

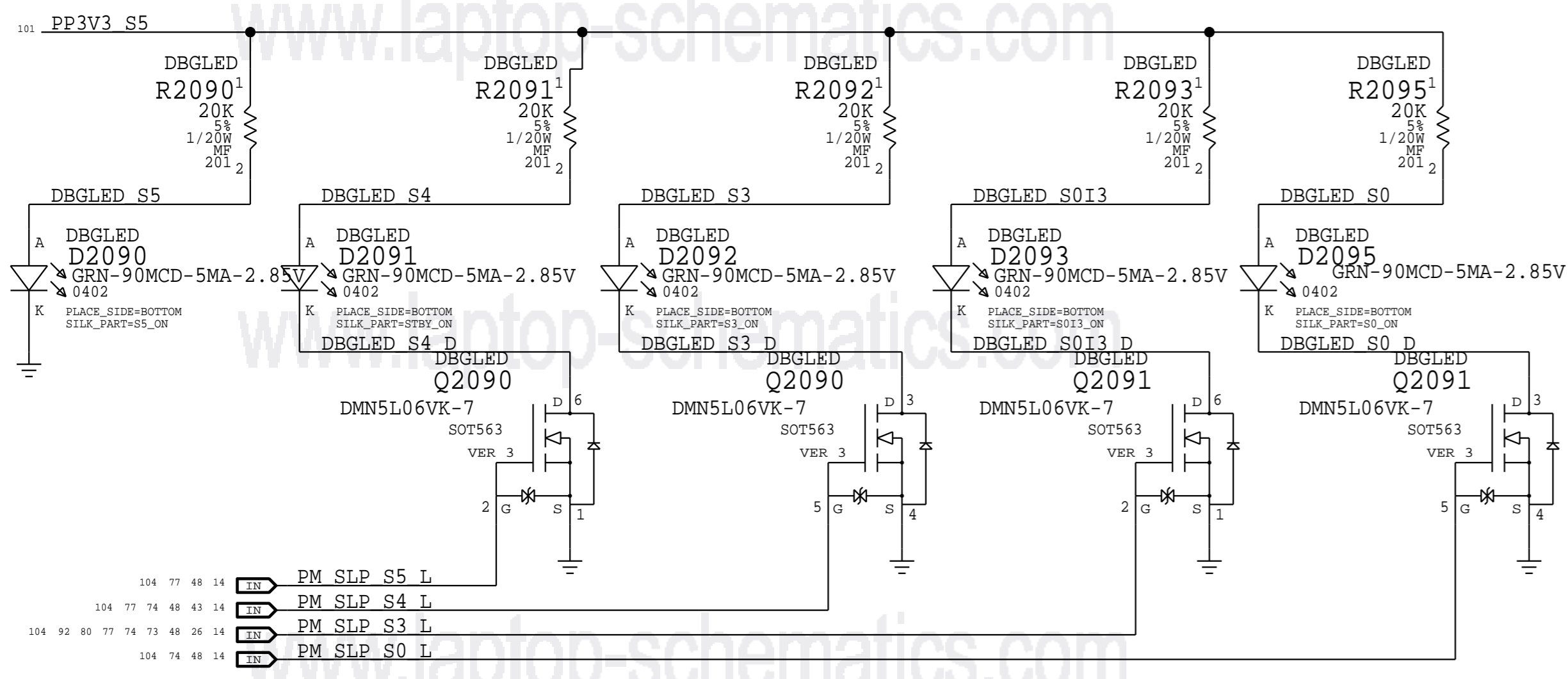


Desense Decoupling Caps on HDA Lines

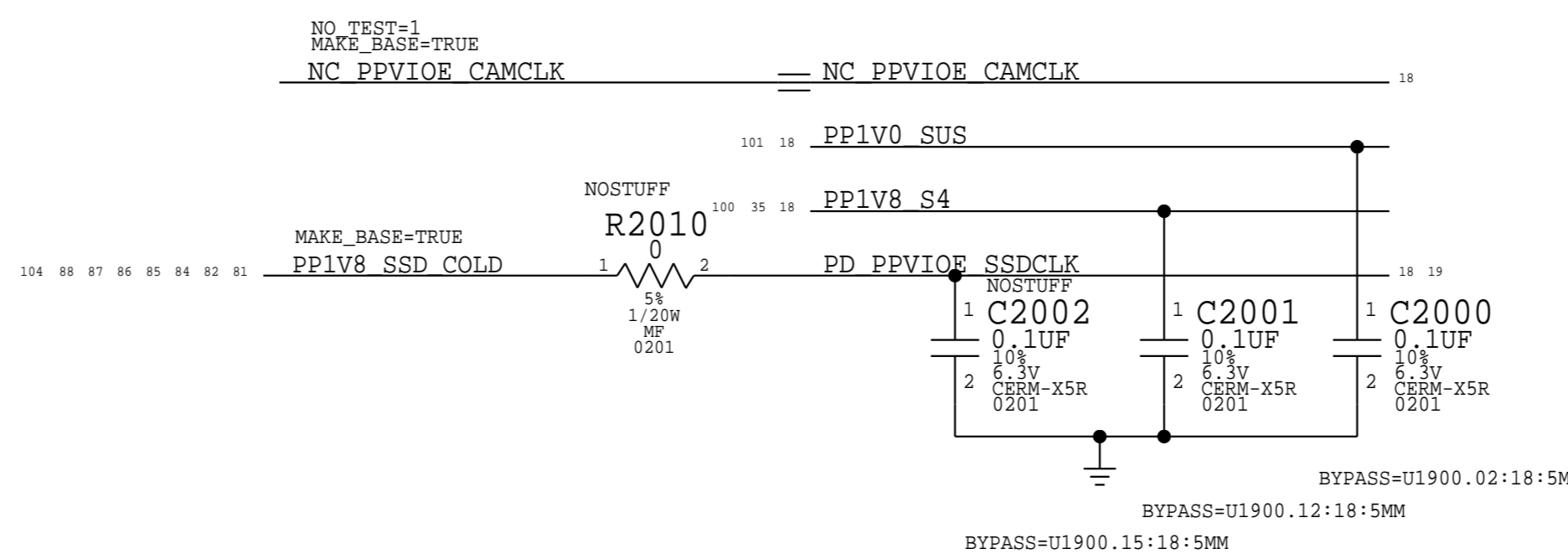


Power State Debug LEDs

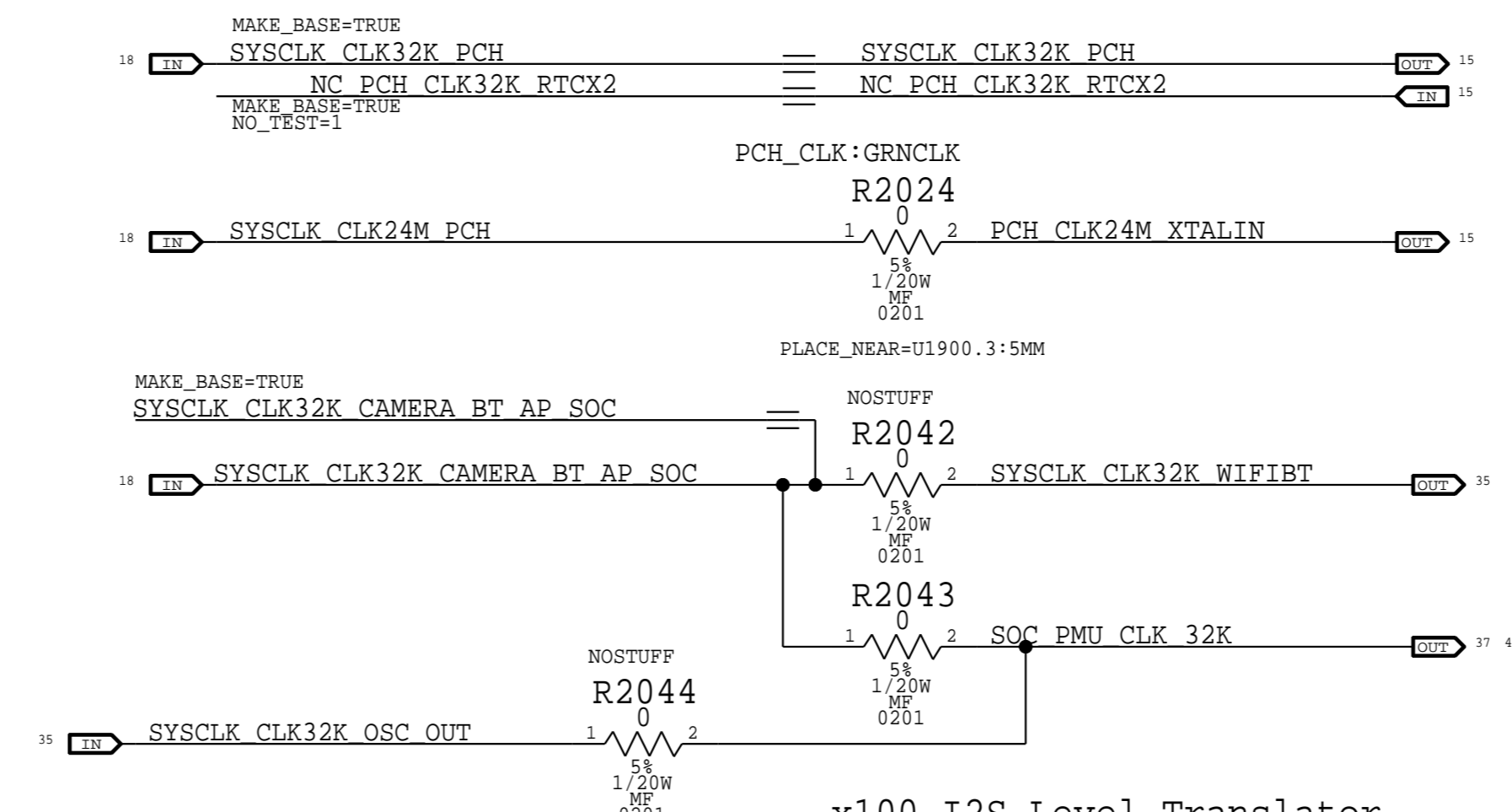
(For development only)



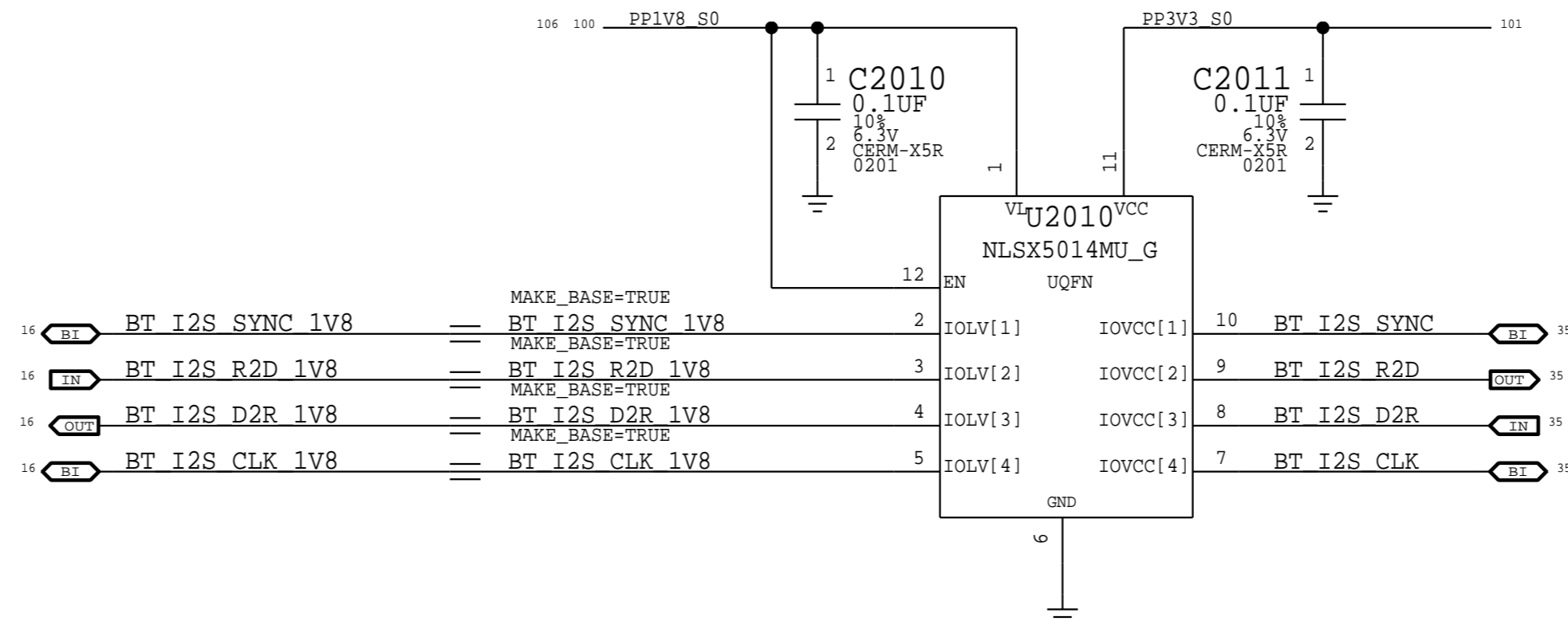
GREENCLK VIOEs



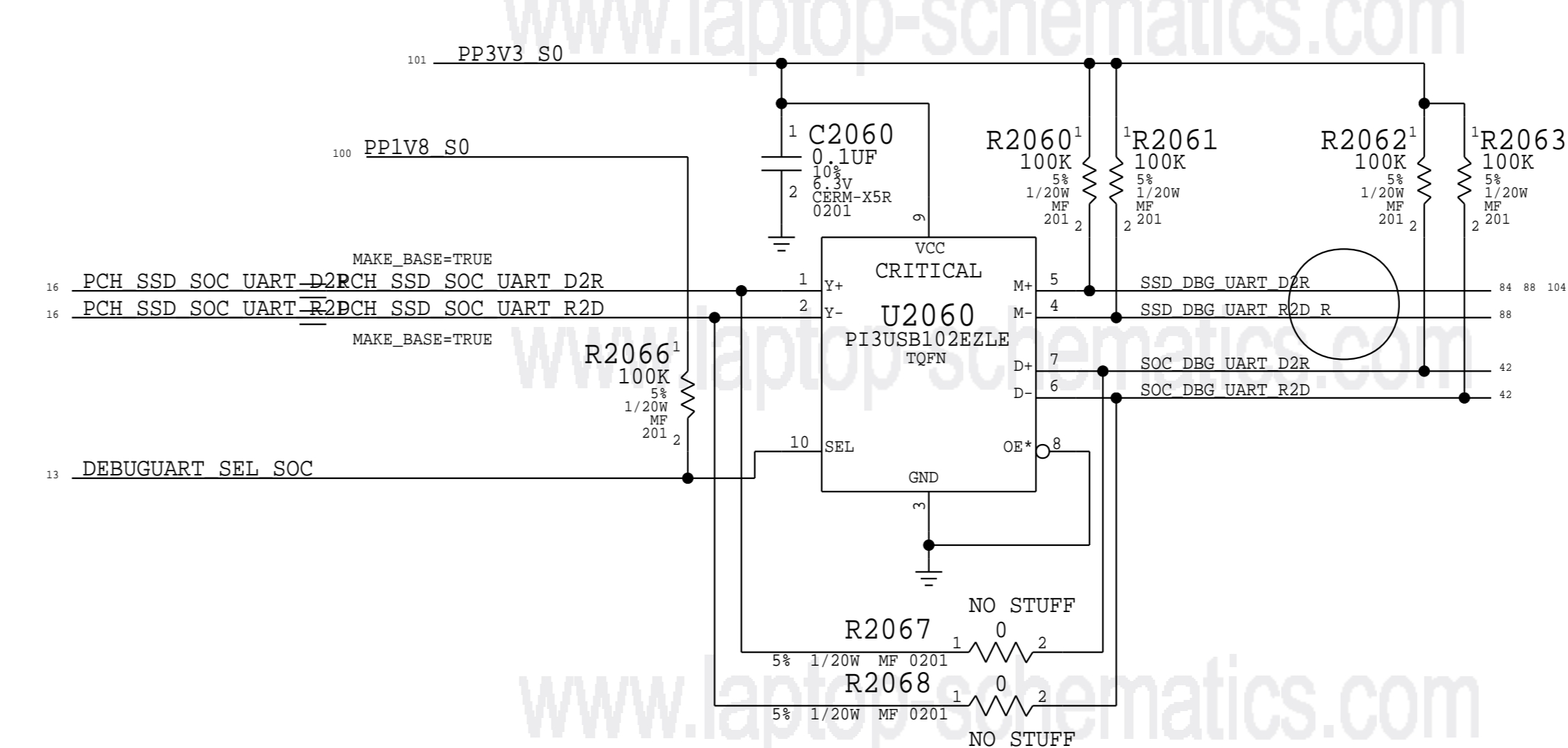
GREENCLK CLOCK OUT ALIASES



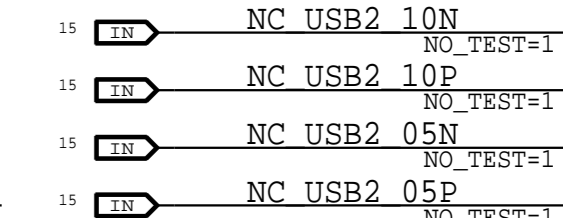
x100 I2S Level Translator



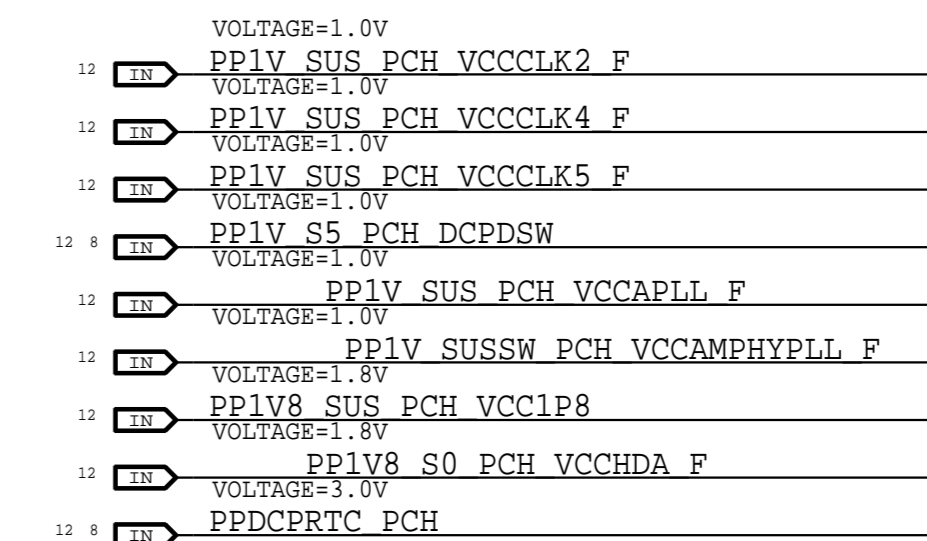
BT/SSD DEBUG UART MUX



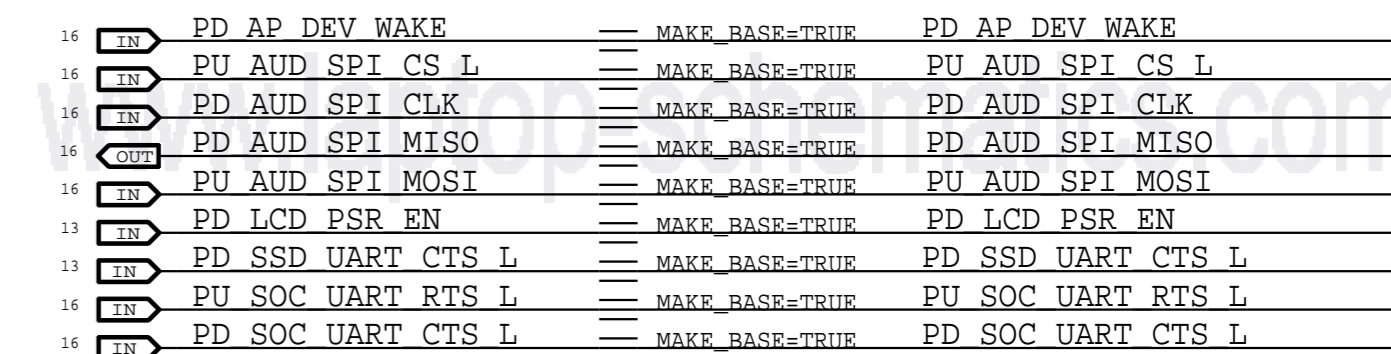
NO TEST



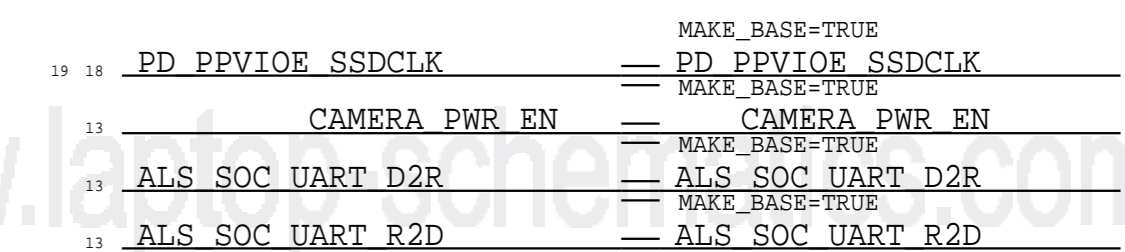
Voltage Props



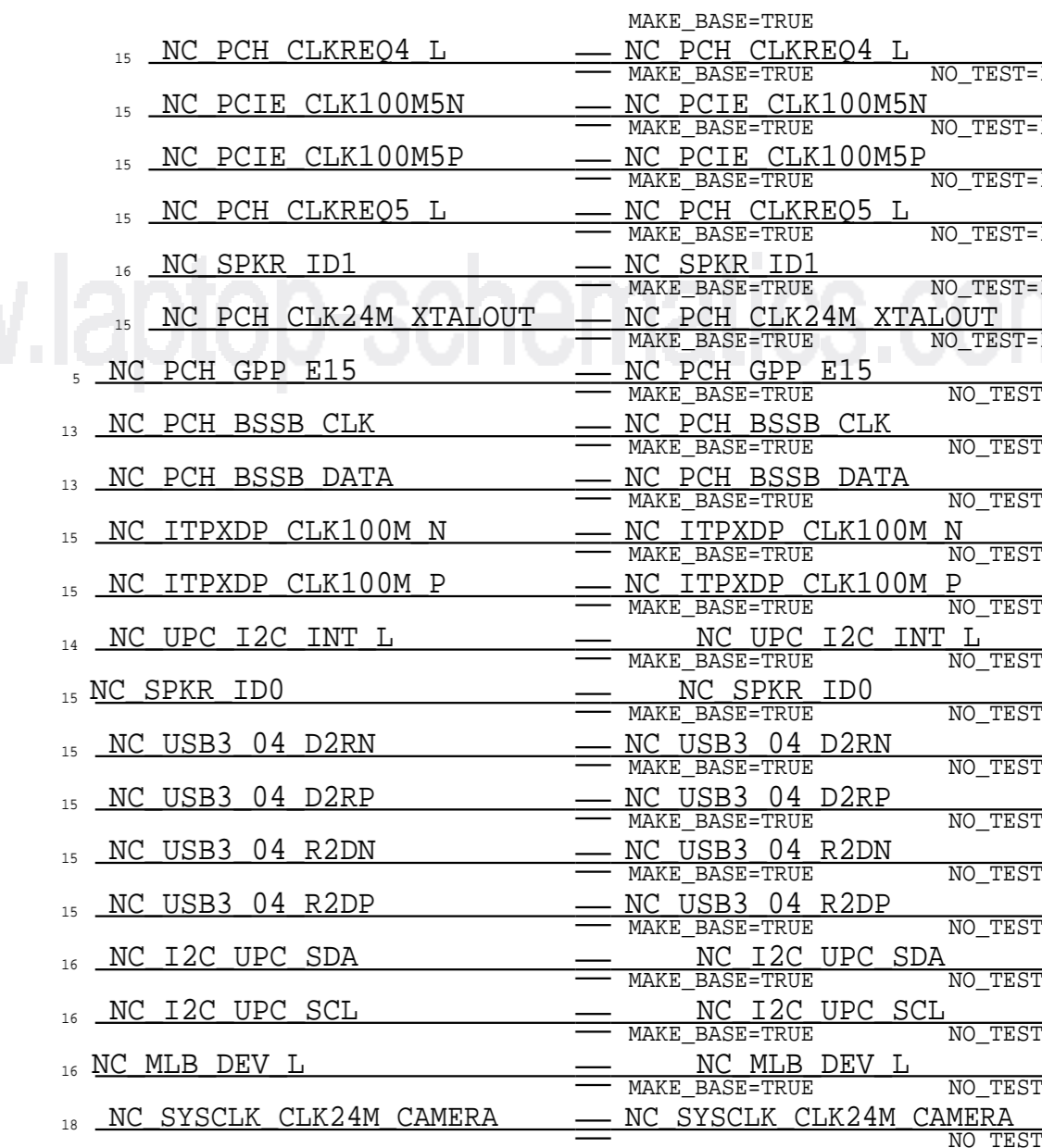
Unused GPIOs with PUs/PDs



SIGNAL ALIASES



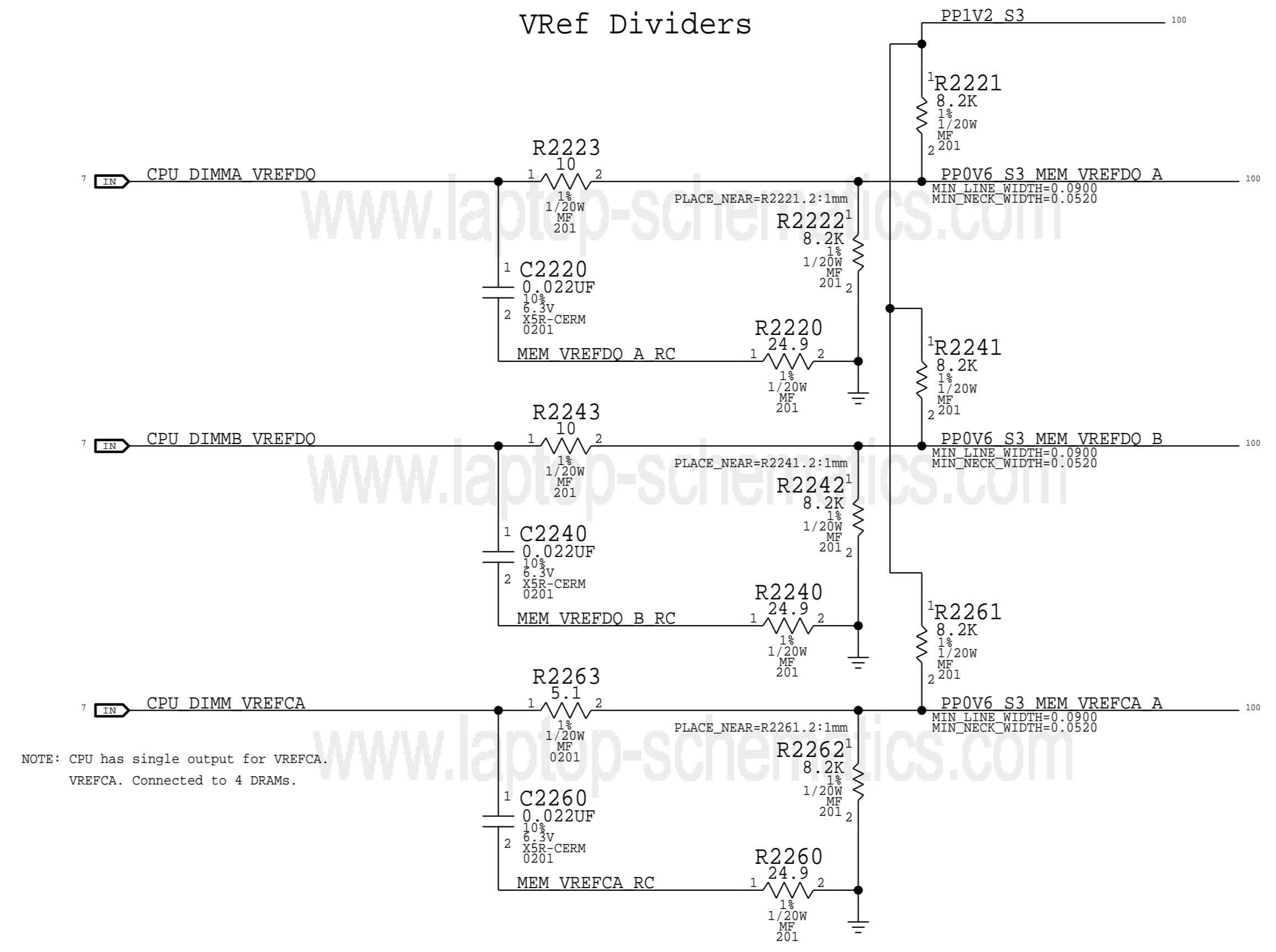
NC SIGNAL ALIASES



| | |
|-------------------|-------------|
| PAGE TITLE | |
| Chipset Support 2 | |
| Apple Inc. | |
| DRAWING NUMBER | 051-00777 |
| REVISION | 9.0.0 |
| BRANCH | dvt-fab09-0 |
| PAGE | 20 OF 145 |
| SHEET | 19 OF 119 |

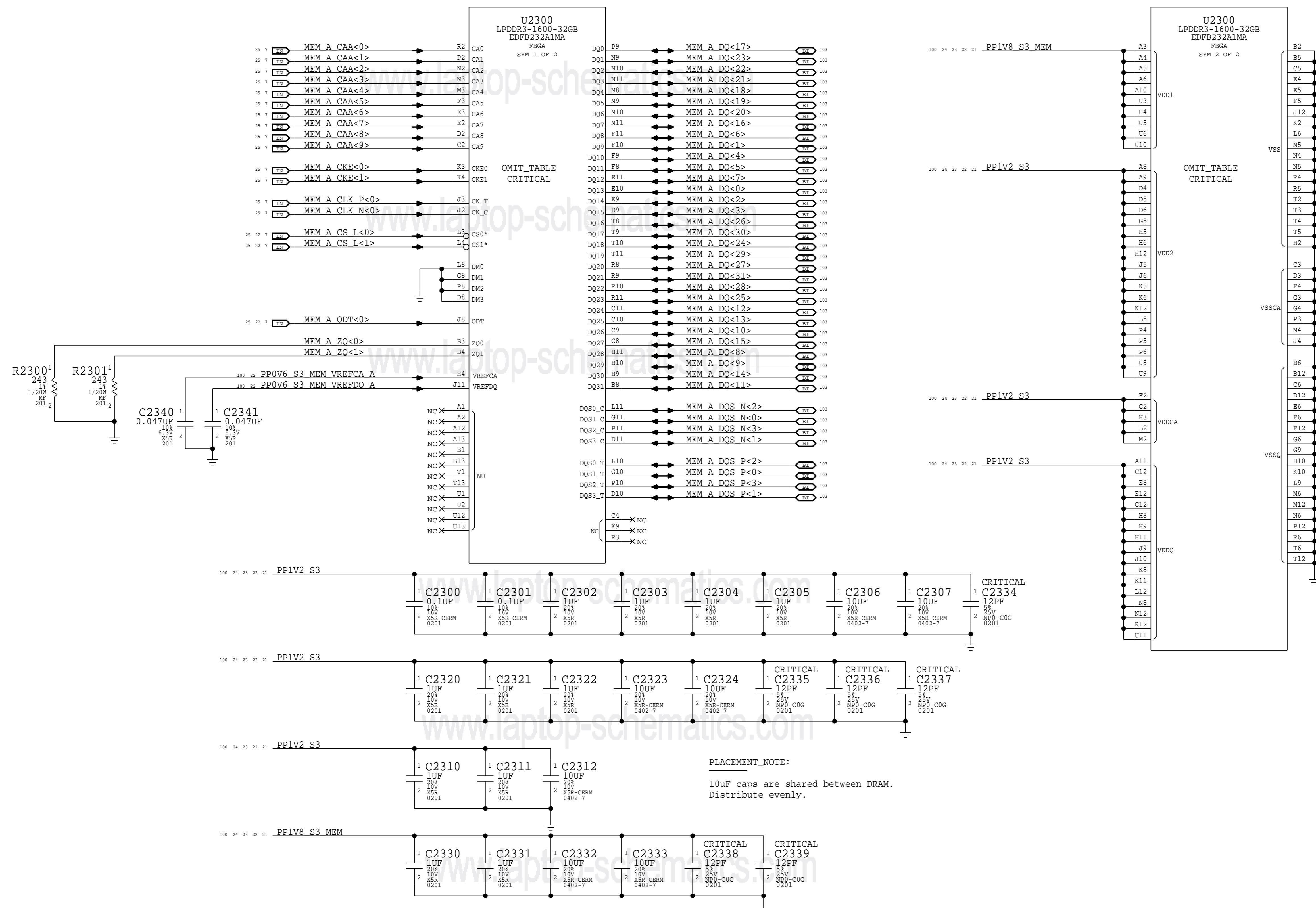
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY INFORMATION OF APPLE INC. THE POSSESSOR AGREES TO THE I TO THIENHUONG NGUYEN DOCUMENT IN CONFIDENCE I I NOT TO REPRODUCE OR COPY IT I I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I I ALL RIGHTS RESERVED

CPU-Based Margining



| | | | |
|---|----------------|------------------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 VREF Margining | | | |
| | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 22 OF 145 |
| | | SHEET | 20 OF 119 |
| | | BOM_COST_GROUP=CPU & CHIPSET | |

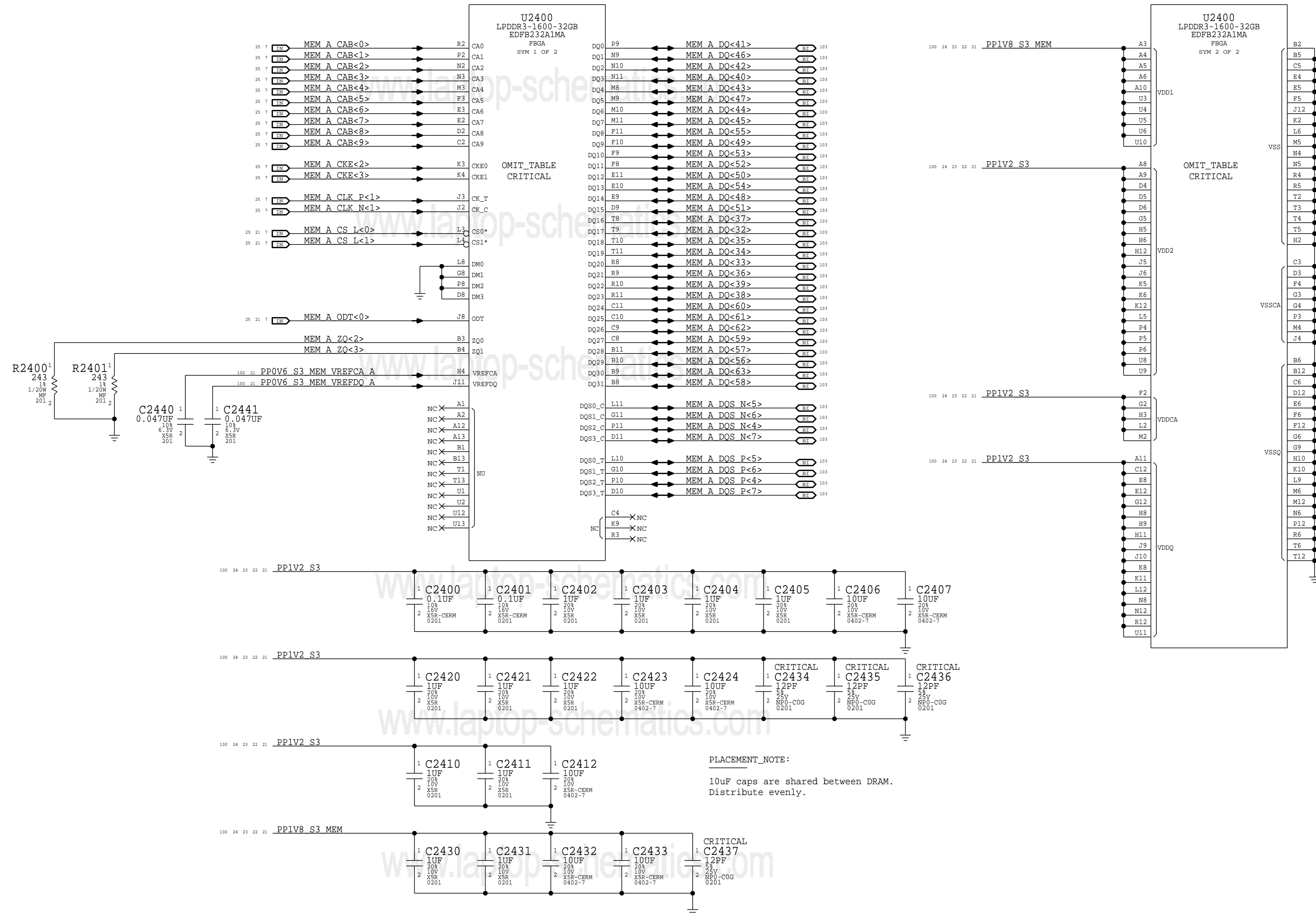
LPDDR3 CHANNEL A (0-31)



BOM_COST_GROUP=DRAM

| | | | |
|---|--|----------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 DRAM Channel A (00-31) | | | |
| | | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 23 OF 145 |
| | | SHEET | 21 OF 119 |

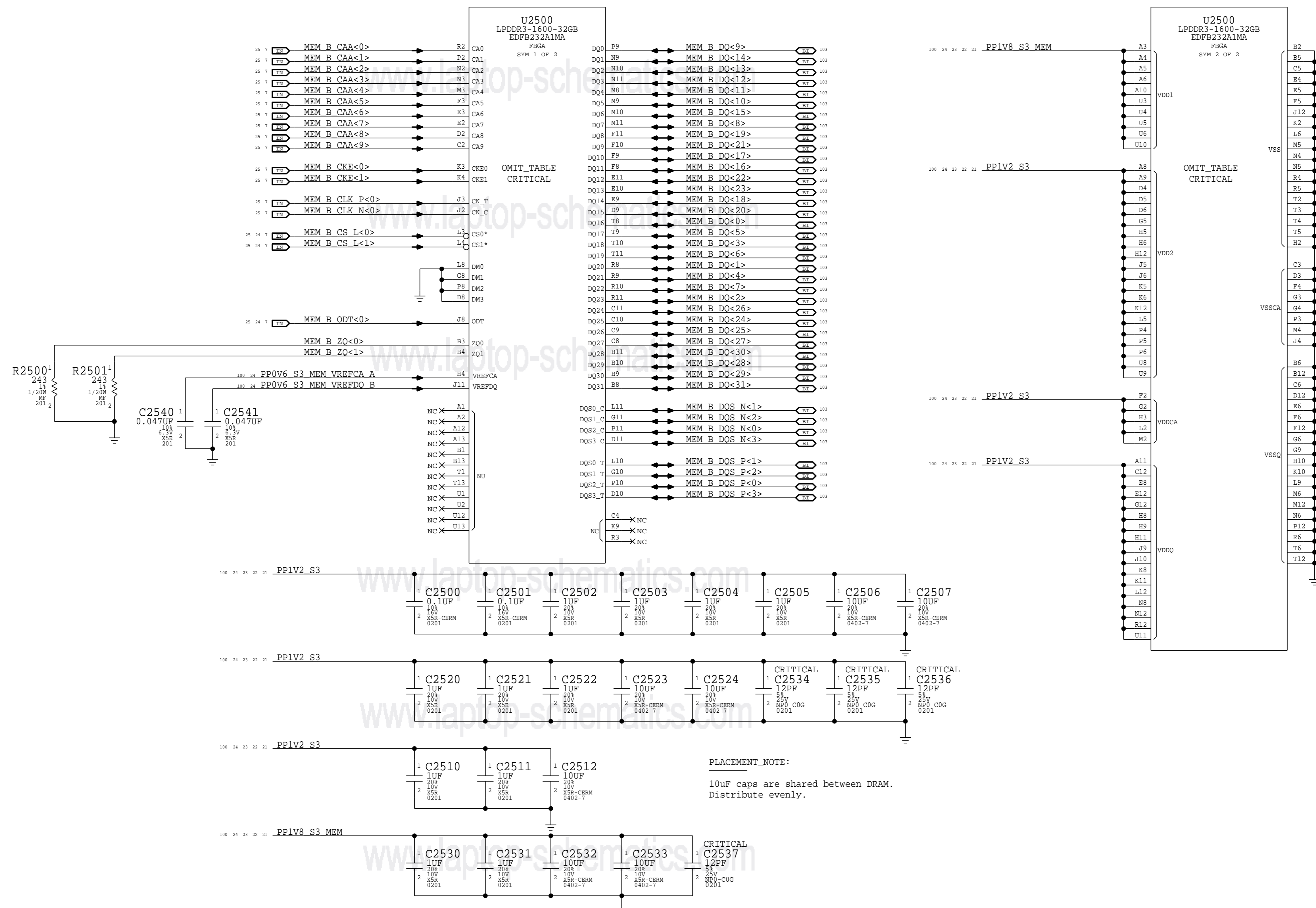
LPDDR3 CHANNEL A (32-63)



BOM_COST_GROUP=DRAM

| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 DRAM Channel A (32-63) | | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 | STEP |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | 24 OF 145 |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | SHEET | 22 OF 119 |
| I1 NOT TO REPRODUCE OR COPY IT | | | |
| I2 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | | |
| I4 ALL RIGHTS RESERVED | | | |

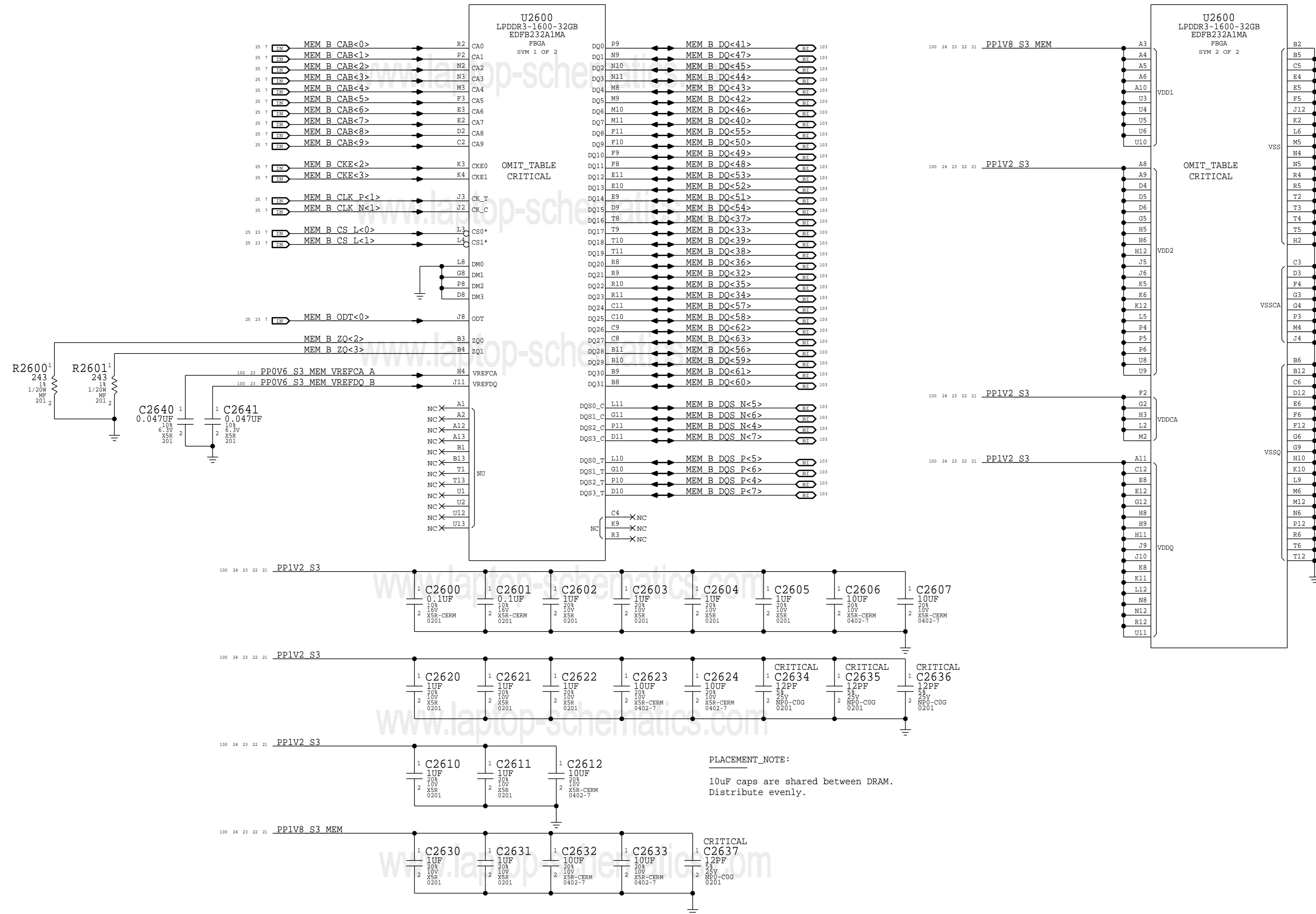
LPDDR3 CHANNEL B (0-31)



BOM_COST_GROUP=DRAM

| | | | |
|--|----------------|----------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 DRAM Channel B (00-31) | | | |
| | DRAWING NUMBER | 051-00777 | |
| | REVISION | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2 NOT TO REPRODUCE OR COPY IT 3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4 ALL RIGHTS RESERVED | | PAGE | 25 OF 145 |
| | | SHEET | 23 OF 119 |

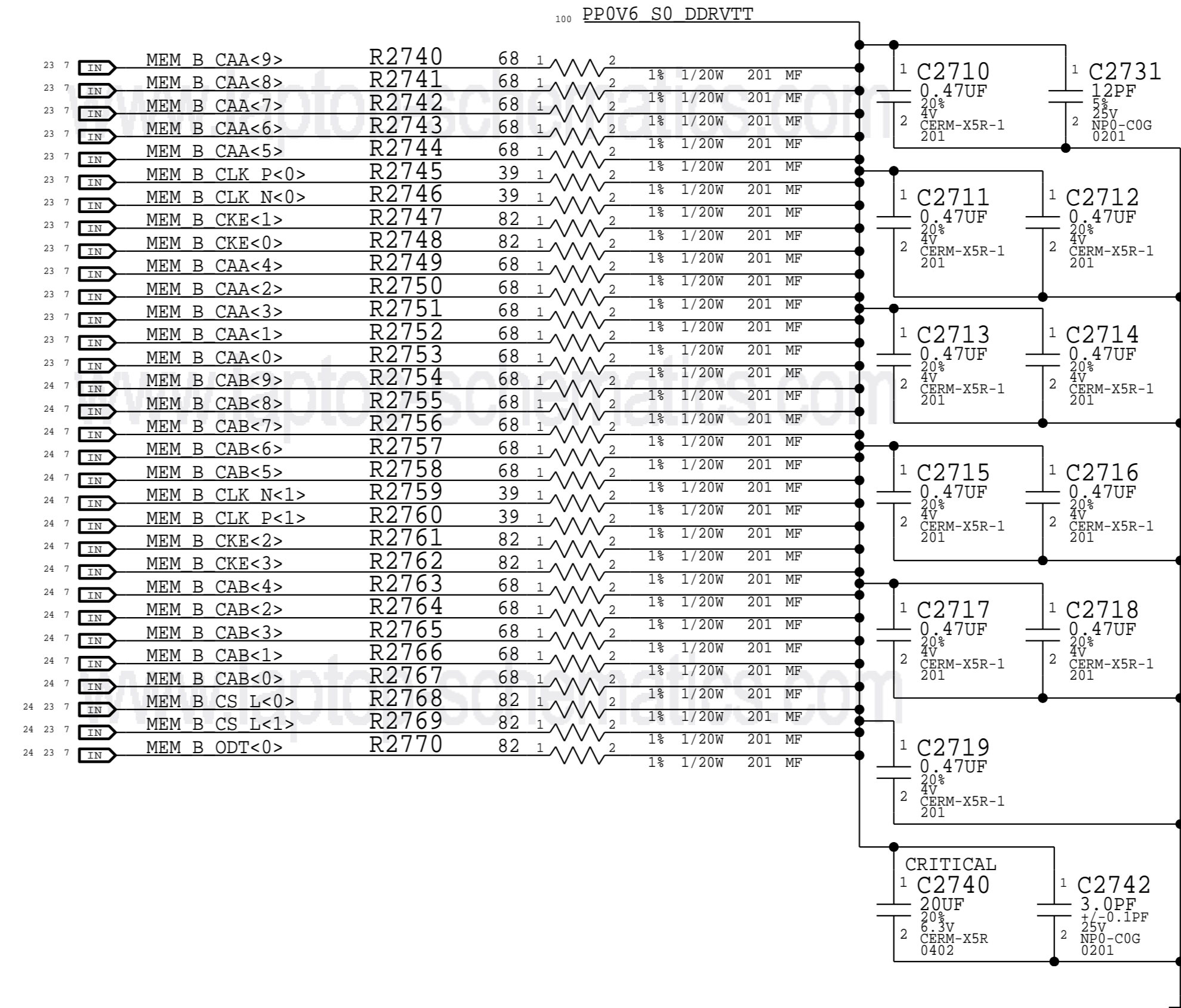
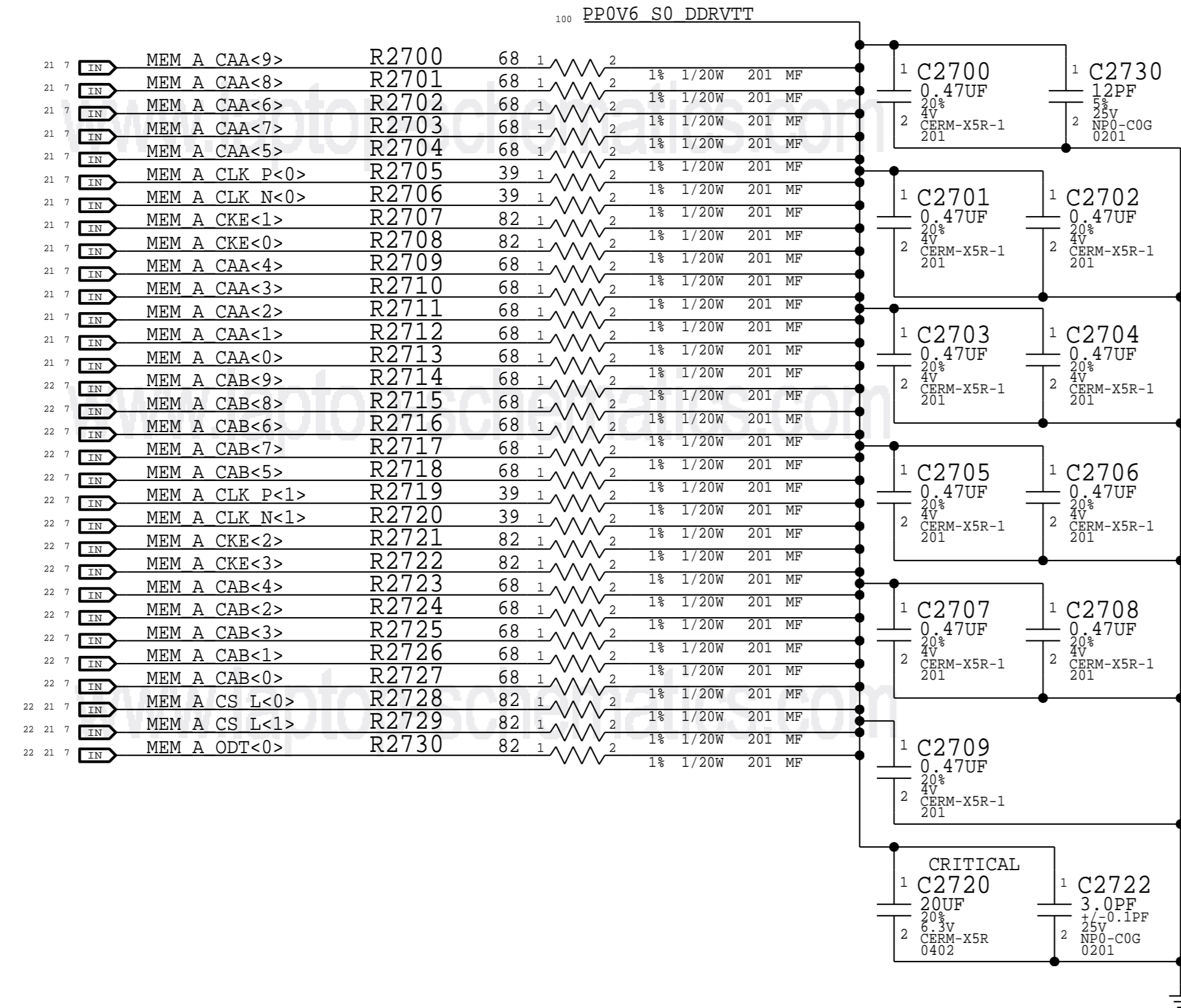
LPDDR3 CHANNEL B (32-63)



BOM_COST_GROUP=DRAM

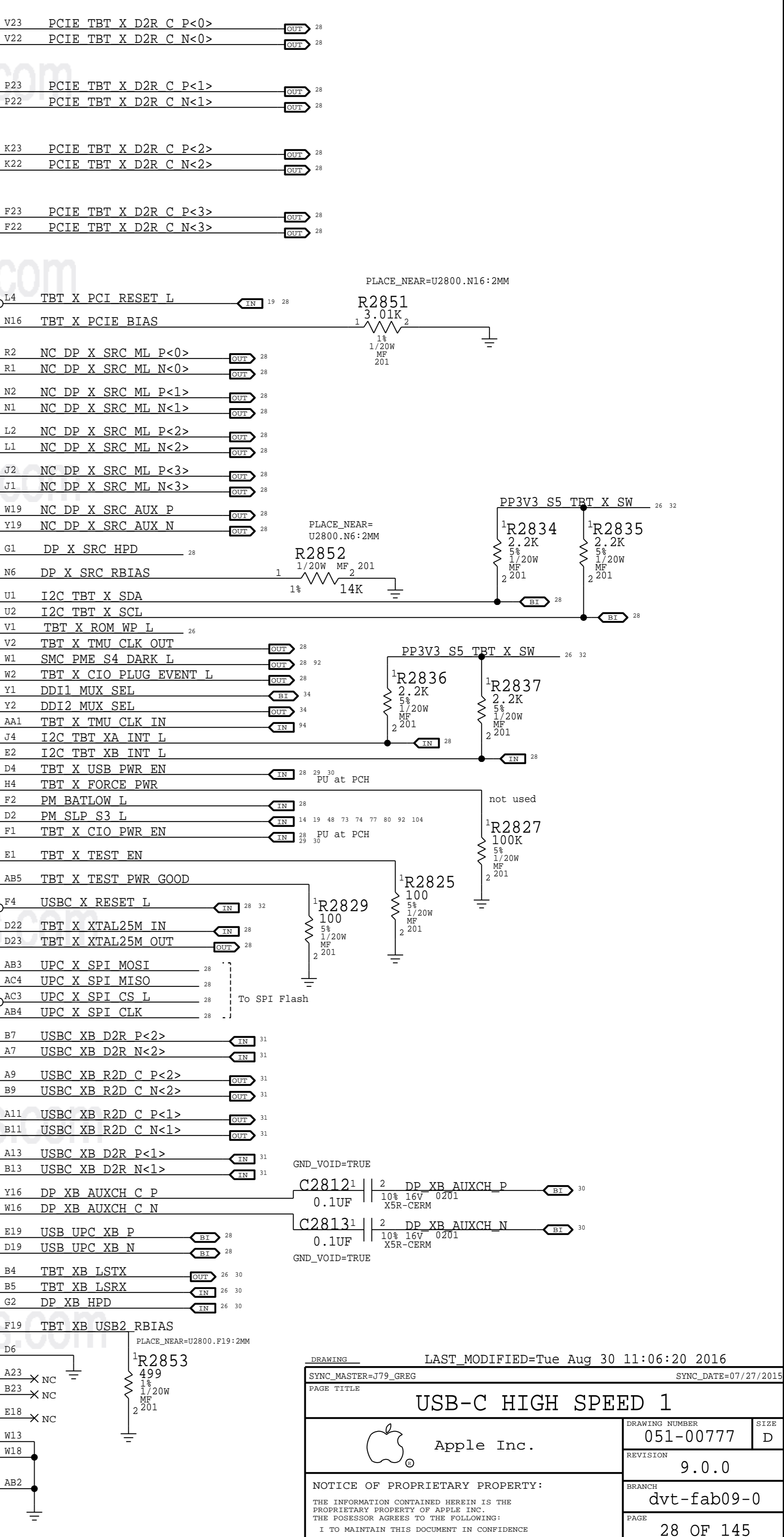
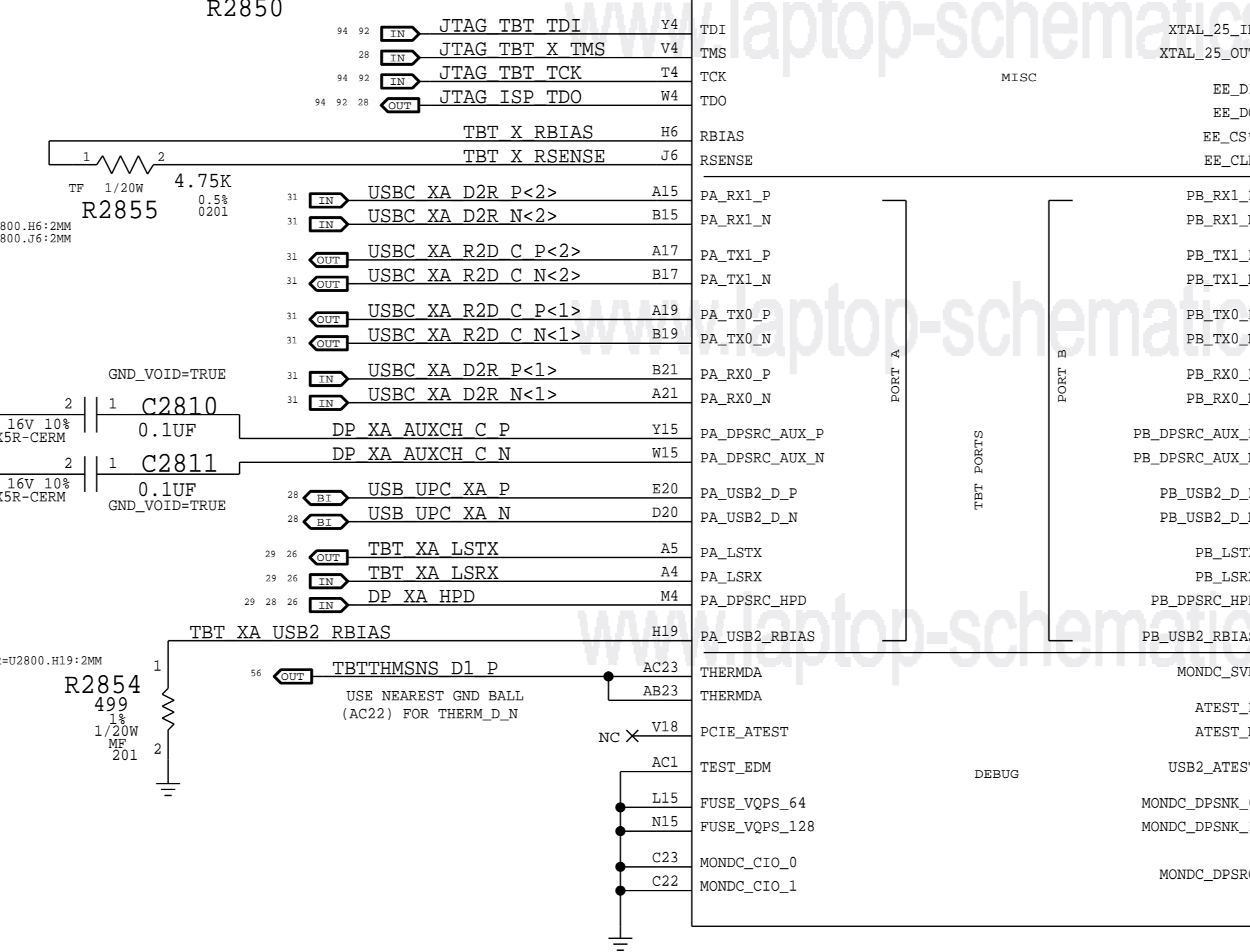
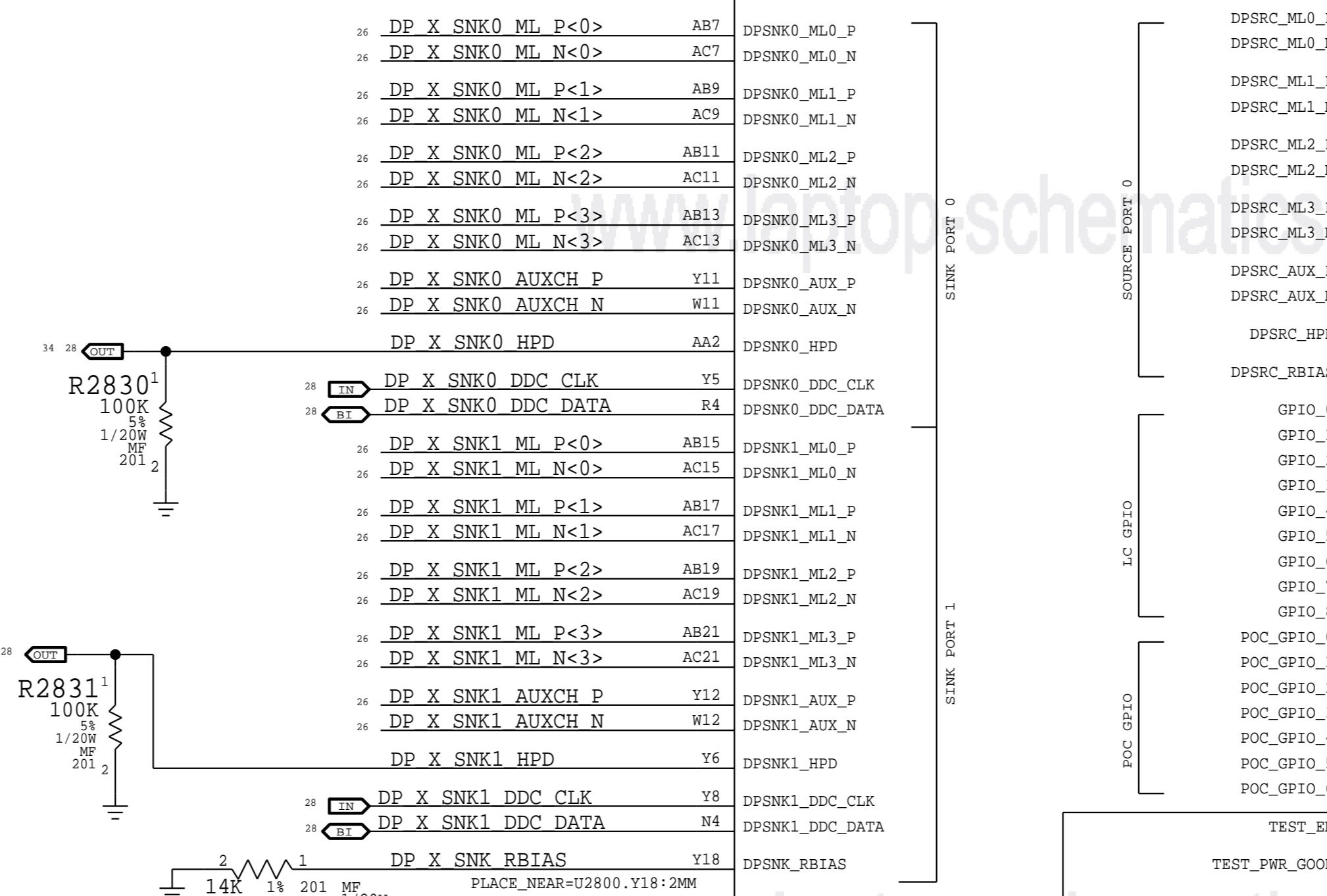
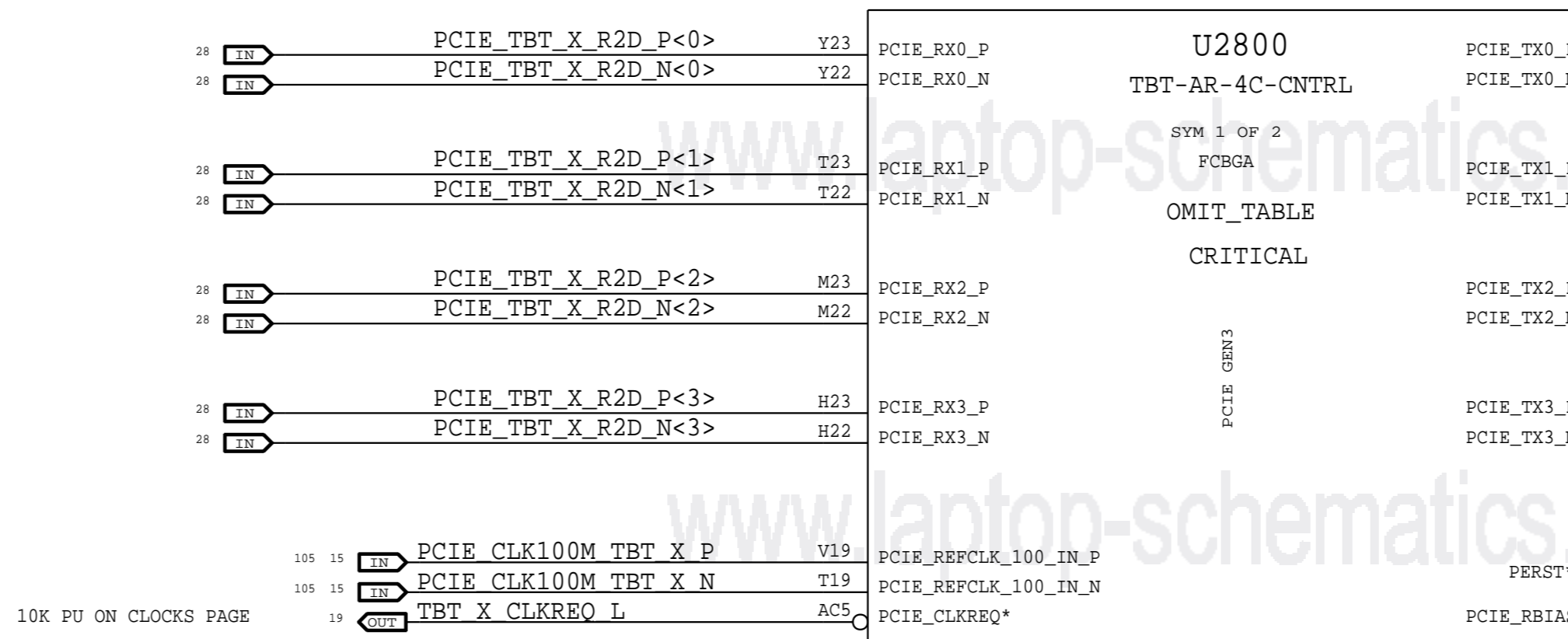
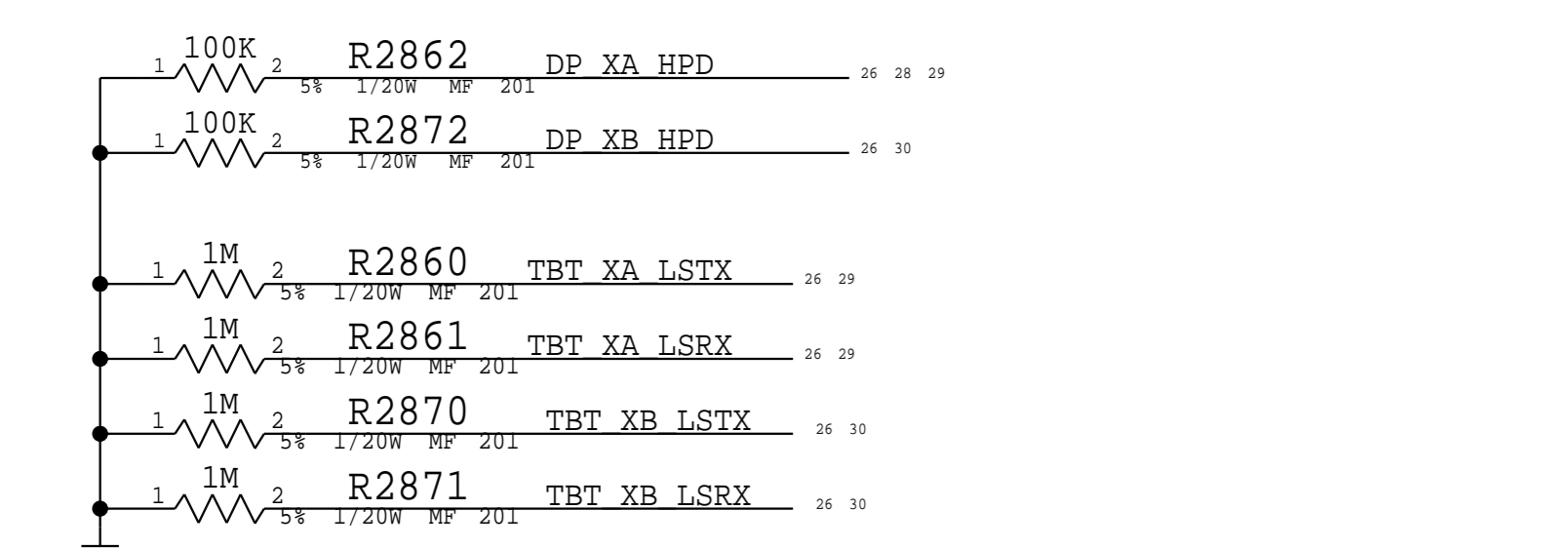
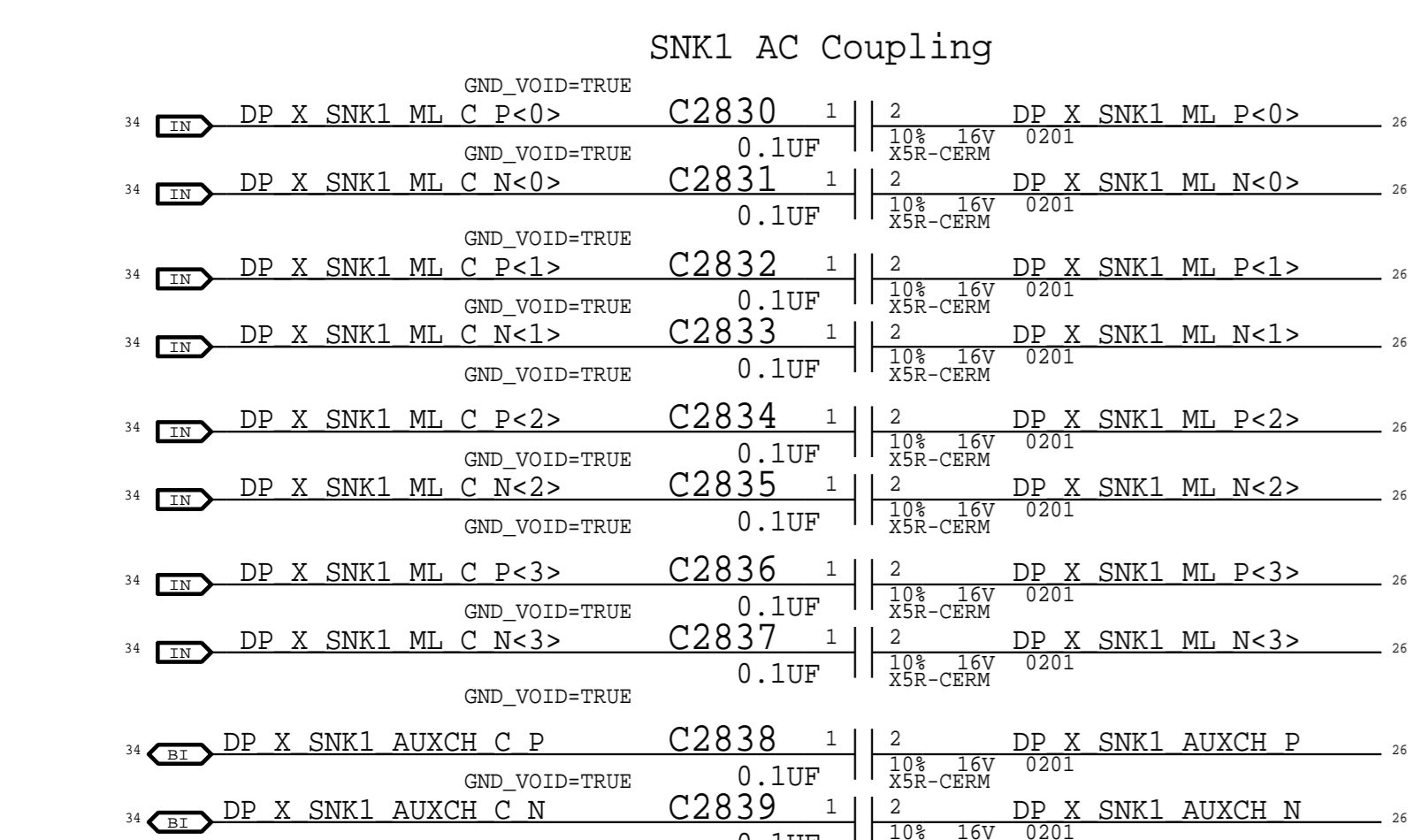
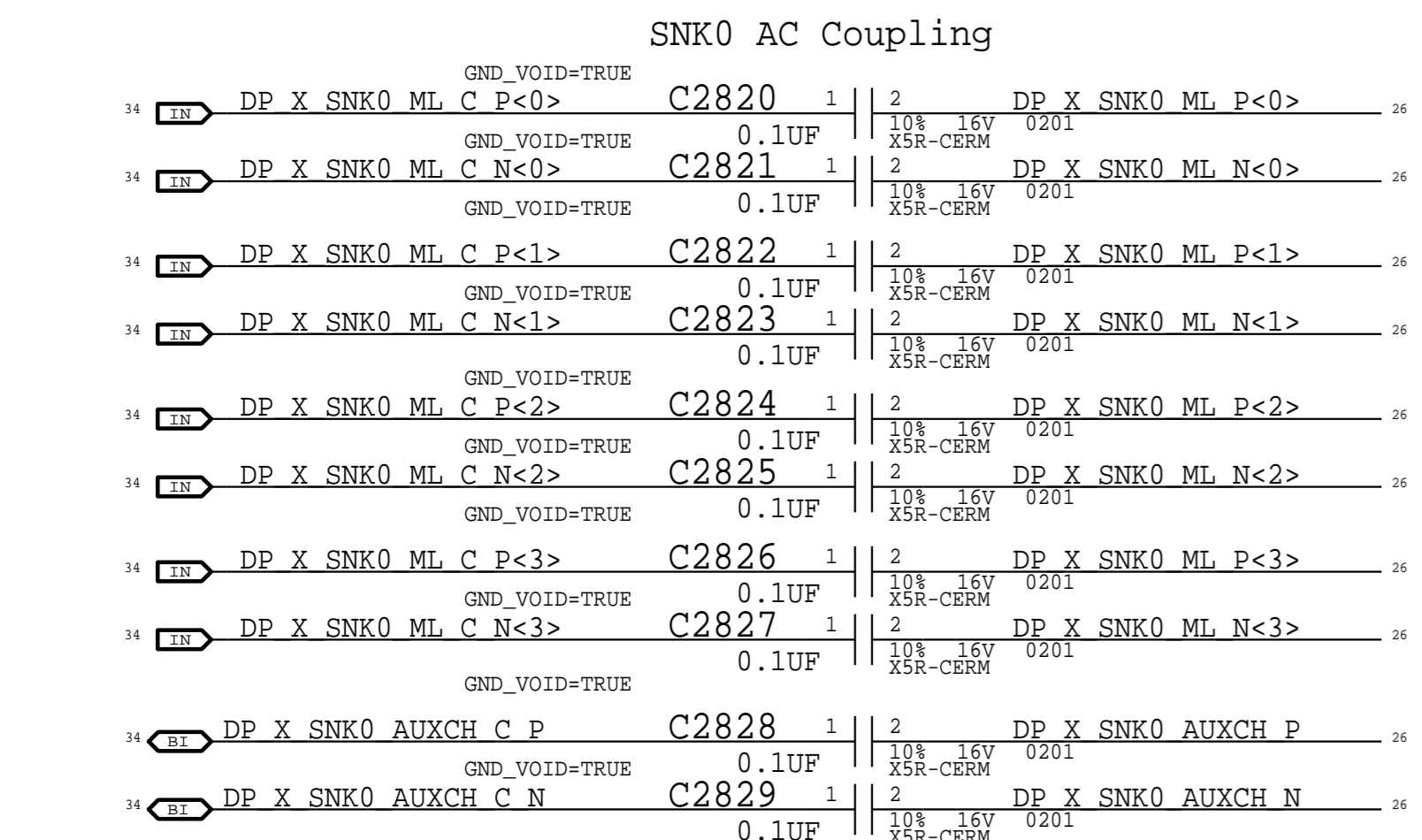
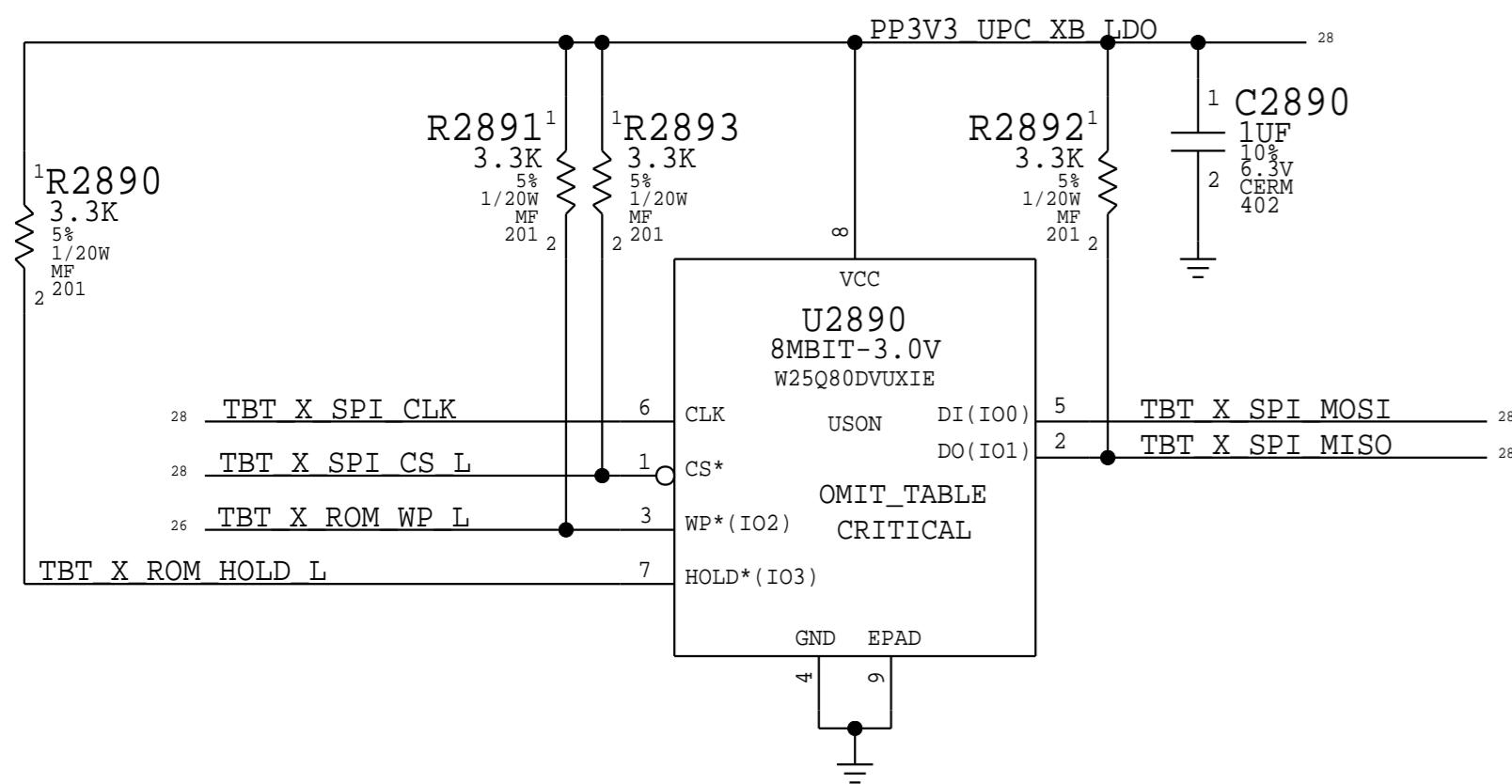
| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 DRAM Channel B (32-63) | | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 | STEP |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvf-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | 26 OF 145 |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | SHEET | 24 OF 119 |
| I1 NOT TO REPRODUCE OR COPY IT | | | |
| I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | | |
| I1V ALL RIGHTS RESERVED | | | |

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK



BOM_COST_GROUP=DRAM

| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=J52_MLB | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| LPDDR3 DRAM Termination | | | |
| | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 27 OF 145 |
| | | SHEET | 25 OF 119 |



DRAWING: LAST MODIFIED= Tue Aug 30 11:06:20 2016

SYNC_MASTER=J79_GREG SYNC_DATE=07/27/2015

PAGE TITLE: USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER: 051-00777

REVISION: 9.0.0

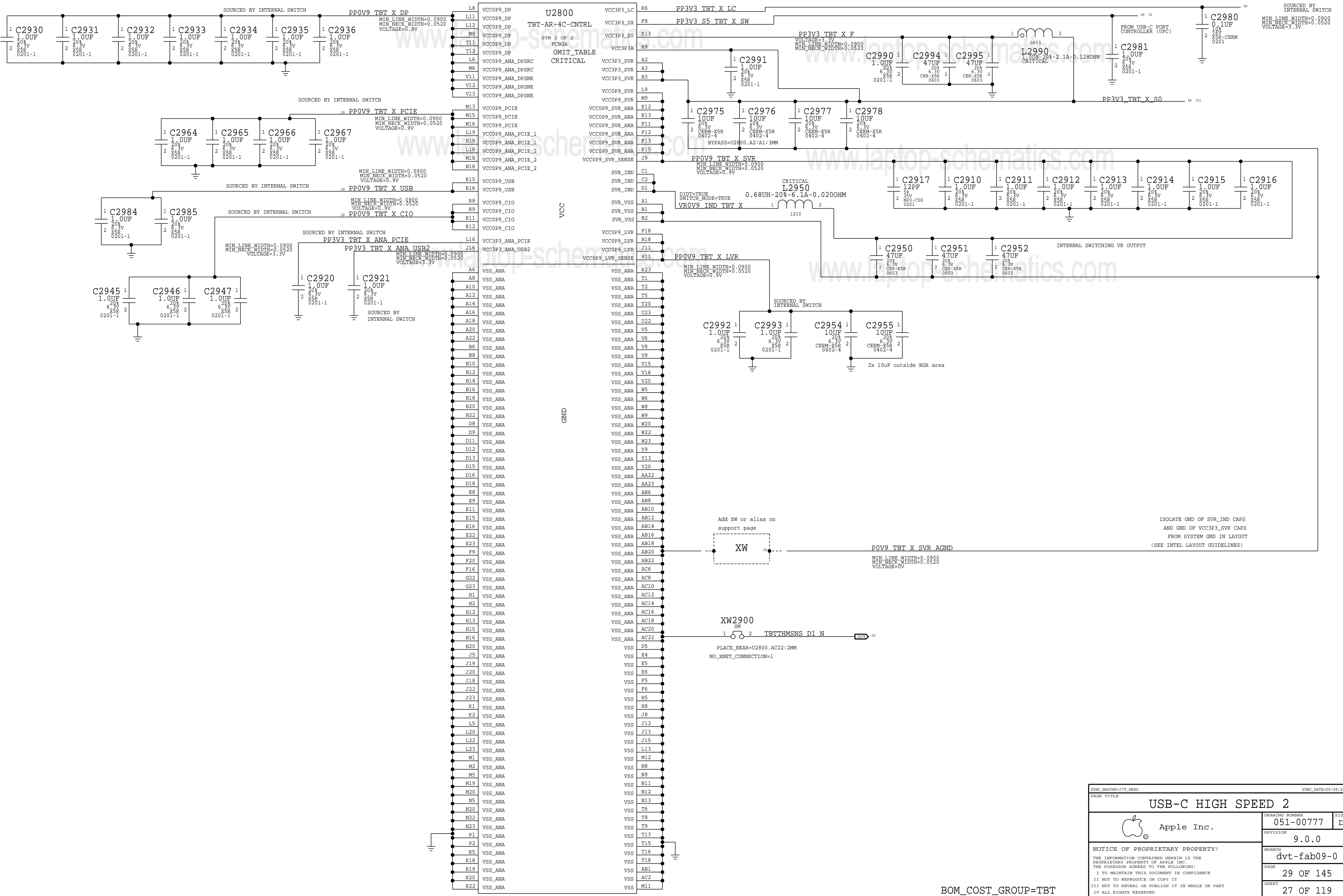
BRANCH: dvt-fab09-0

PAGE: 28 OF 145

SHEET: 26 OF 119

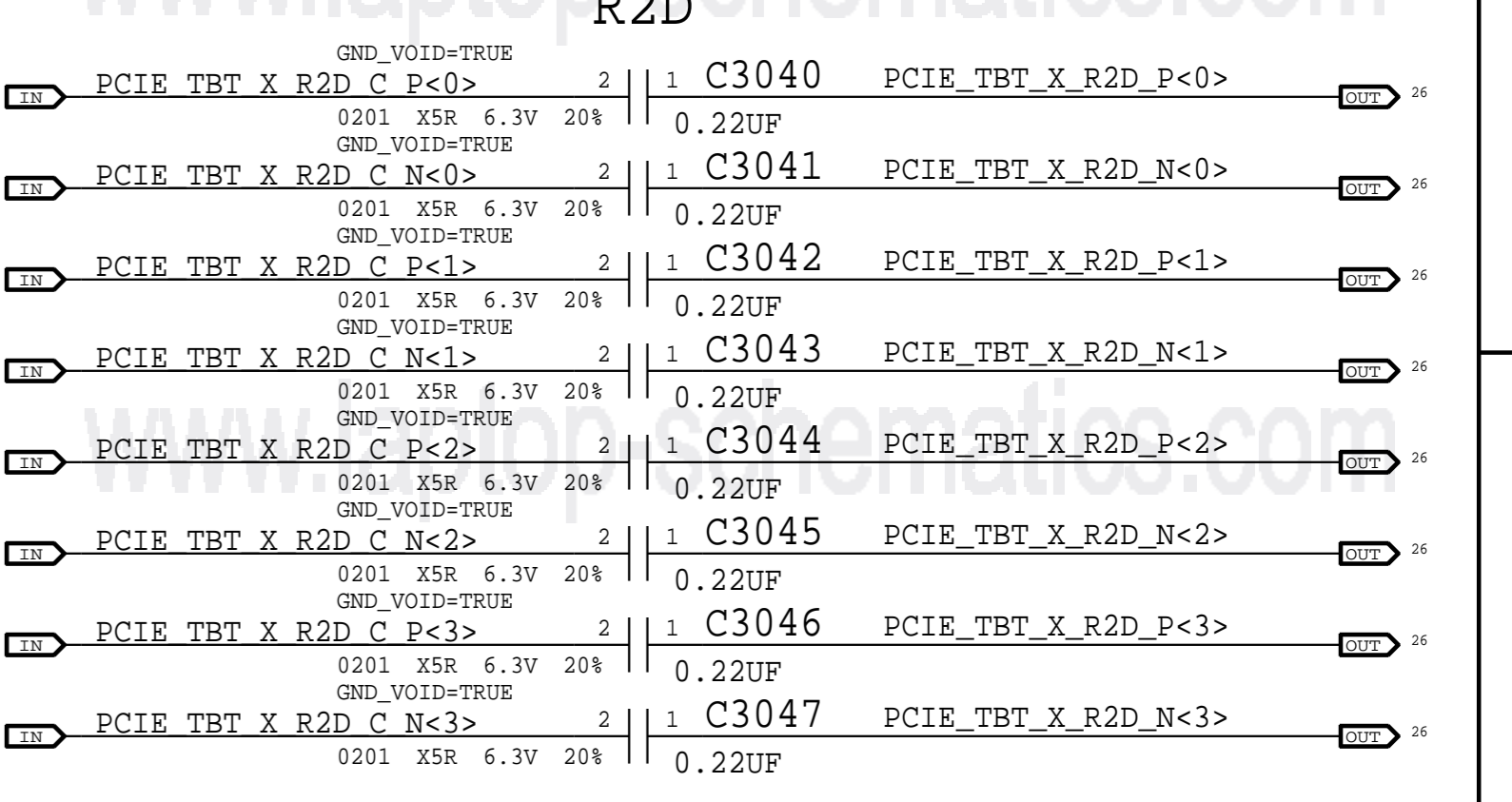
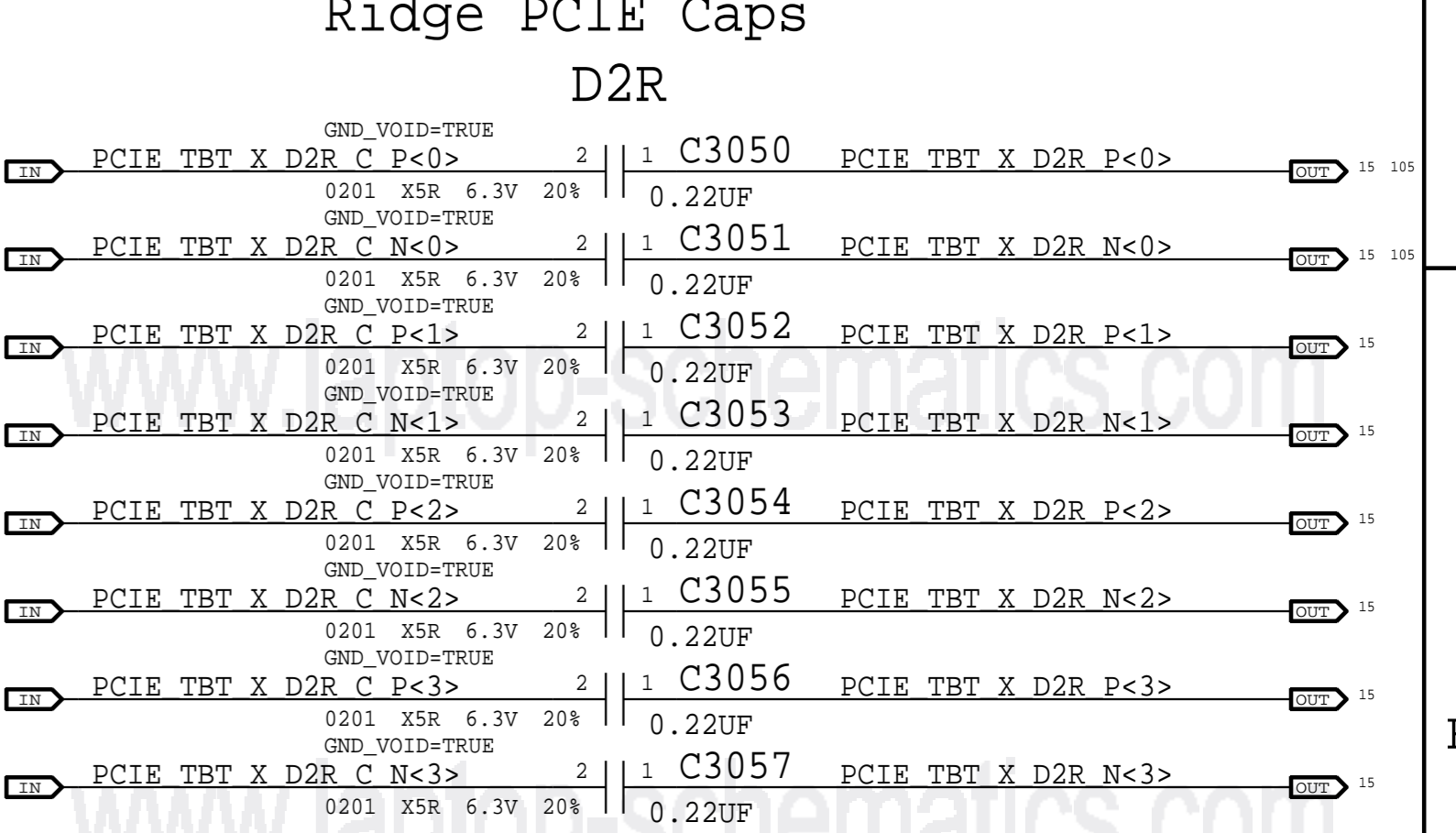
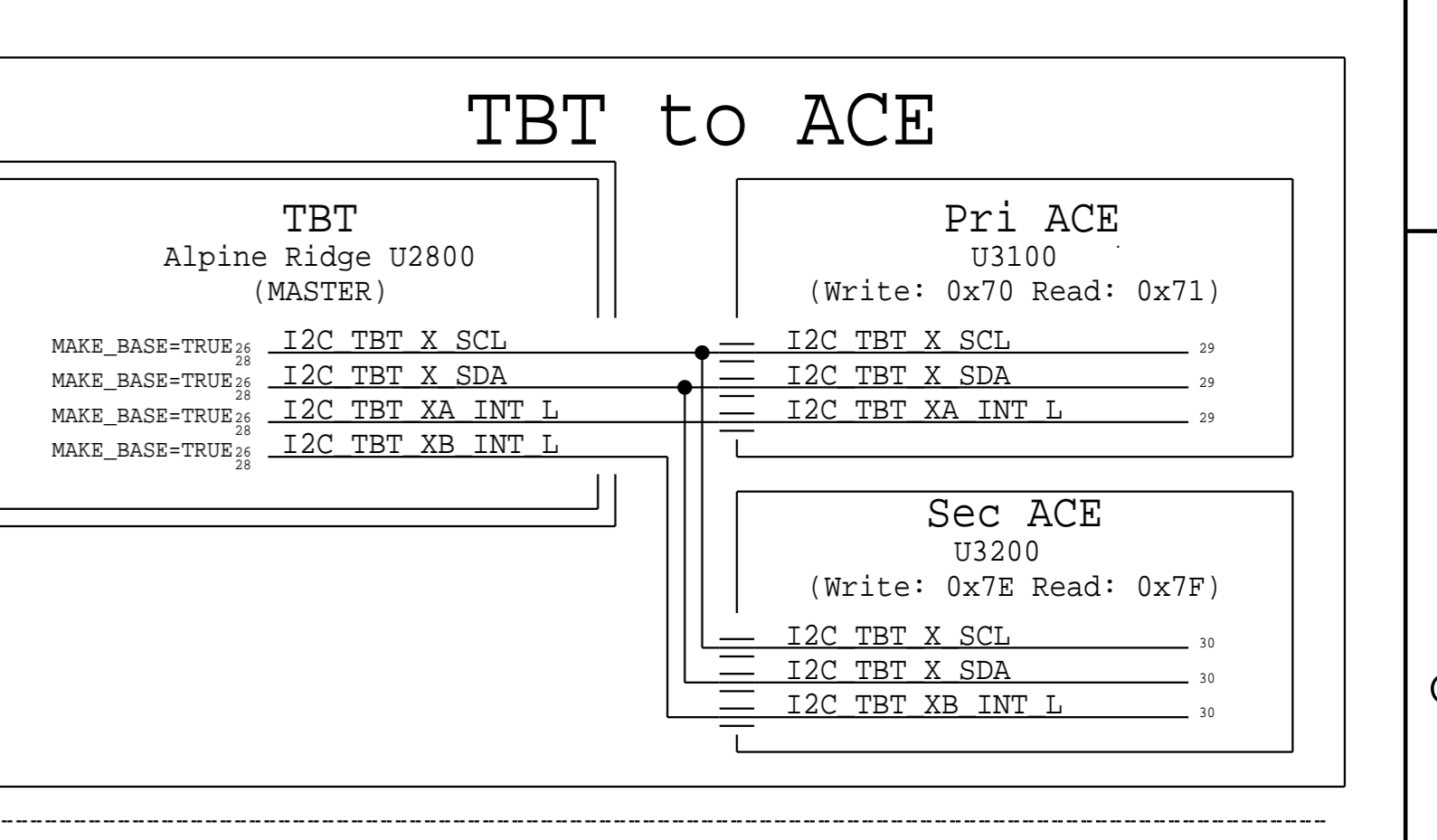
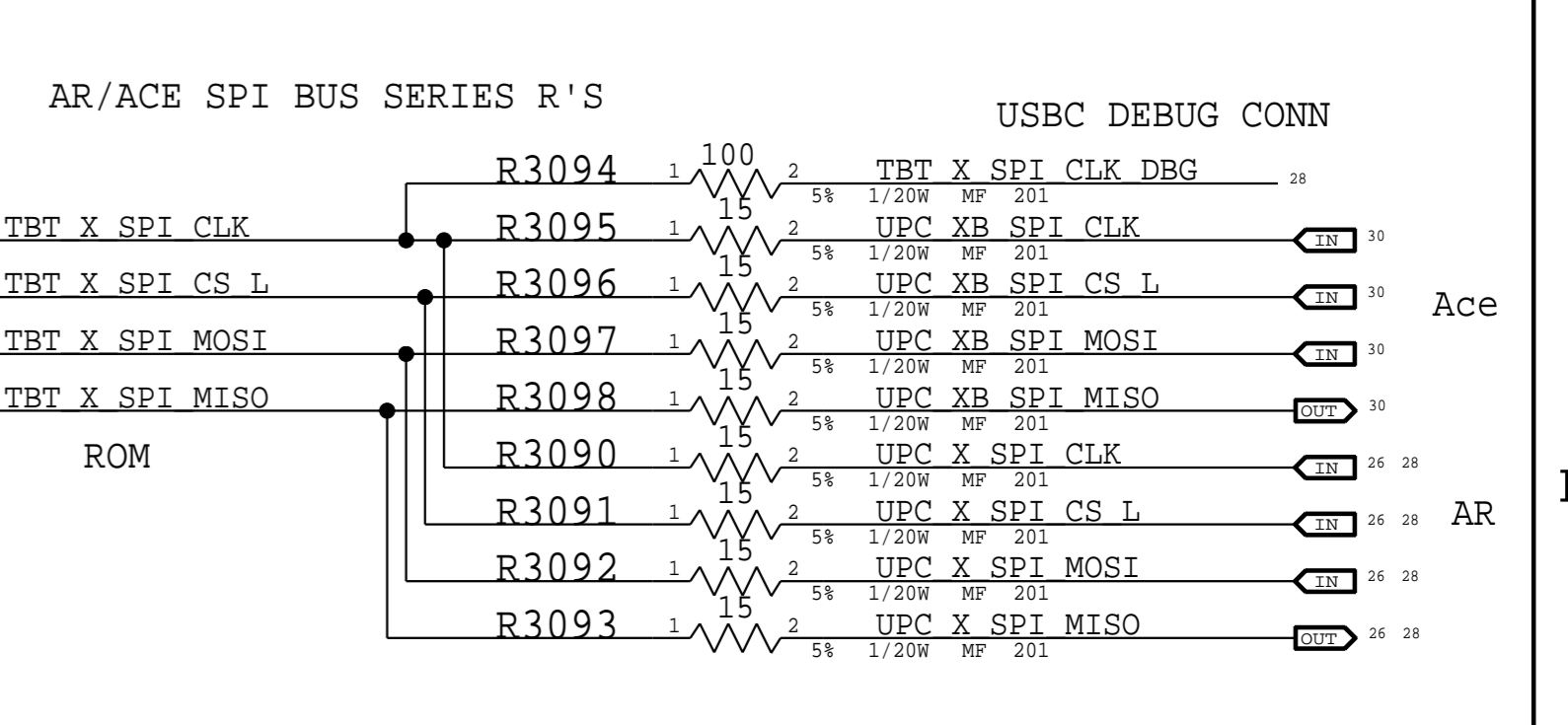
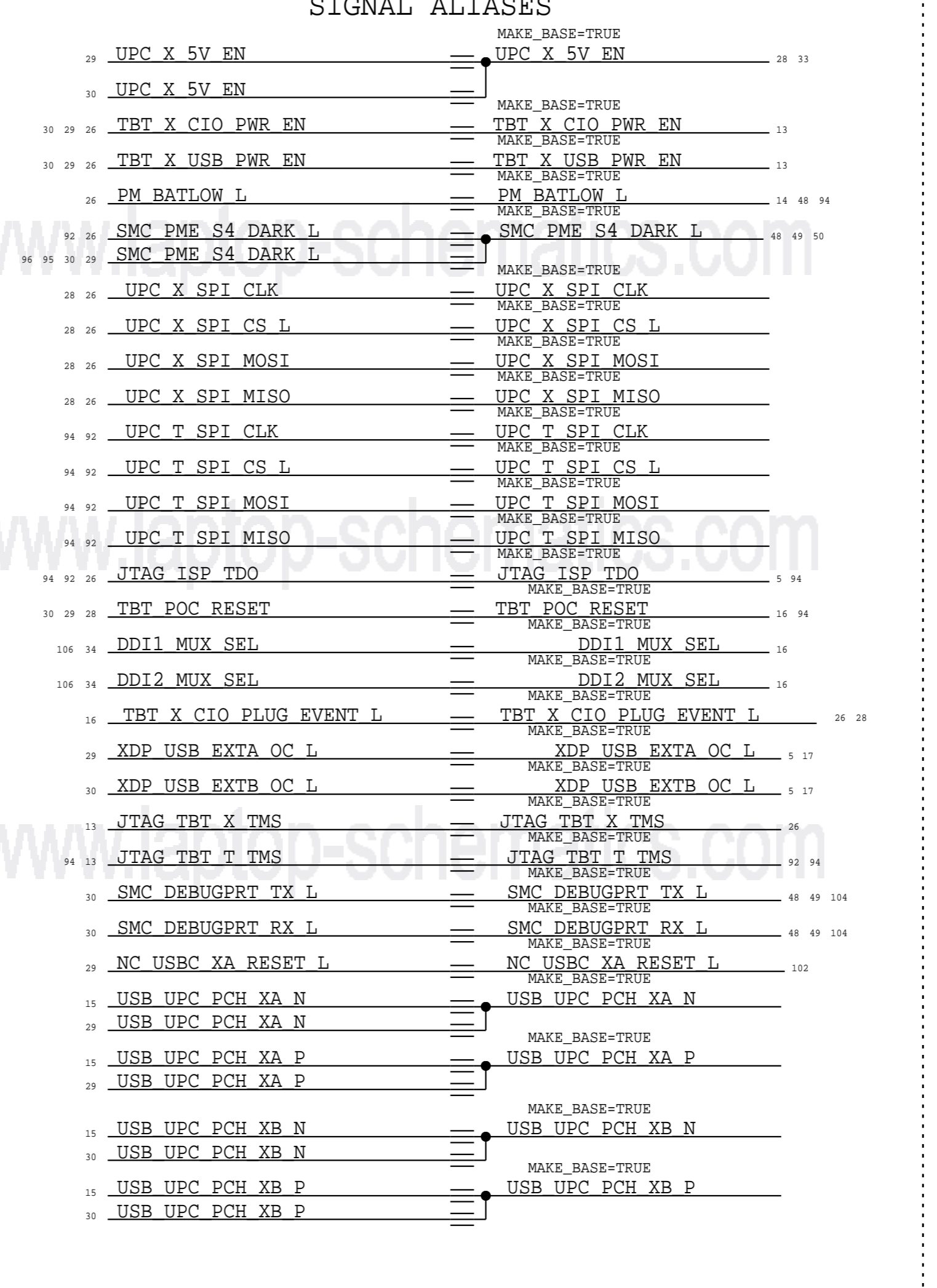
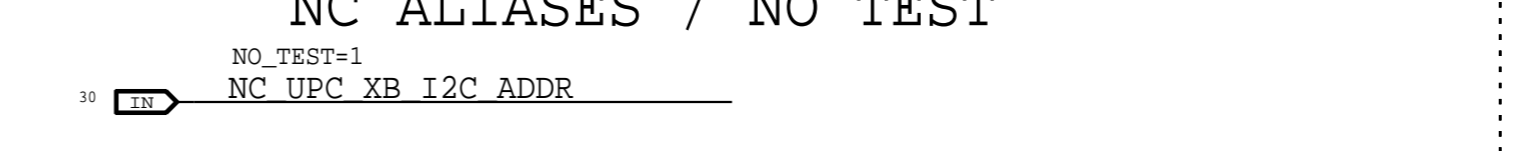
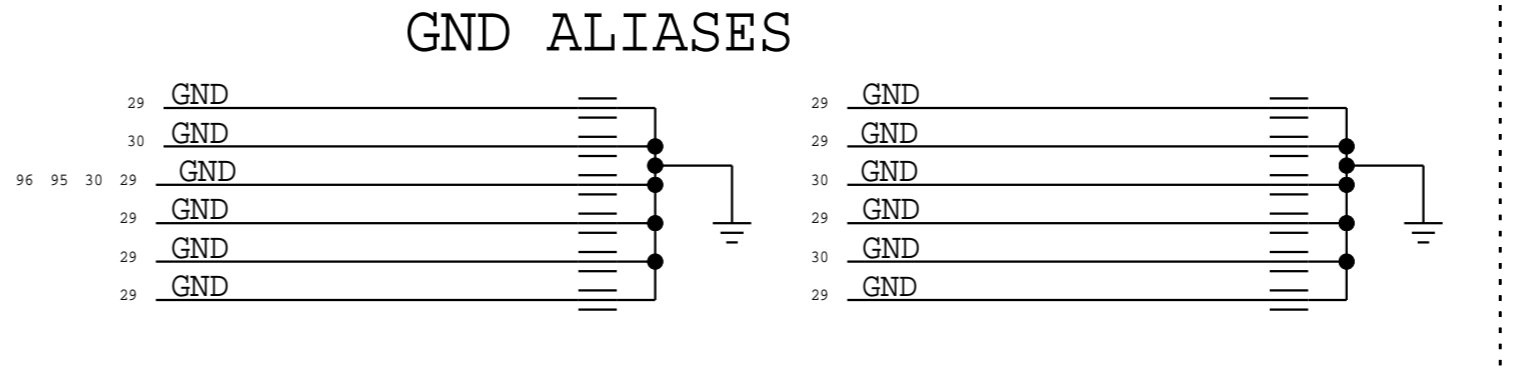
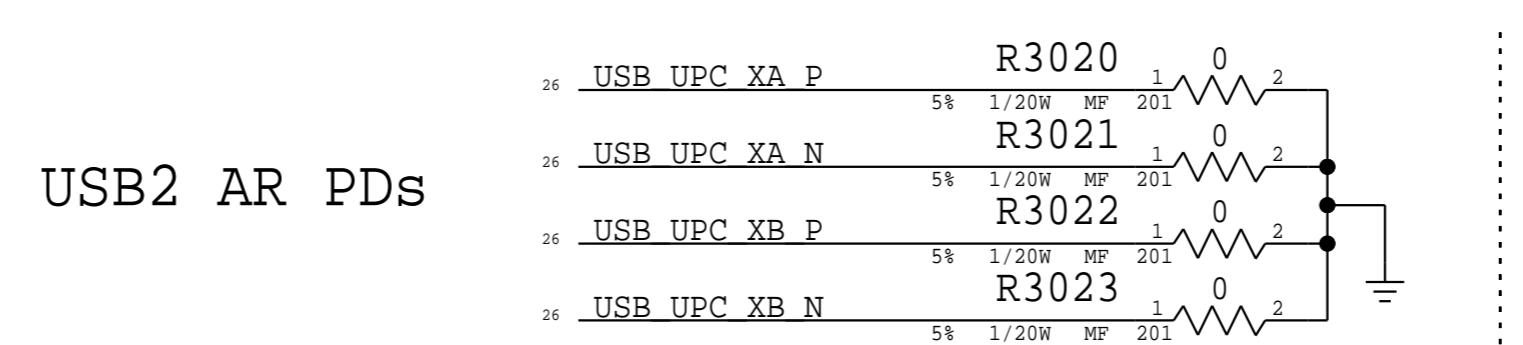
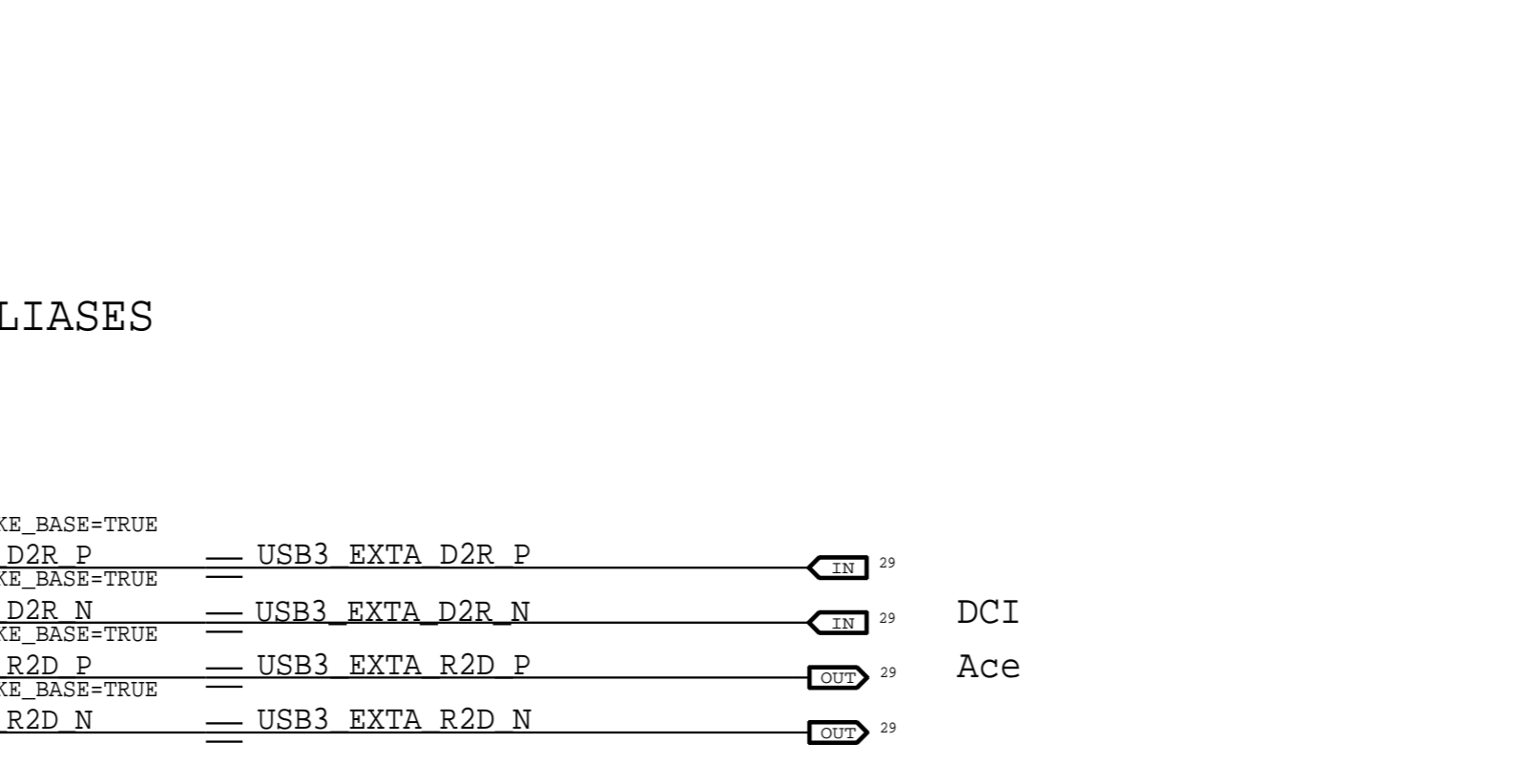
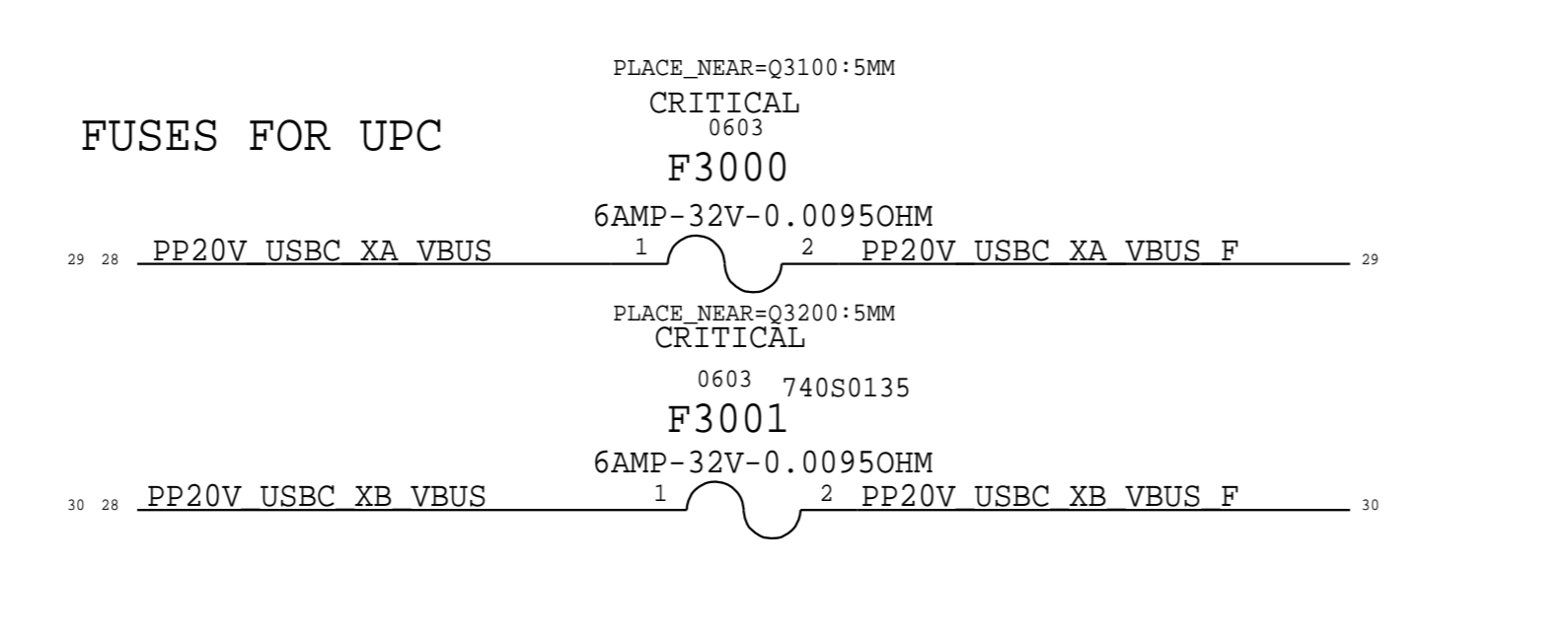
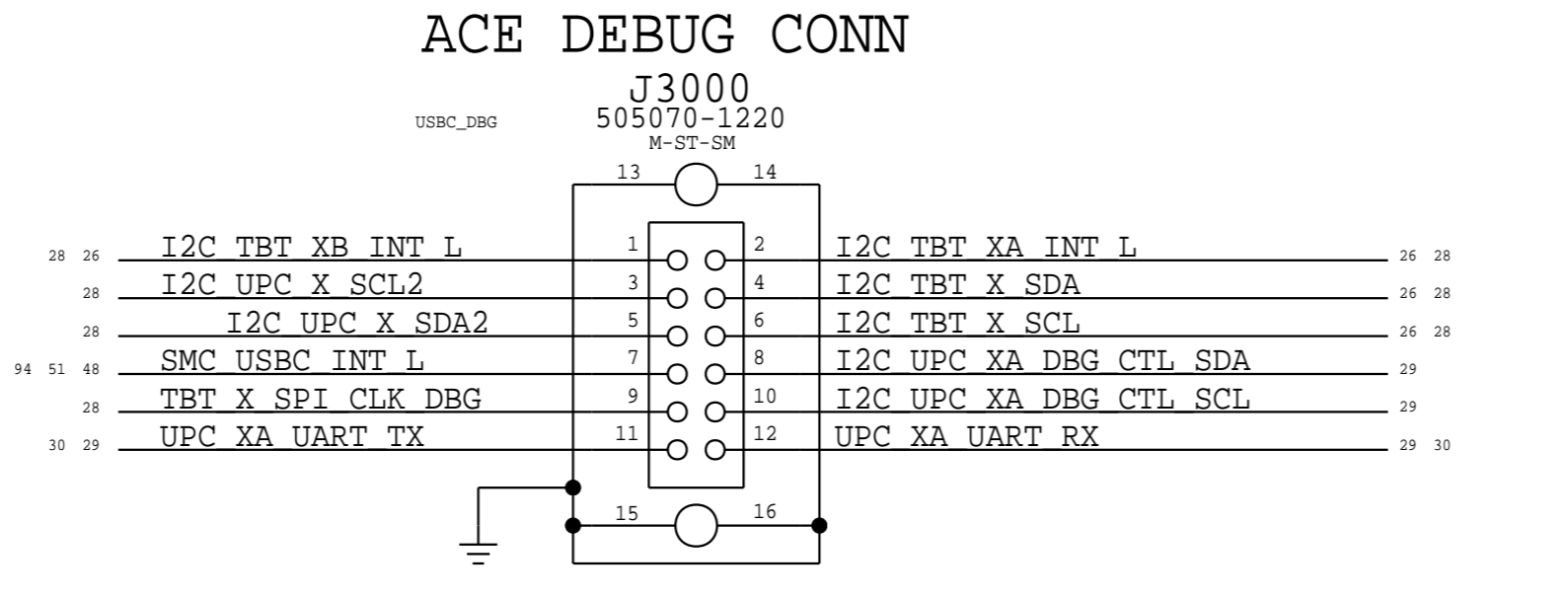
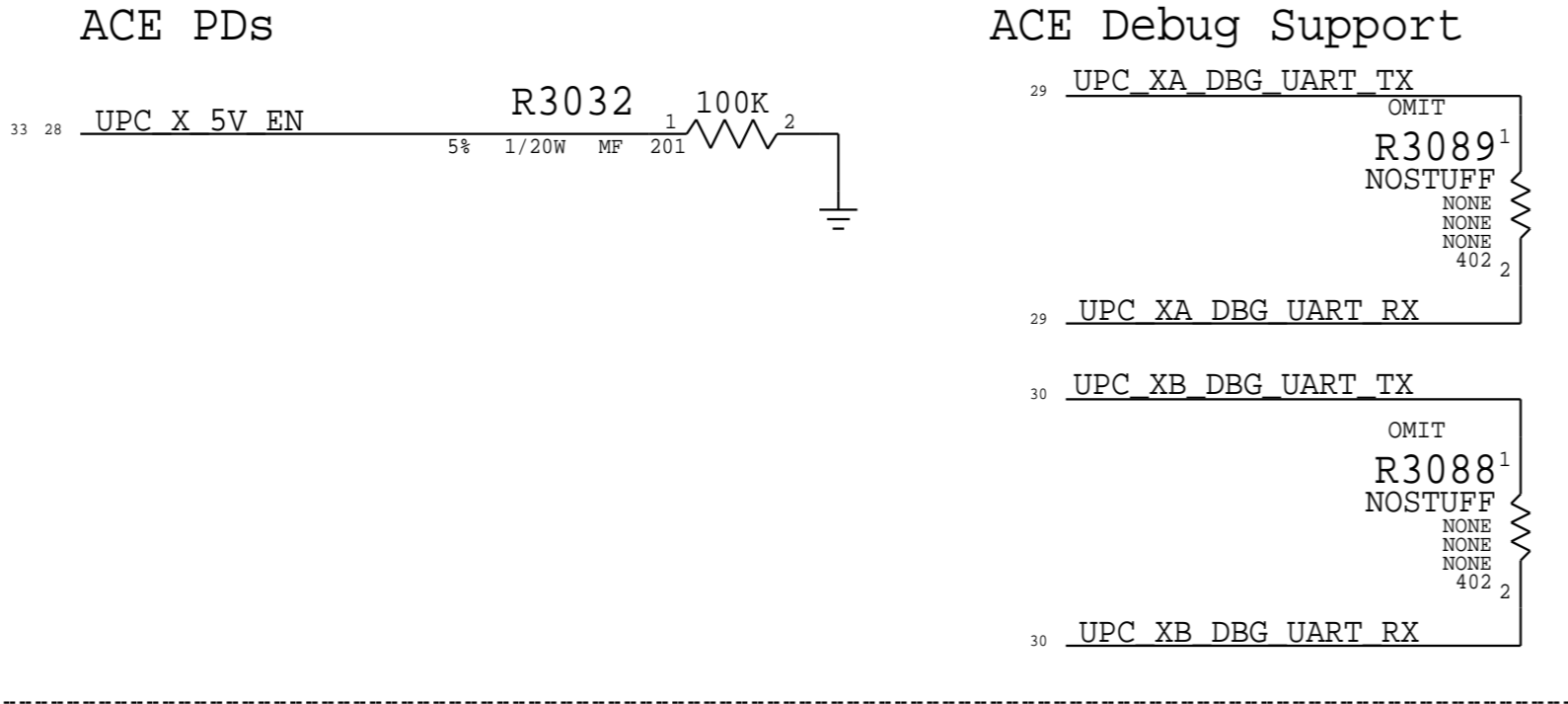
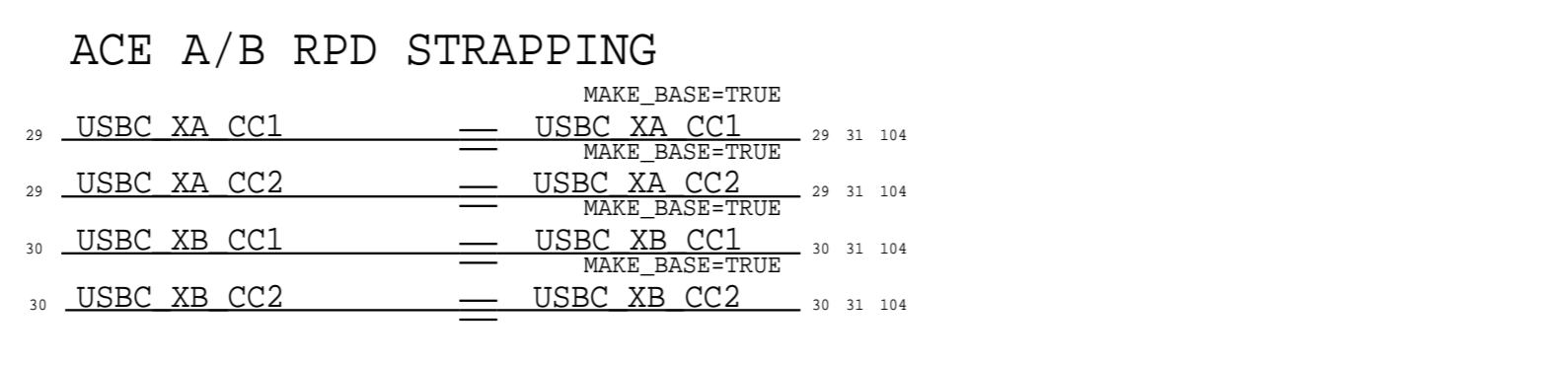
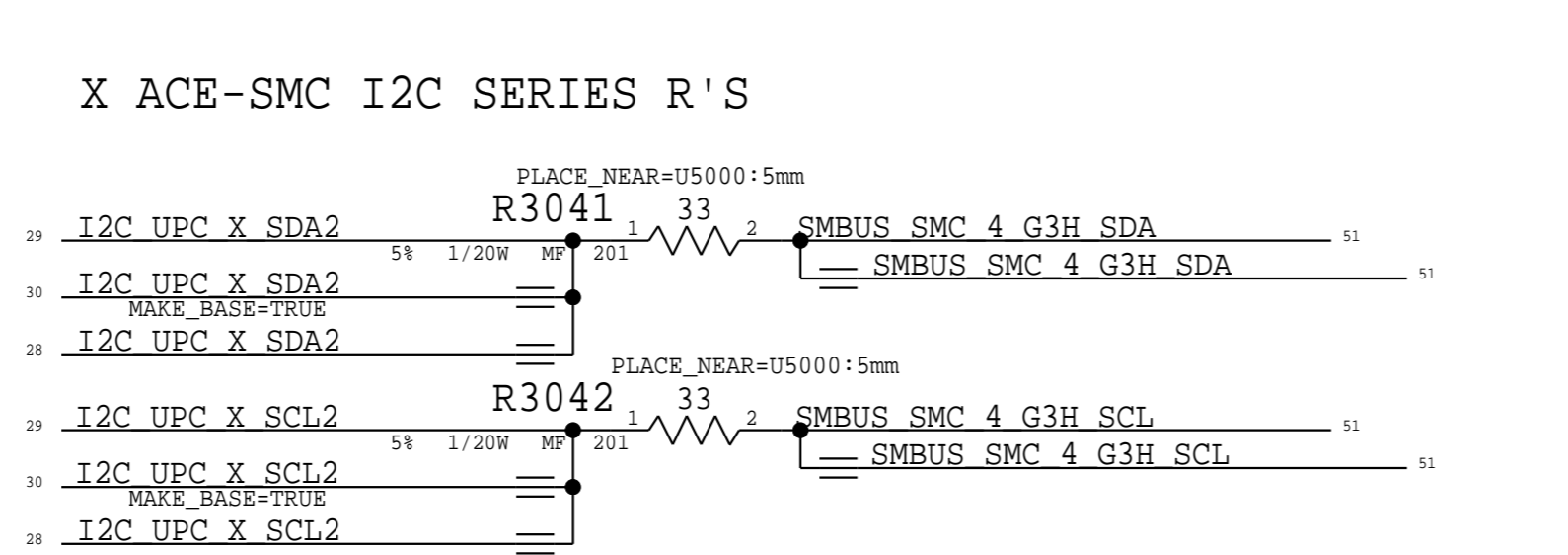
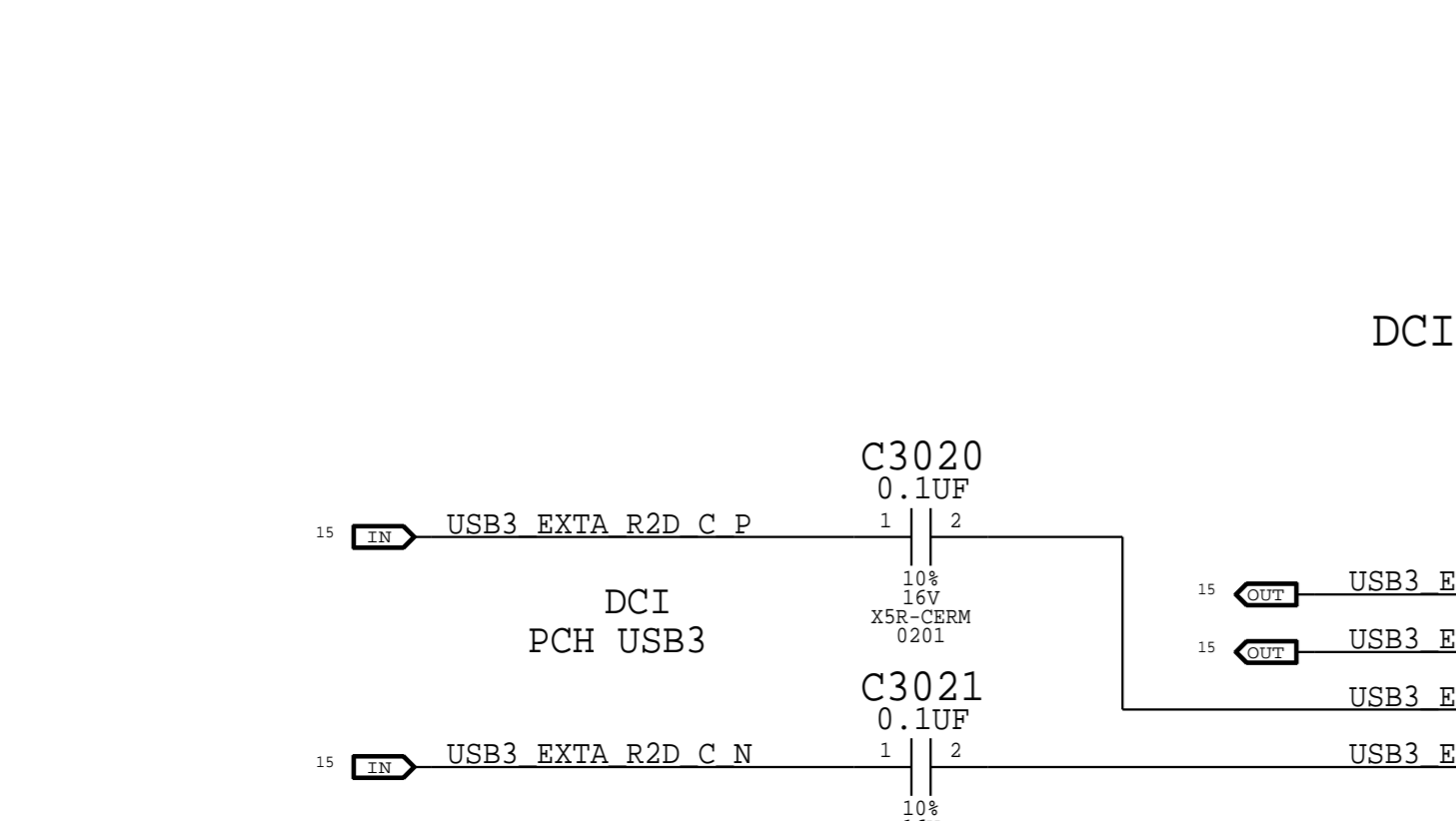
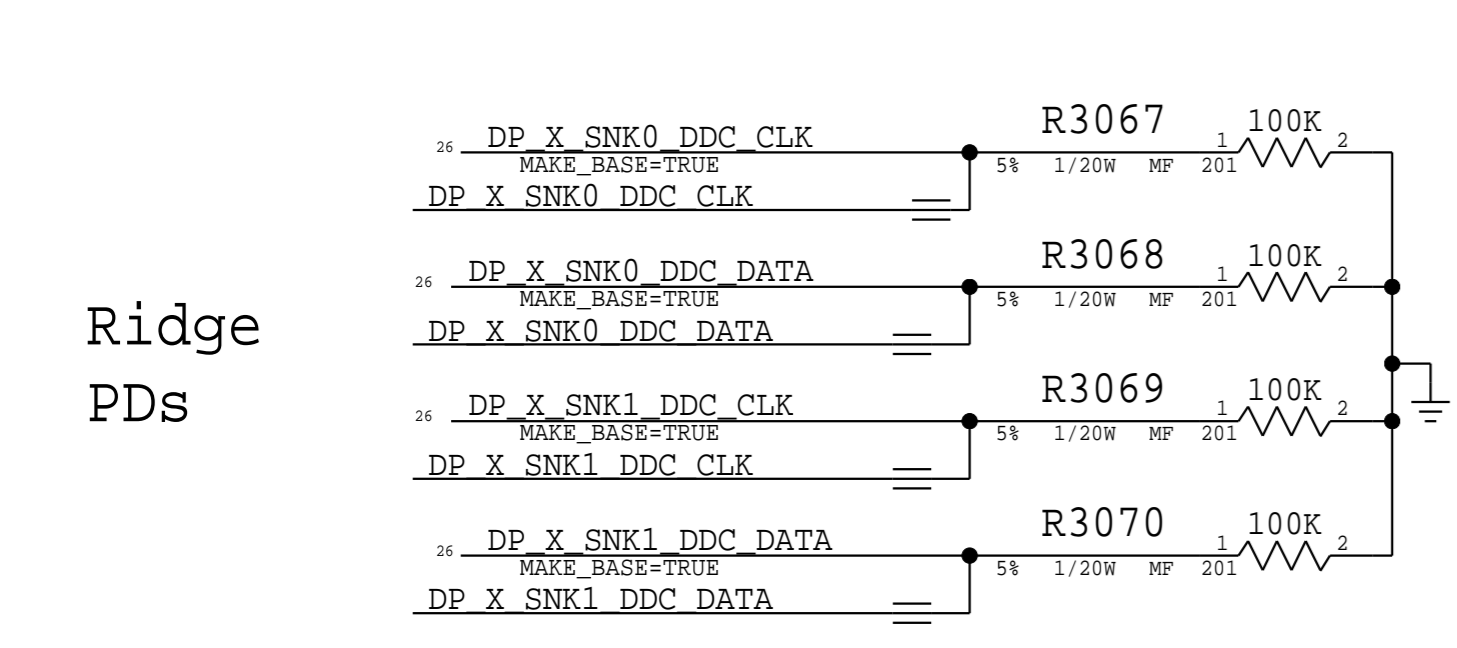
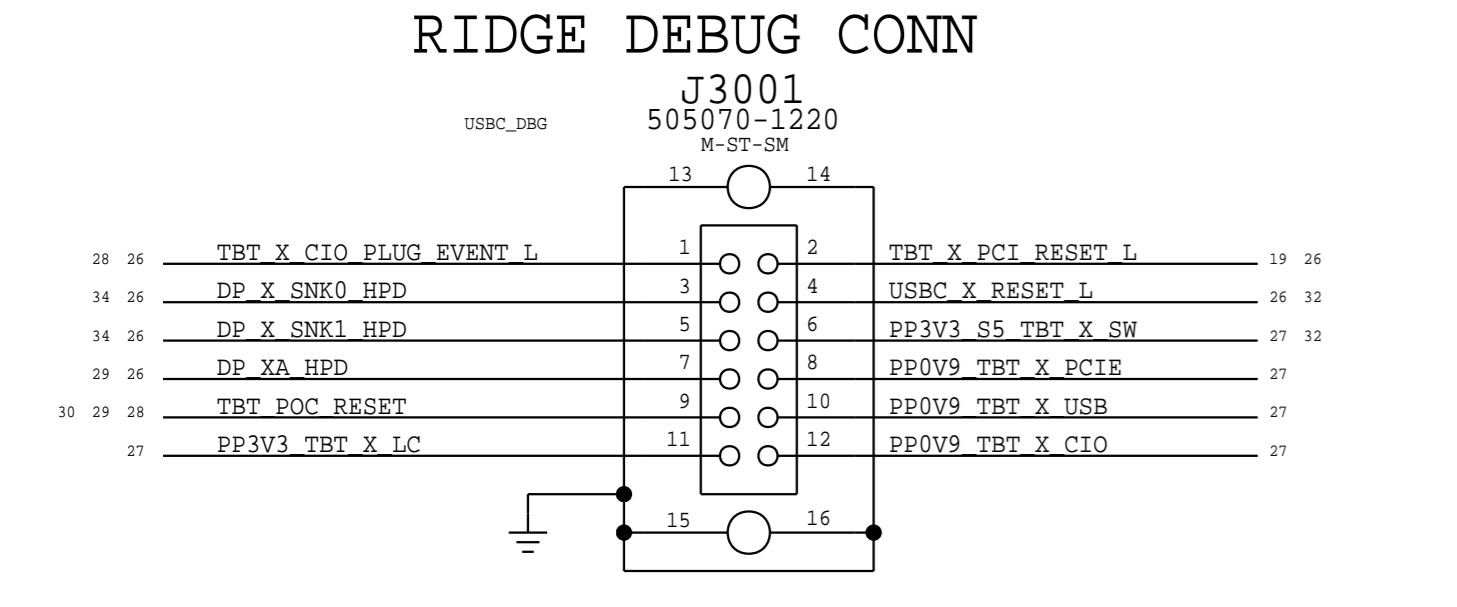
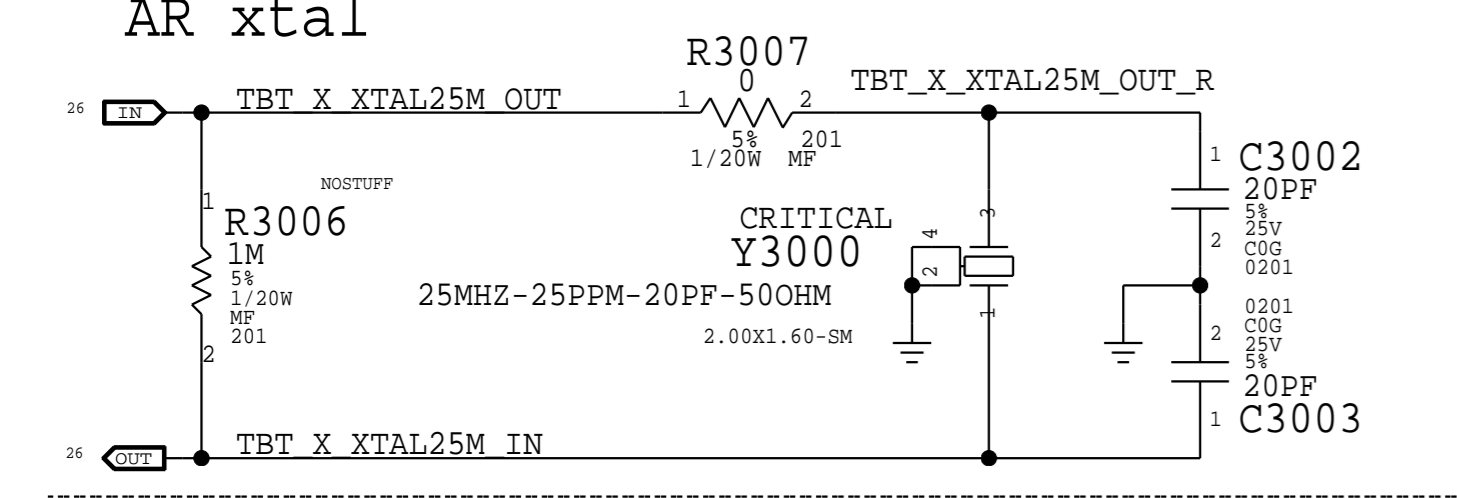
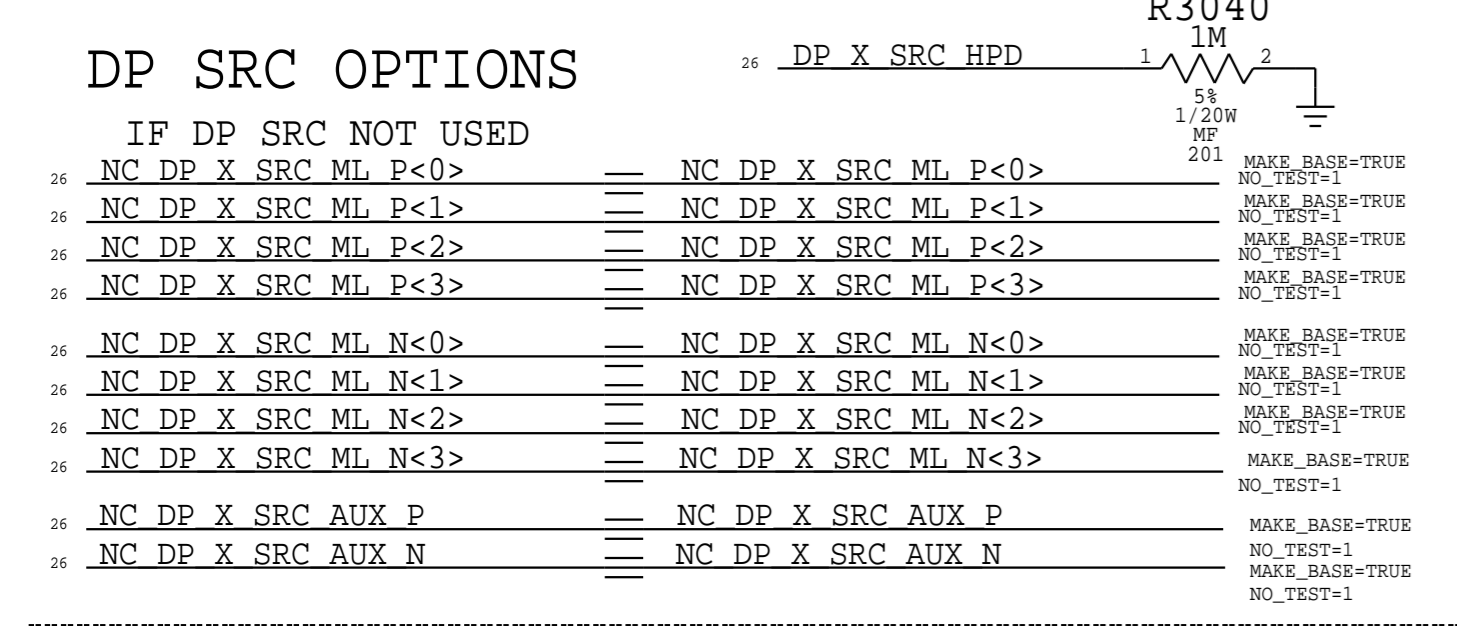
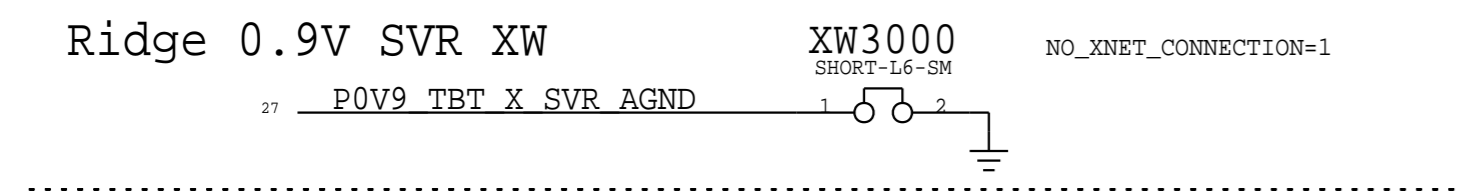
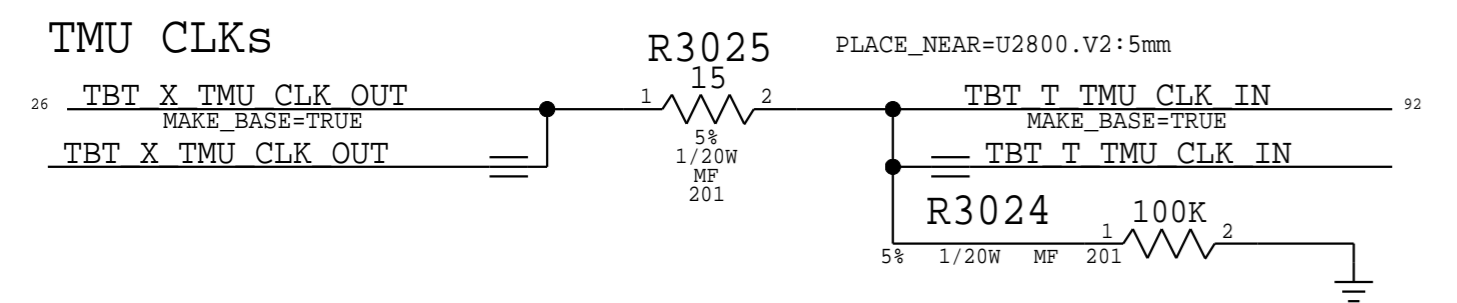
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 11V ALL RIGHTS RESERVED

BOM_COST_GROUP=TBT



| | | | |
|---|--|----------------------|-------------|
| SYNC_MASTER=779_0REG | | SYNC_DATE=09/09/2015 | |
| PAGE TITLE | | | |
| | | DRAWING NUMBER | 51-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2 NOT TO REPRODUCE OR COPY IT 3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4 ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 29 OF 145 |
| | | SHEET | 27 OF 119 |

BOM_COST_GROUP=TBT



USB-C Support

PAGE TITLE

Apple Inc.

DRWING NUMBER: 051-00777

REVISION: 9.0.0

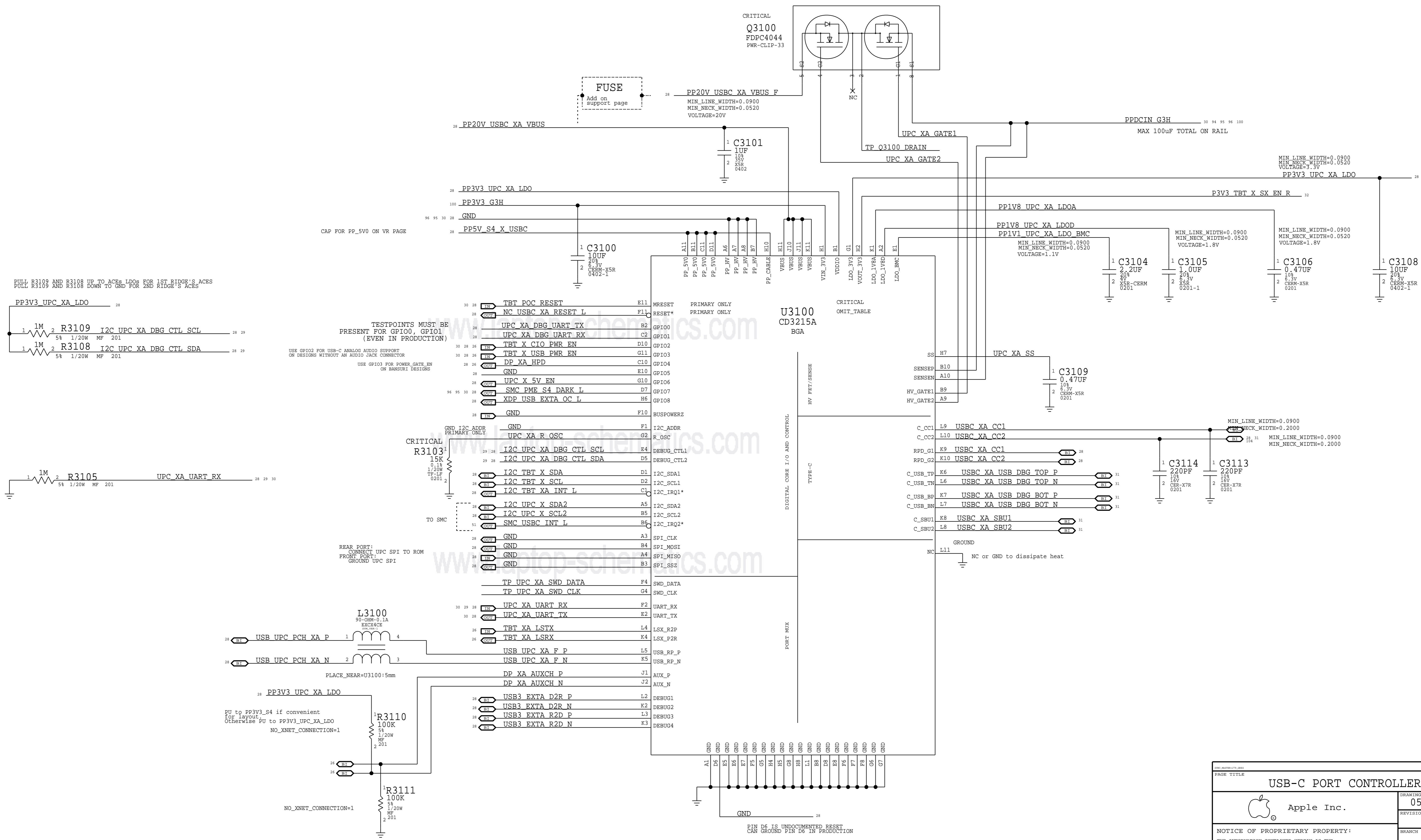
BRANCH: dvt-fab09-0

PAGE: 30 OF 145

SHEET: 28 OF 119

NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED

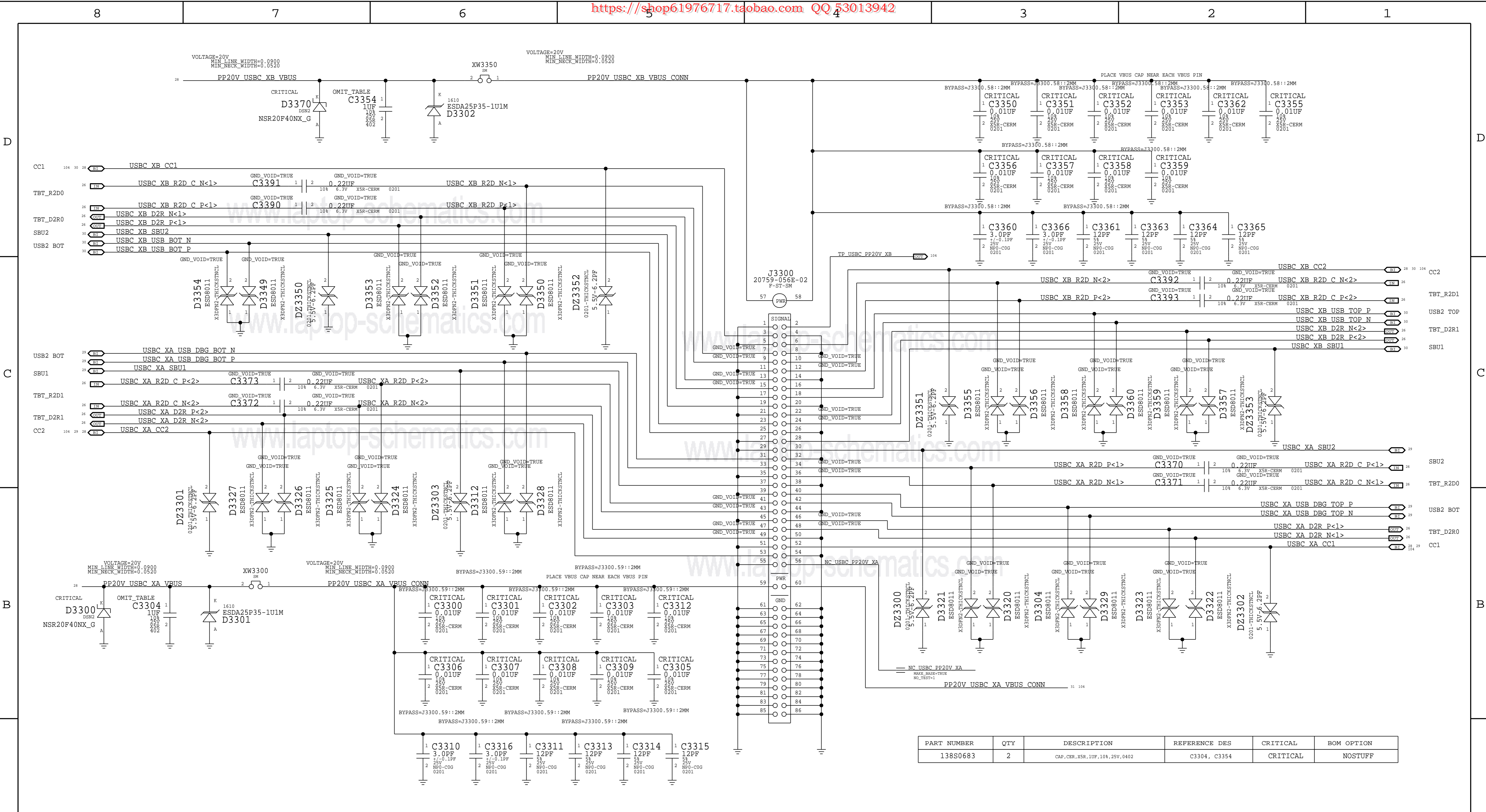
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



| | | |
|---|----------------|-------------|
| PAGE TITLE | | |
| USB-C PORT CONTROLLER A | | |
| | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 31 OF 145 |
| | SHEET | 29 OF 119 |

BOM_COST_GROUP=USB-C

PIN D6 IS UNDOCUMENTED RESET CAN GROUND PIN D6 IN PRODUCTION



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|------------------------------|---------------|----------|------------|
| 138S0683 | 2 | CAP,CER,XSR,1UF,10%,25V,0402 | C3304, C3354 | CRITICAL | NOSTUFF |

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C CONNECTOR A

Apple Inc.

| | | | |
|----------------|-------------|-----|---|
| DRAWING NUMBER | 051-00777 | STR | D |
| REVISION | 9.0.0 | | |
| BRANCH | dvt-fab09-0 | | |
| PAGE | 33 OF 145 | | |
| SHEET | 31 OF 119 | | |

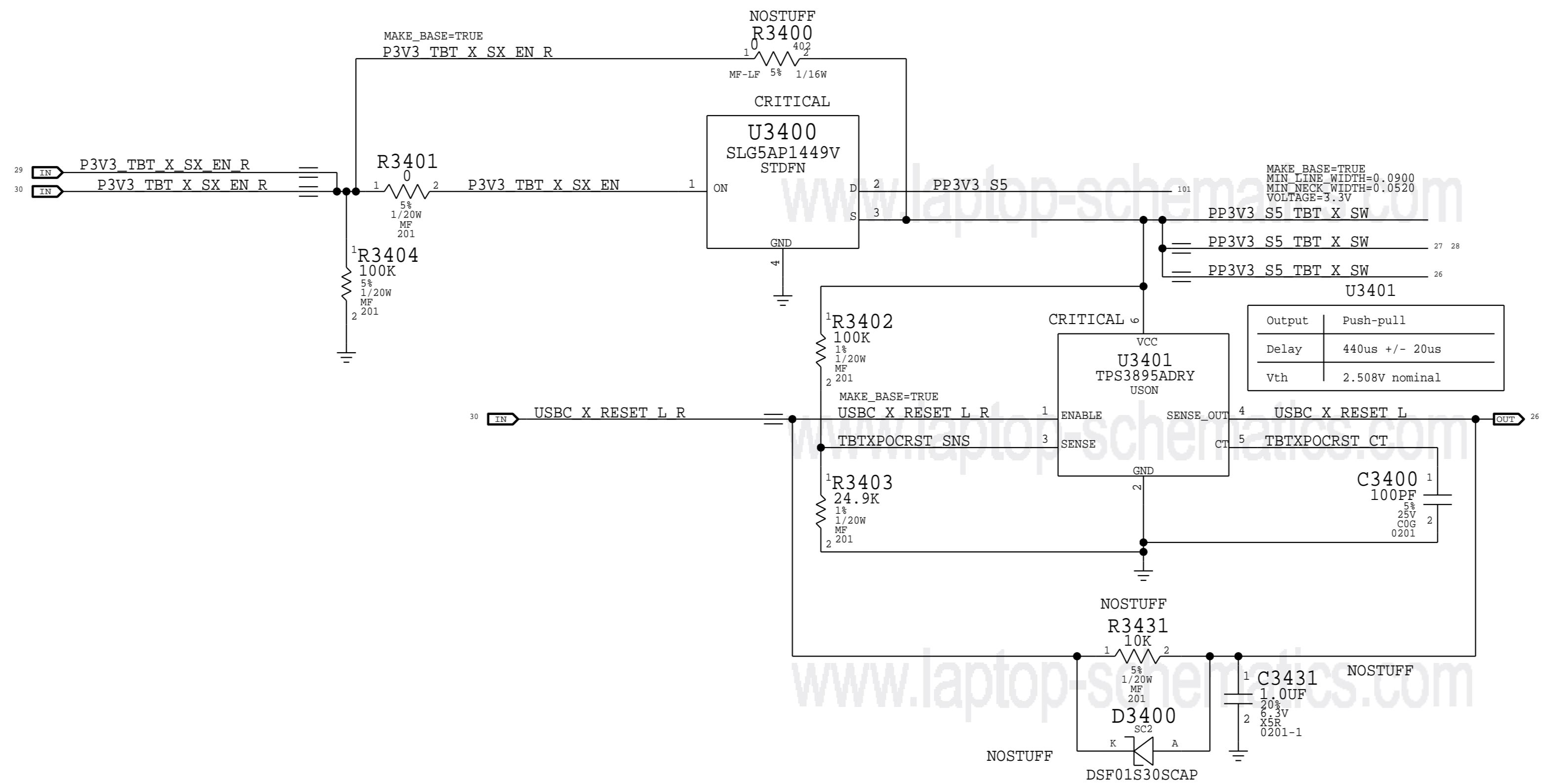
NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 1111 ALL RIGHTS RESERVED

BOM_COST_GROUP=USB-C

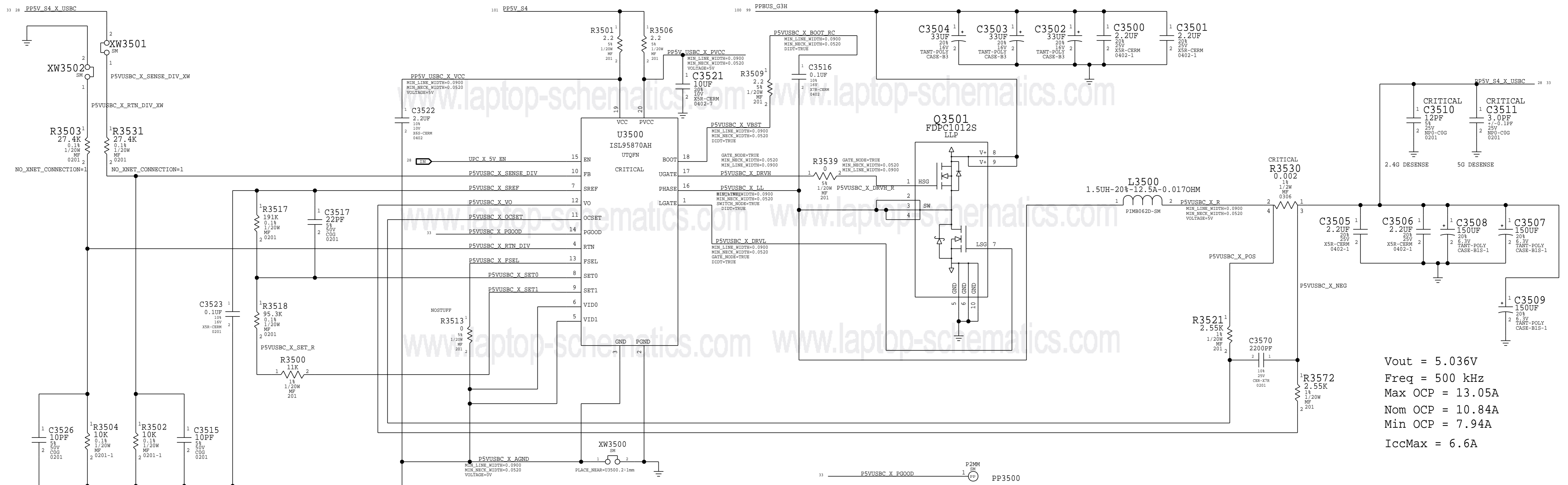
A

A

TBT X "POC" Power-up Reset



| | |
|---|-----------------------------|
| DESIGN: X502/DEV_MLB_U | |
| LAST CHANGE: Wed Feb 18 17:12:24 2015 | |
| PAGE TITLE | |
| USB-C CONNECTOR B | |
| | DRAWING NUMBER 051-00777 |
| | REVISION 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH dvt-fab09-0 |
| | PAGE 34 OF 145 |
| | SHEET 32 OF 119 |



Vout = 5.036V
 Freq = 500 kHz
 Max OCP = 13.05A
 Nom OCP = 10.84A
 Min OCP = 7.94A
 IccMax = 6.6A

| | | | |
|---|--|------------------|------|
| PAGE TITLE | | TBT 5V REGULATOR | |
| DRAWING NUMBER | | 051-00777 | SIZE |
| REVISION | | 9.0.0 | D |
| BRANCH | | dvt-fab09-0 | |
| PAGE | | 35 OF 145 | |
| SHEET | | 33 OF 119 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I I NOT TO REPRODUCE OR COPY IT I I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I V ALL RIGHTS RESERVED | | | |

D

D

C

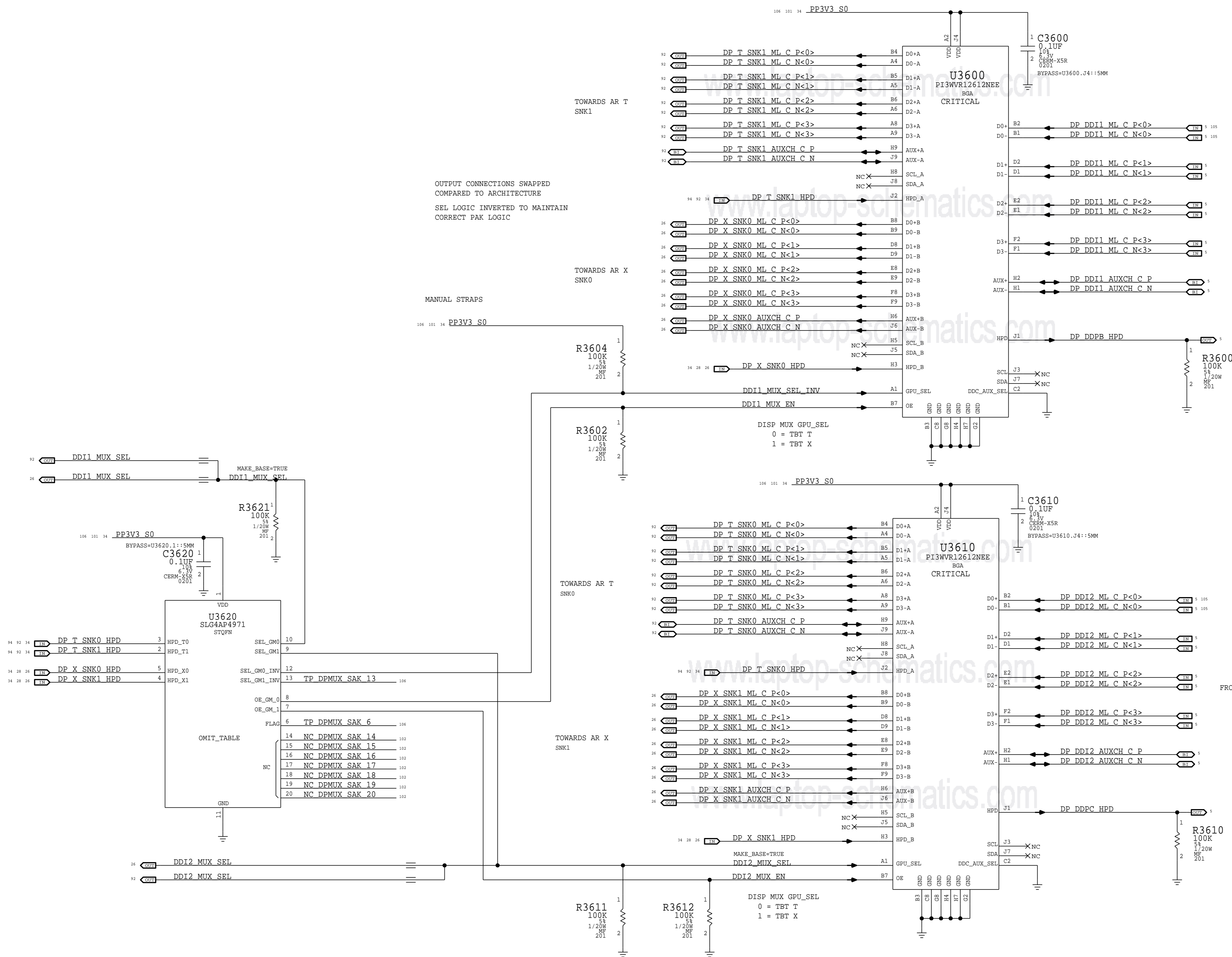
C

B

B

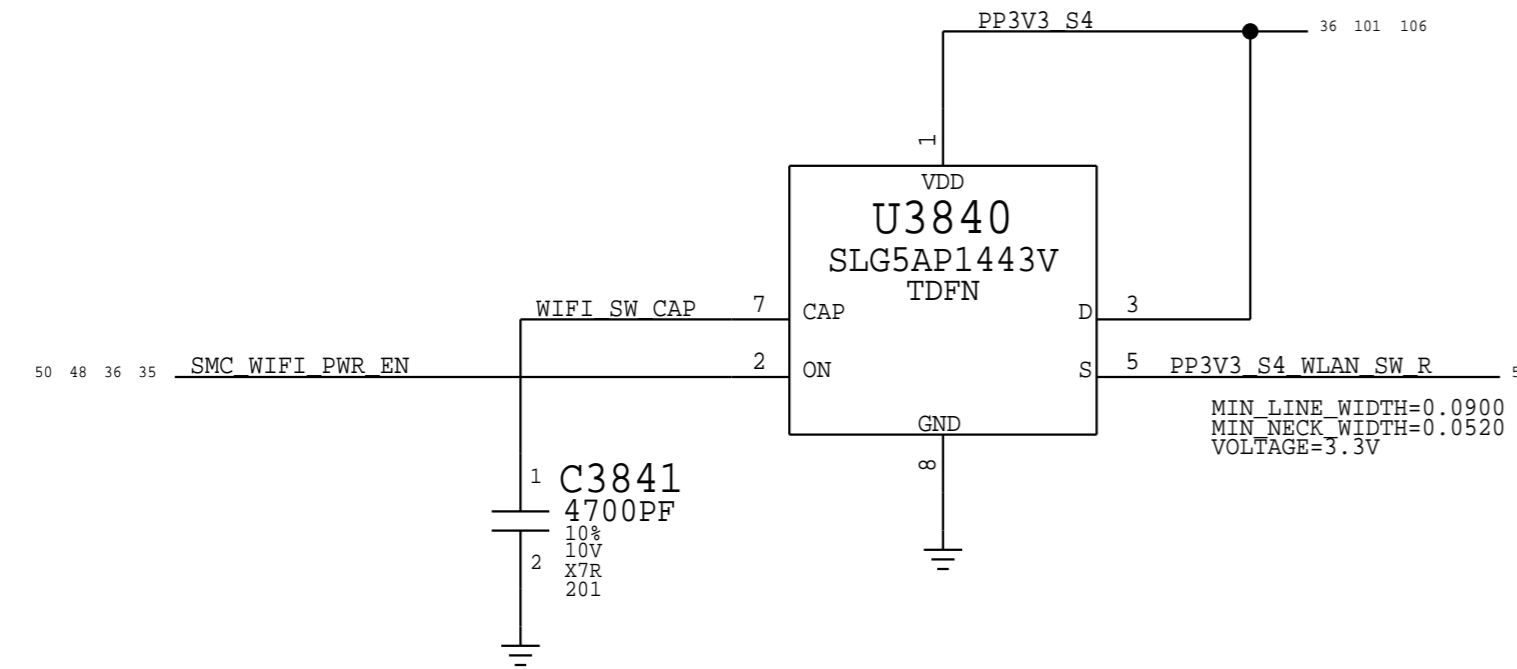
A

A



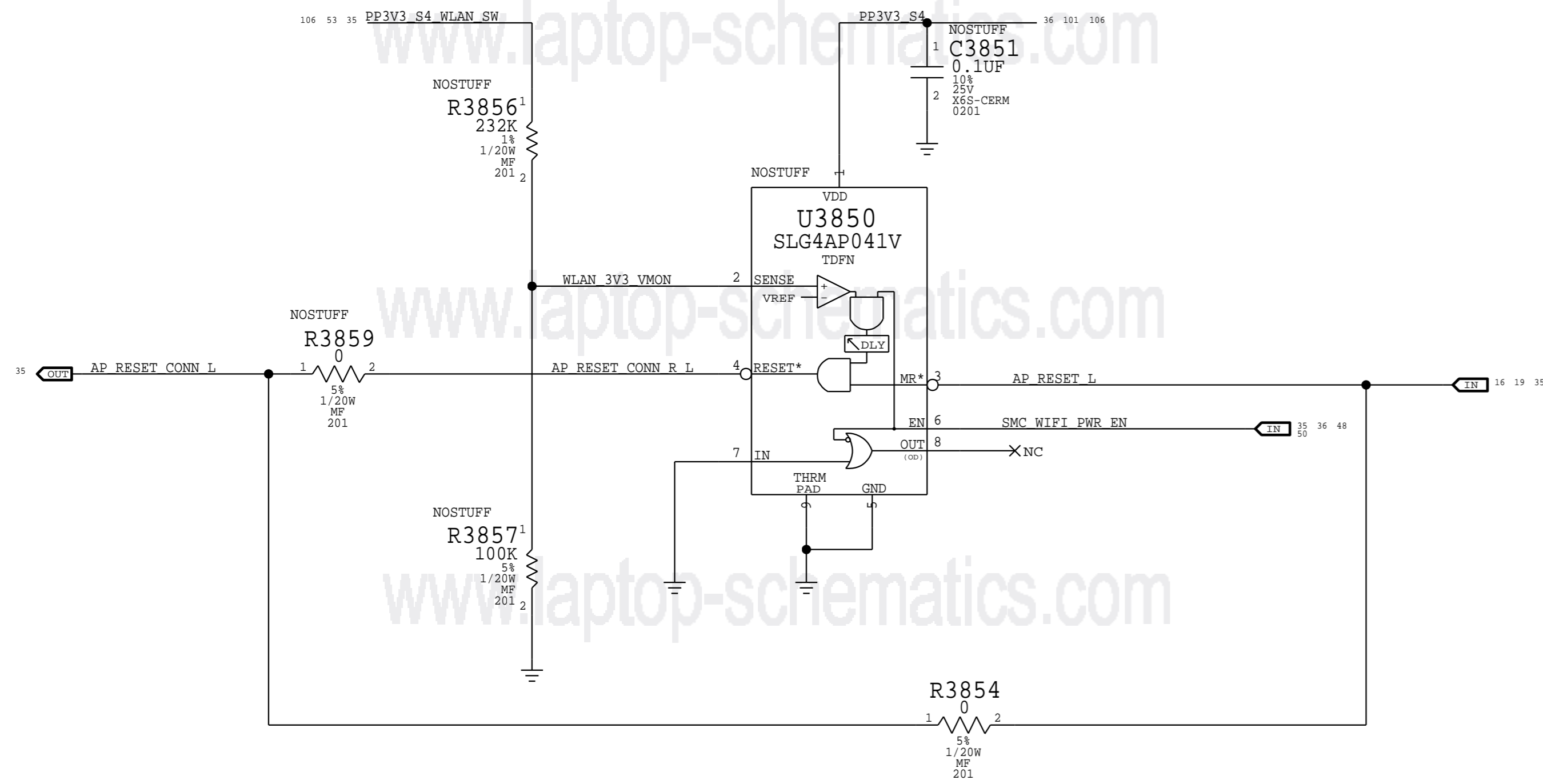
| | | | |
|---|--|-----------------------------|-----------------------|
| Display Mux | | DRAWING NUMBER 051-00777 | SIZE D |
| Apple Inc. | | REVISION 9.0.0 | BRANCH dvt-fab09-0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | | PAGE 36 OF 145 | SHEET 34 OF 119 |
| | | BOM_COST_GROUP=GRAPHICS | |

WLAN Power Switch

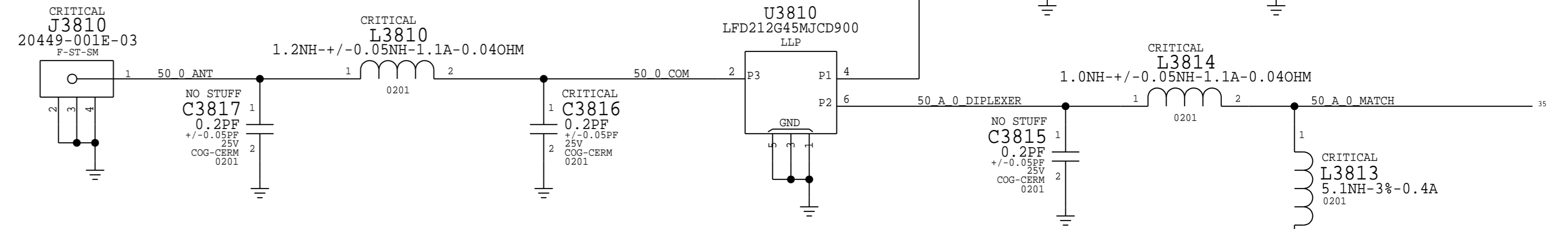


Supervisor & CLKREQ# Isolation

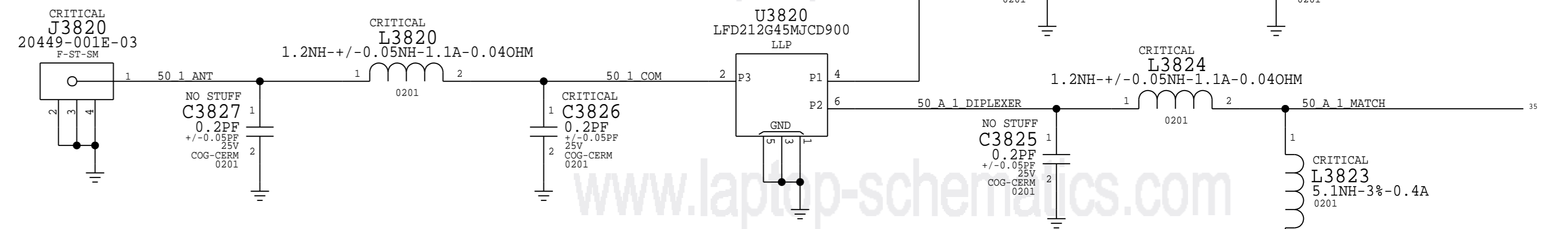
Delay = 130ms +/- 20%



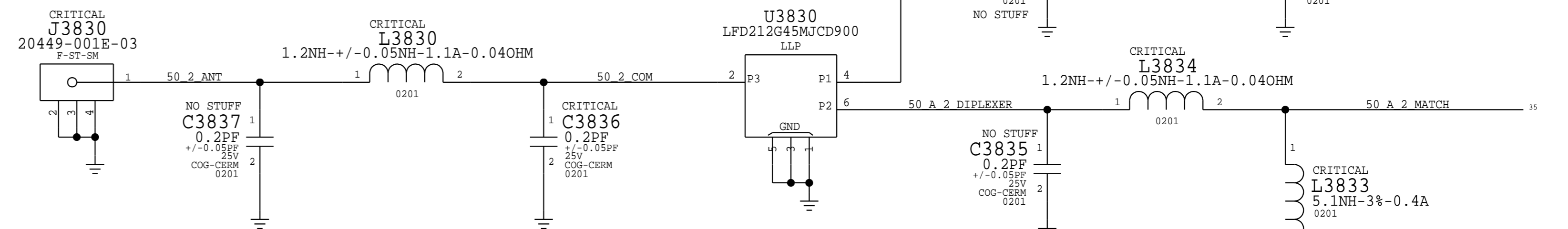
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING

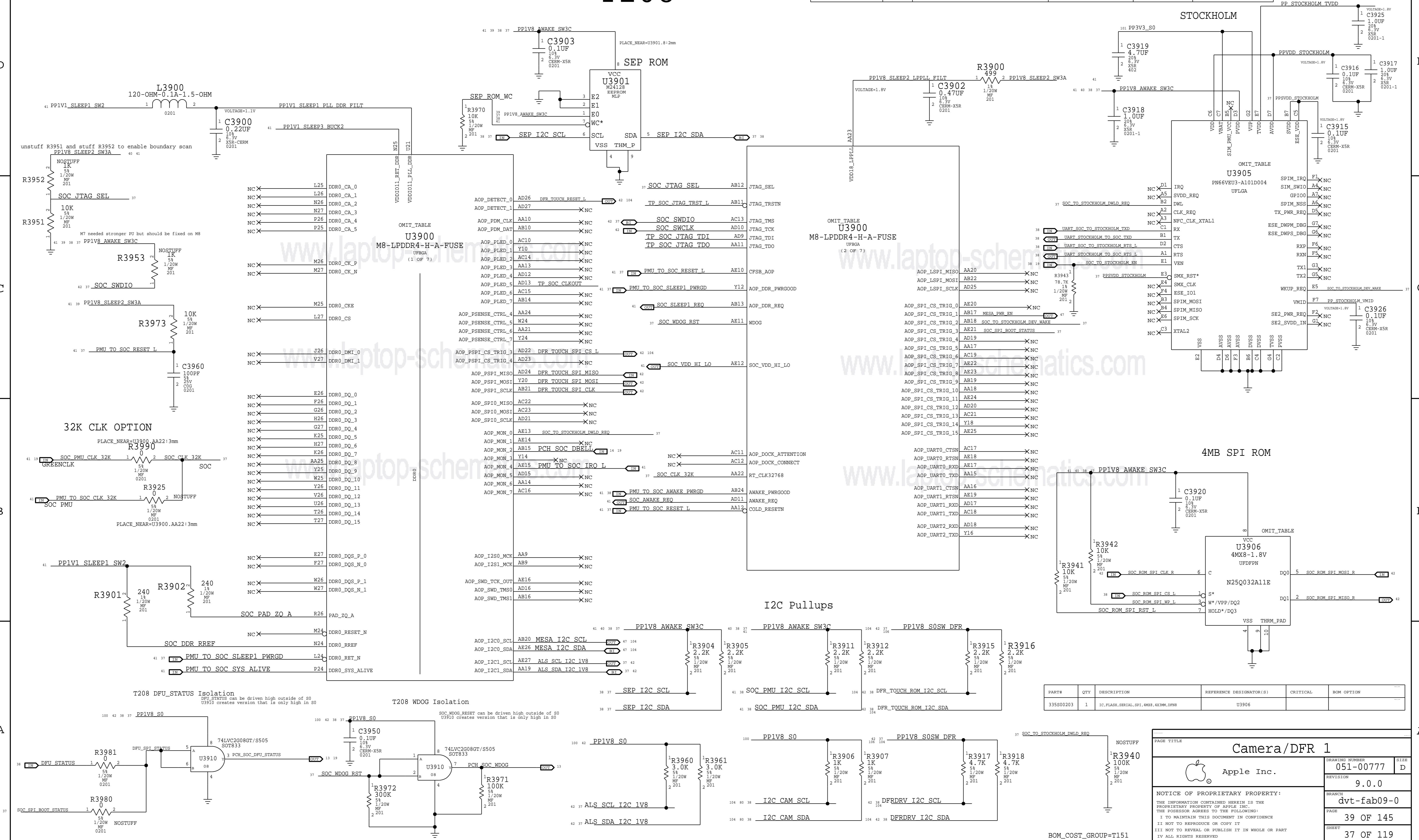


| | | | | | |
|---|--|---------------|-------------|------|-----------|
| WIFI/BT: MODULE 2 | | DRWING NUMBER | 051-00777 | STEP | D |
| Apple Inc. | | REVISION | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 | PAGE | 38 OF 145 |
| | | SHEET | 36 OF 119 | | |

T208

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--|---------------|----------|------------|
| 343800135 | 1 | IC,M8+512MB 20NM DDR,A12,S,S,CK,BGA700 | U3900 | CRITICAL | |

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------|---------------|----------|------------|
| 338800147 | 1 | IC,RTM2,DEV,PN549A1,P61D0 | U3905 | CRITICAL | SE:DEV |
| 338800097 | 1 | IC,RTM2,MP,PN549A1,P61D0 | U3905 | CRITICAL | SE:PROD |



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|-----------|-----|-------------------------------------|-------------------------|----------|------------|
| 335800203 | 1 | IC,FLASH,SERIAL,SPI,4MX8,4K3MM,DFNS | U3906 | | |

Camera/DFR 1

Apple Inc.

DRAGGING NUMBER: 051-00777

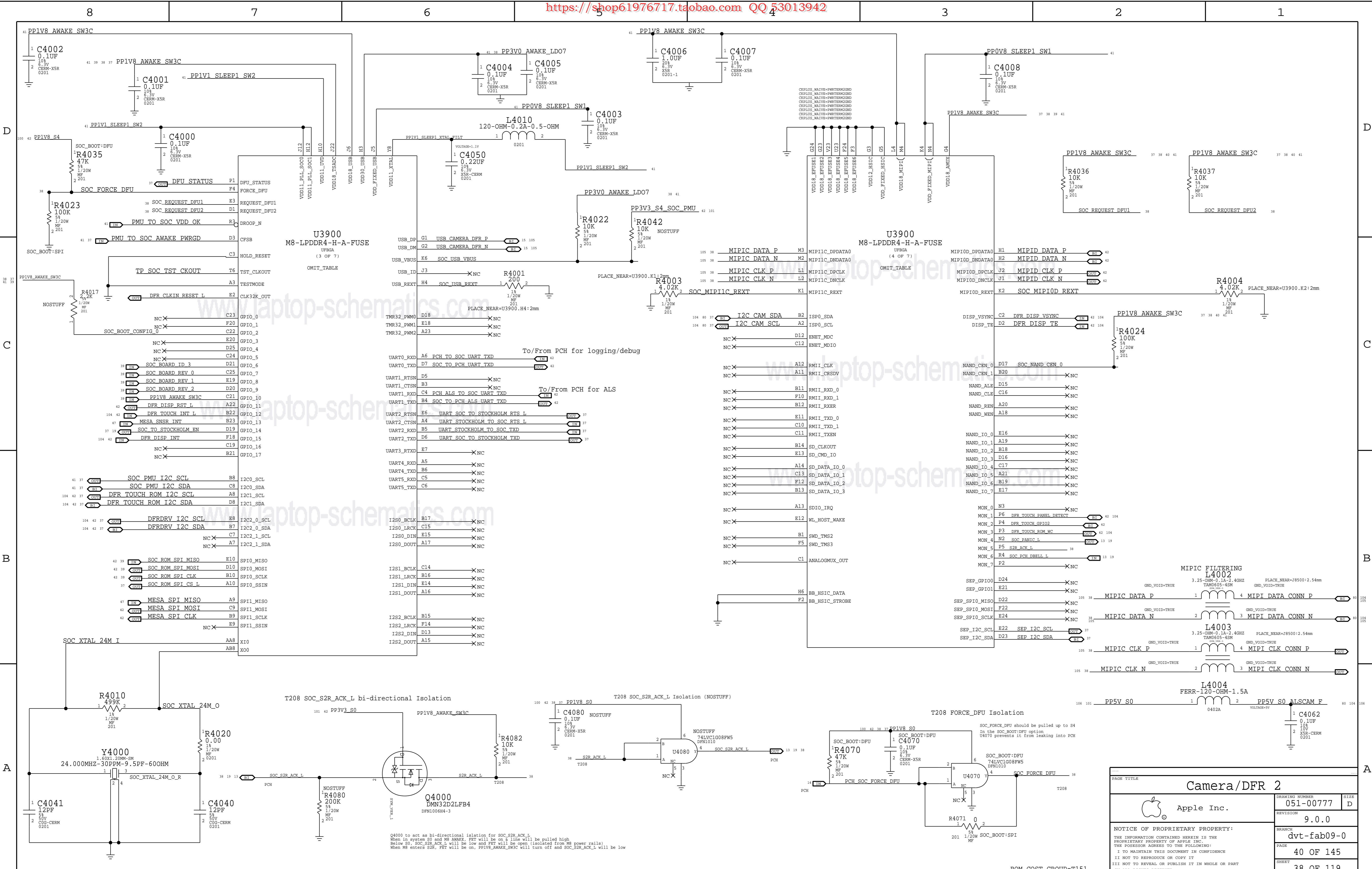
REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 39 OF 145

SHEET: 37 OF 119

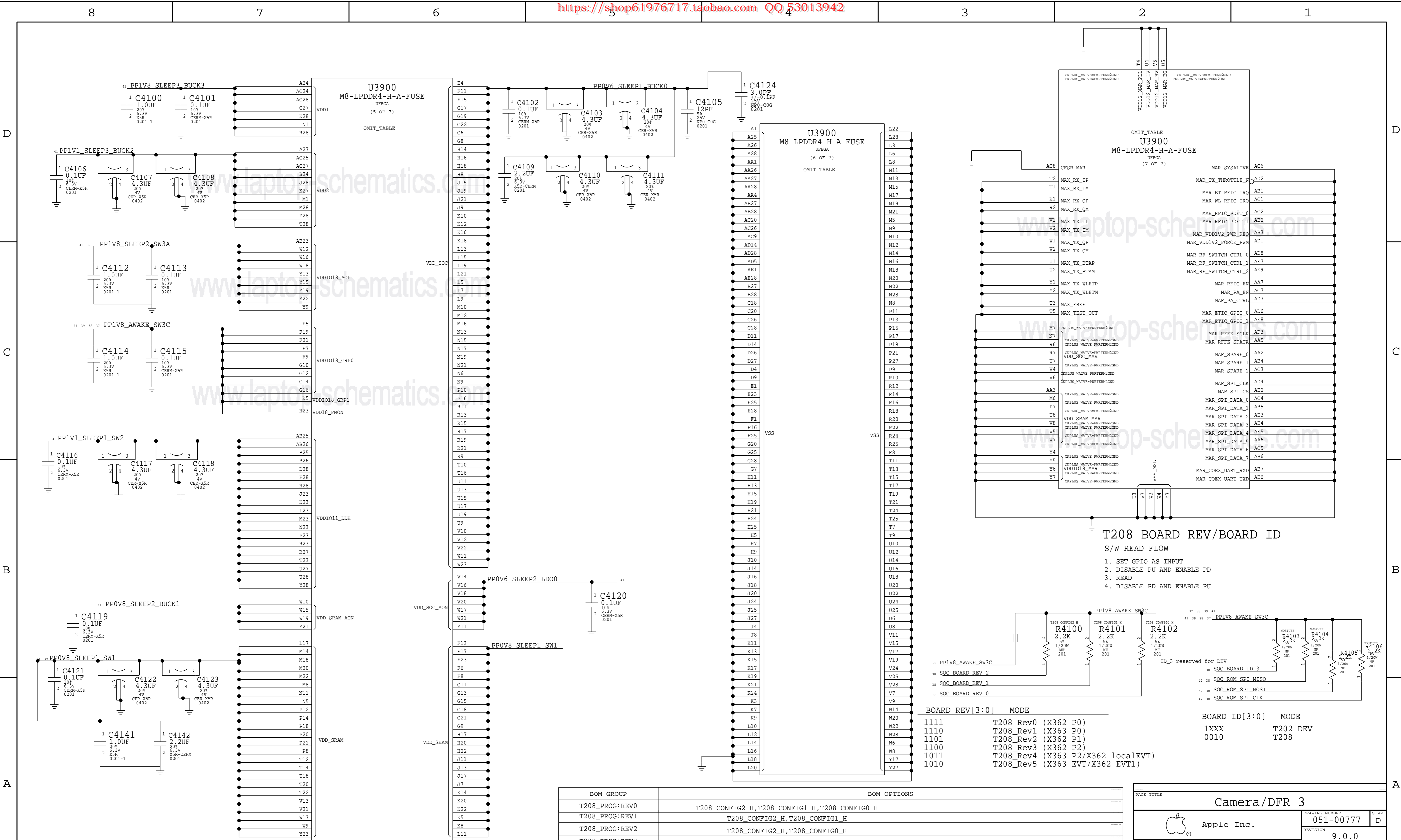
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED



| | | | |
|----------------|--|--------------|-----|
| PAGE TITLE | | Camera/DFR 2 | |
| DRAWING NUMBER | | 051-00777 | STR |
| REVISION | | 9.0.0 | D |
| BRANCH | | dvt-fab09-0 | |
| PAGE | | 40 OF 145 | |
| SHEET | | 38 OF 119 | |

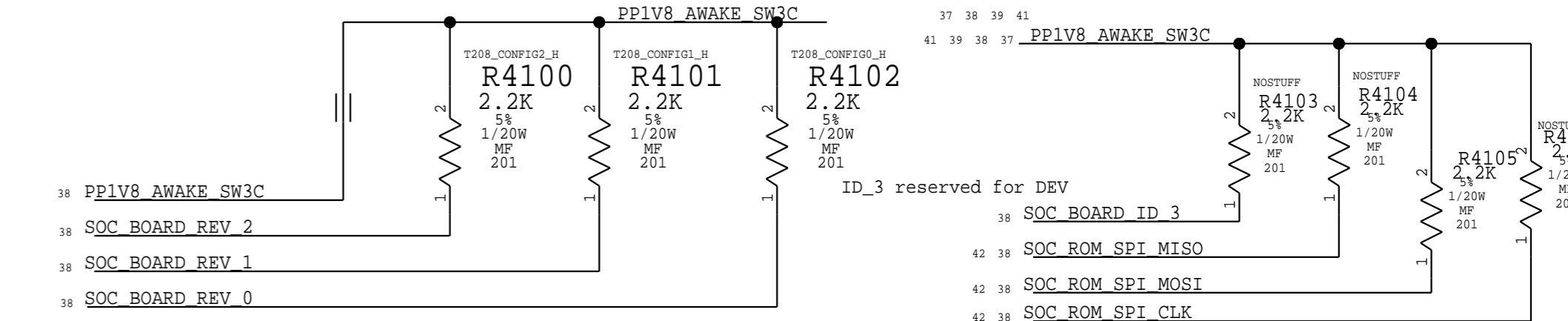
NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 1111 ALL RIGHTS RESERVED

BOM_COST_GROUP=T151



T208 BOARD REV/BOARD ID
S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



| BOARD REV[3:0] | MODE |
|----------------|-----------------------------------|
| 1111 | T208_Rev0 (X362 P0) |
| 1110 | T208_Rev1 (X363 P0) |
| 1101 | T208_Rev2 (X362 P1) |
| 1100 | T208_Rev3 (X362 P2) |
| 1011 | T208_Rev4 (X363 P2/X362 localEVT) |
| 1010 | T208_Rev5 (X363 EVT/X362 EVT1) |

| BOARD ID[3:0] | MODE |
|---------------|----------|
| 1XXX | T202 DEV |
| 0010 | T208 |

| BOM GROUP | BOM OPTIONS |
|----------------|--|
| T208_PROG:REV0 | T208_CONFIG2_H, T208_CONFIG1_H, T208_CONFIG0_H |
| T208_PROG:REV1 | T208_CONFIG2_H, T208_CONFIG1_H |
| T208_PROG:REV2 | T208_CONFIG2_H, T208_CONFIG0_H |
| T208_PROG:REV3 | T208_CONFIG2_H |
| T208_PROG:REV4 | T208_CONFIG1_H, T208_CONFIG0_H |
| T208_PROG:REV5 | T208_CONFIG1_H |

PAGE TITLE: **Camera/DFR 3**

Apple Inc.

BRANCH: dvt-fab09-0

NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 111 NOT TO REPRODUCE OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED

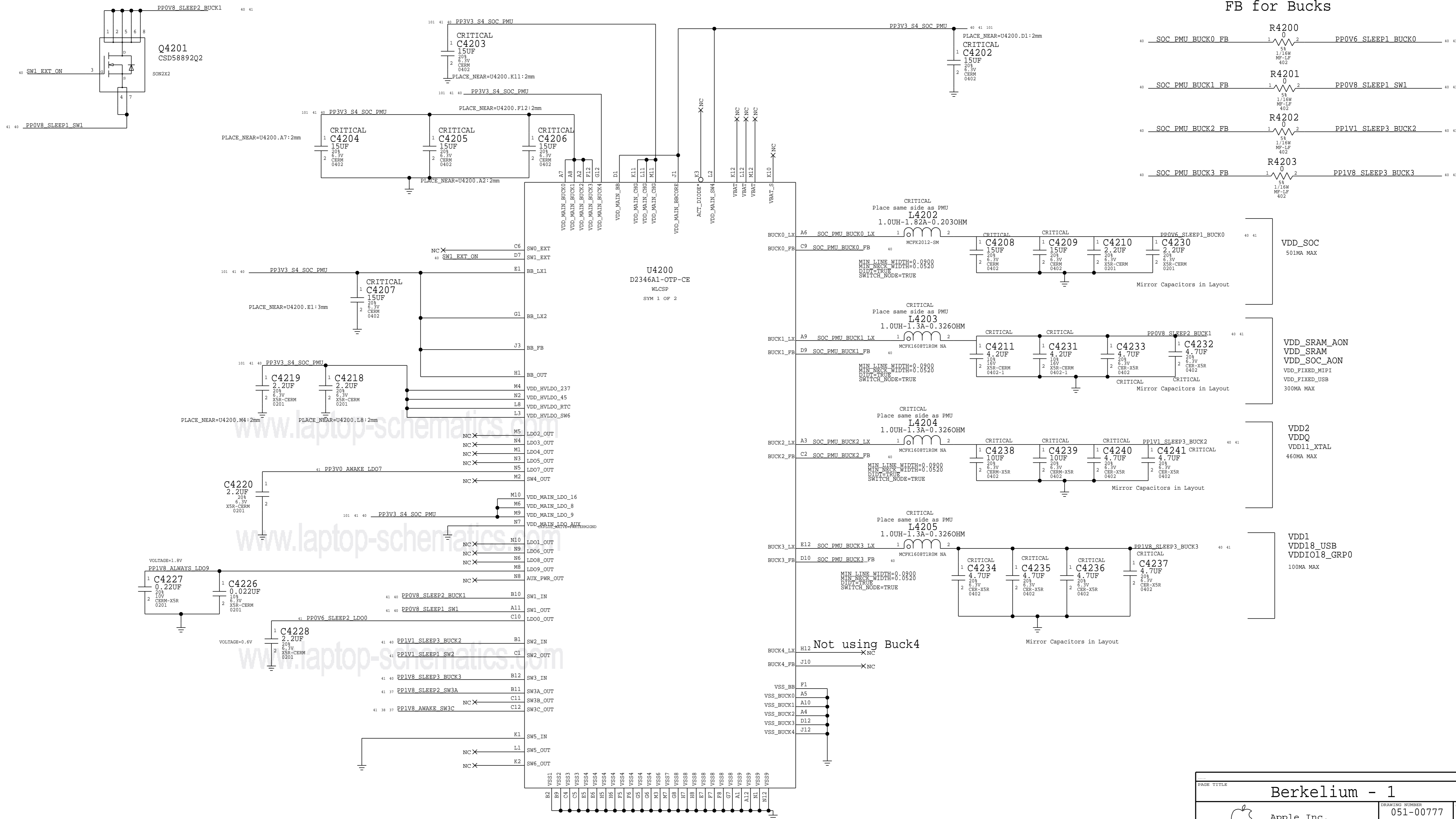
BRANCH: dvt-fab09-0

PAGE: 41 OF 145

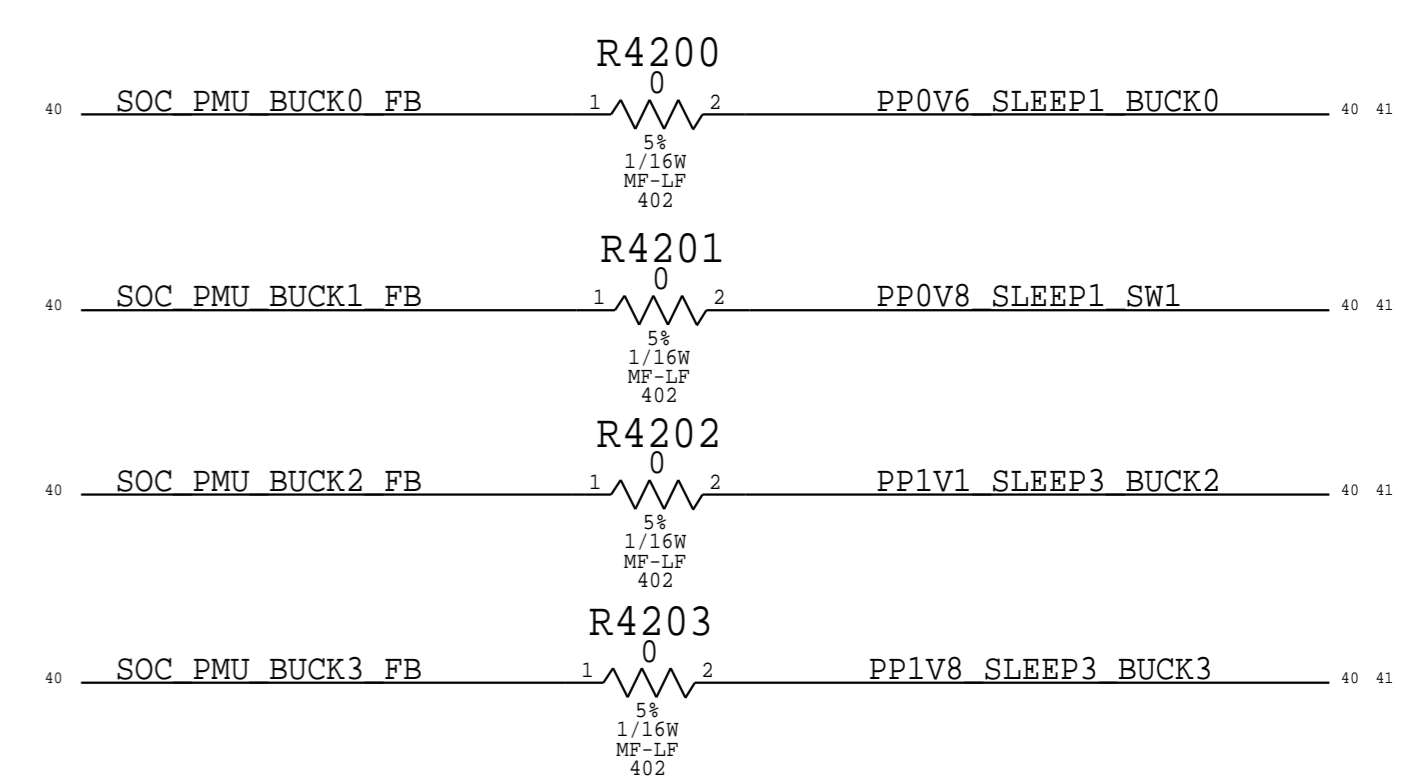
SHEET: 39 OF 119

BOM_COST_GROUP=T151

Berkelium



FB for Bucks



VDD_SOC
501MA MAX

VDD_SRAM_AON
VDD_SOC_AON
VDD_FIXED_MIPI
VDD_FIXED_USB
300MA MAX

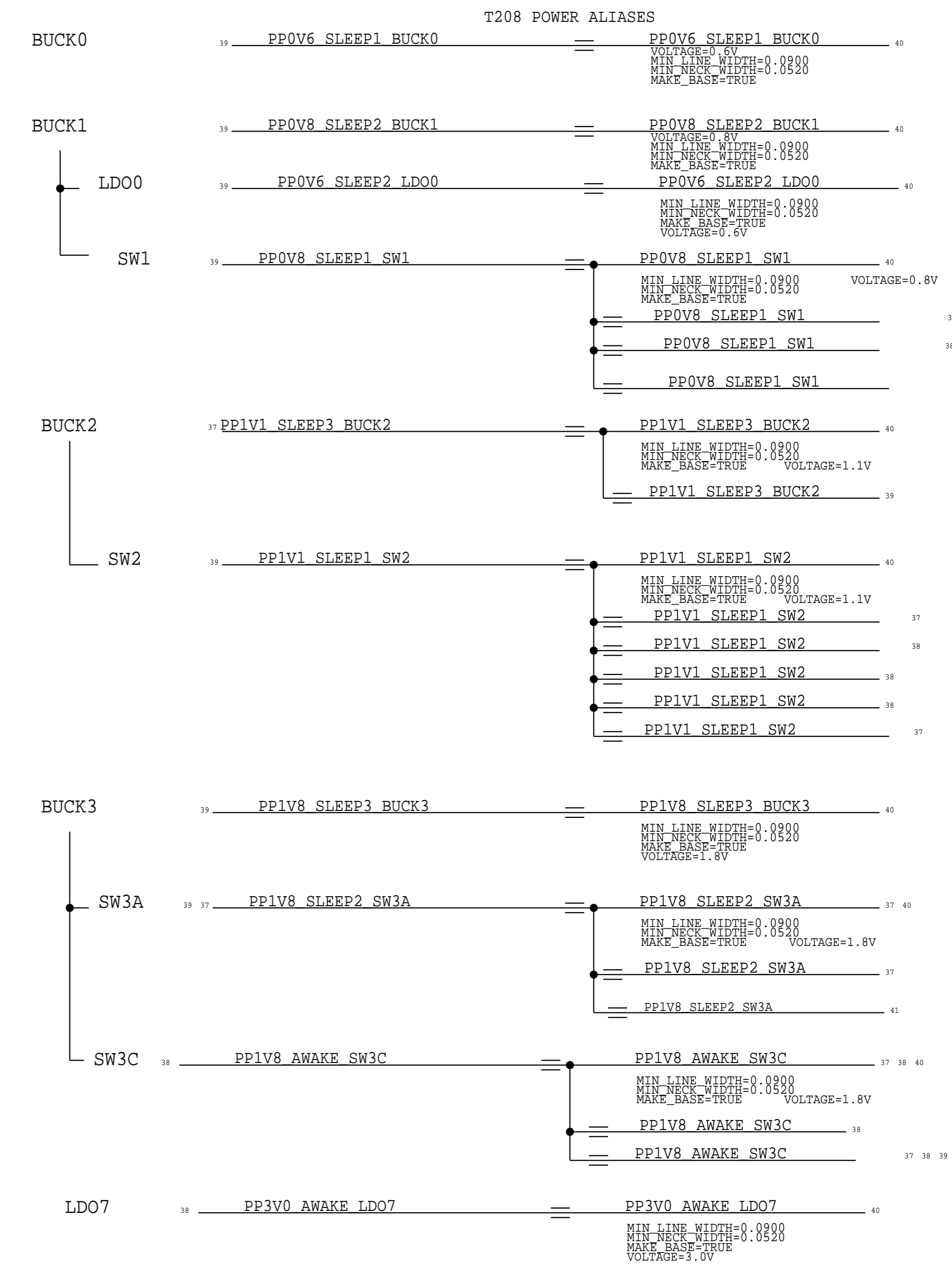
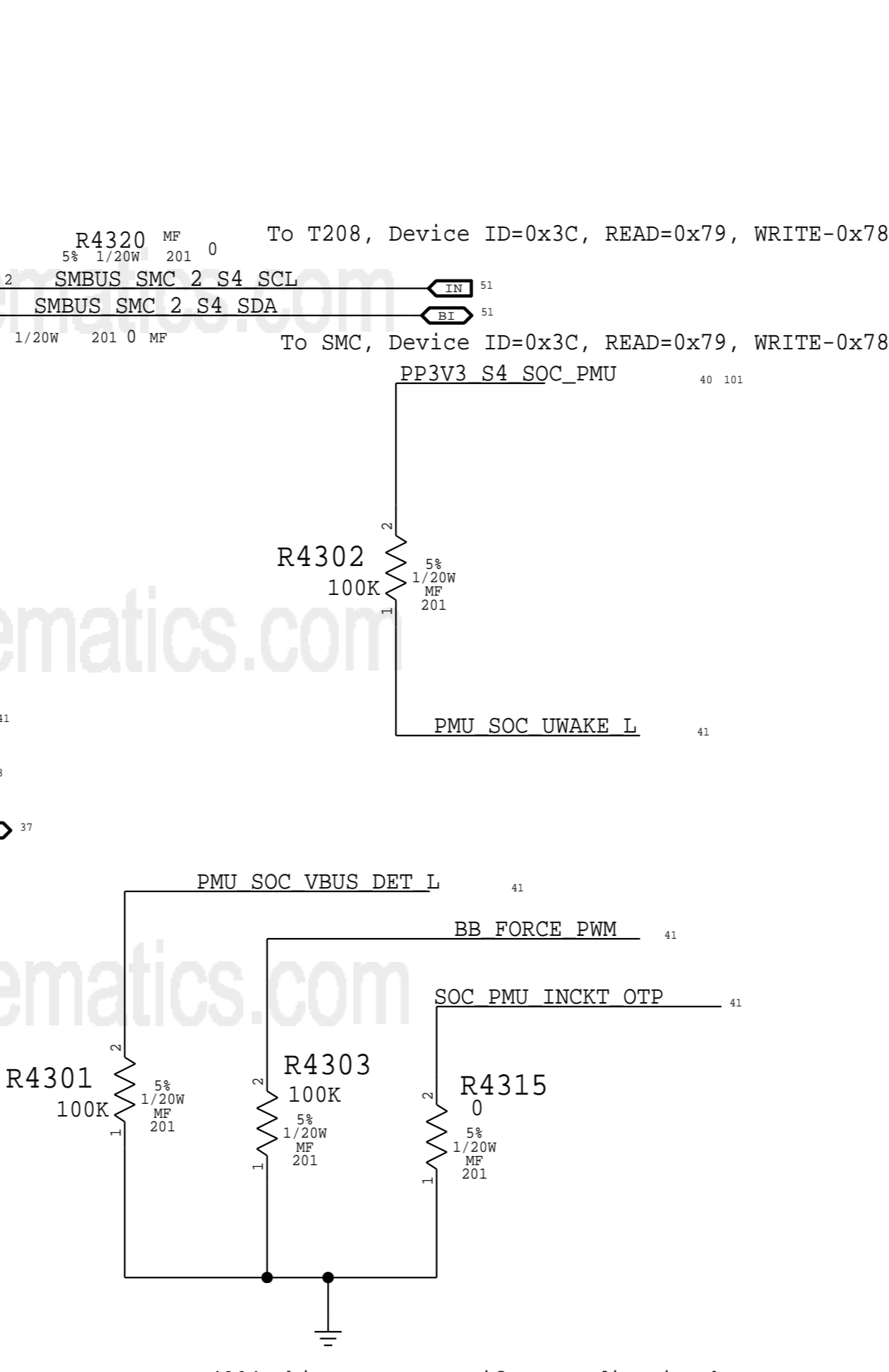
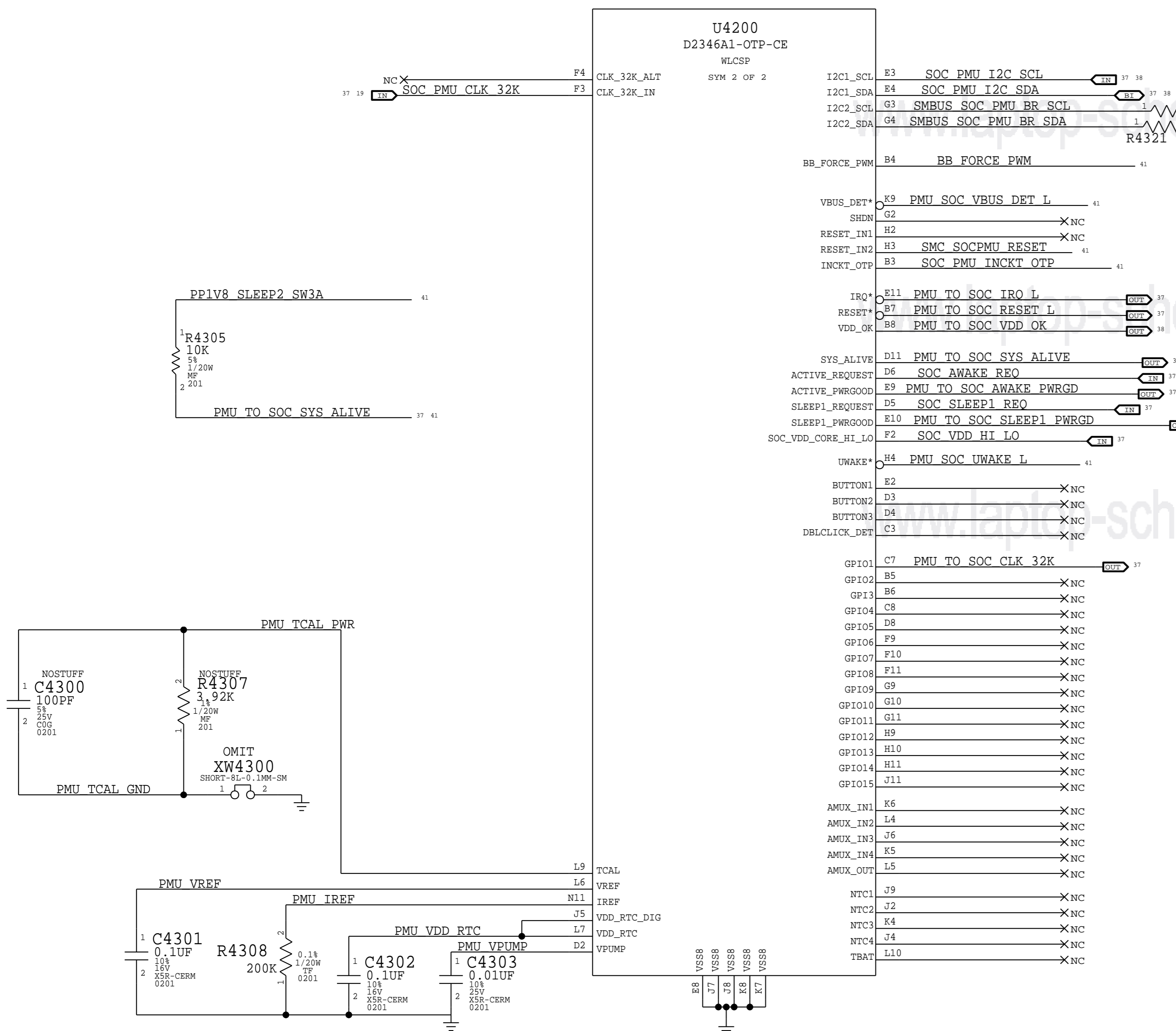
VDD2
VDDQ
VDDI1_XTAL
460MA MAX

VDDI1
VDDI18_USB
VDDI18_GRP0
100MA MAX

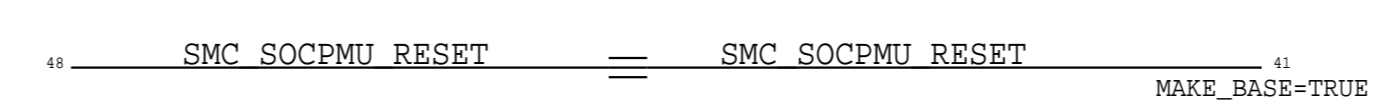
Not using Buck4

| | | |
|---|----------------|-----------|
| PAGE TITLE | | |
| Berkelium - 1 | | |
| | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: | | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | |
| 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | |
| 11 NOT TO REPRODUCE OR COPY IT | | |
| 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | |
| 1V ALL RIGHTS RESERVED | | |
| BRANCH | dvt-fab09-0 | |
| PAGE | 42 OF 145 | |
| SHEET | 40 OF 119 | |

Berkelium - 2

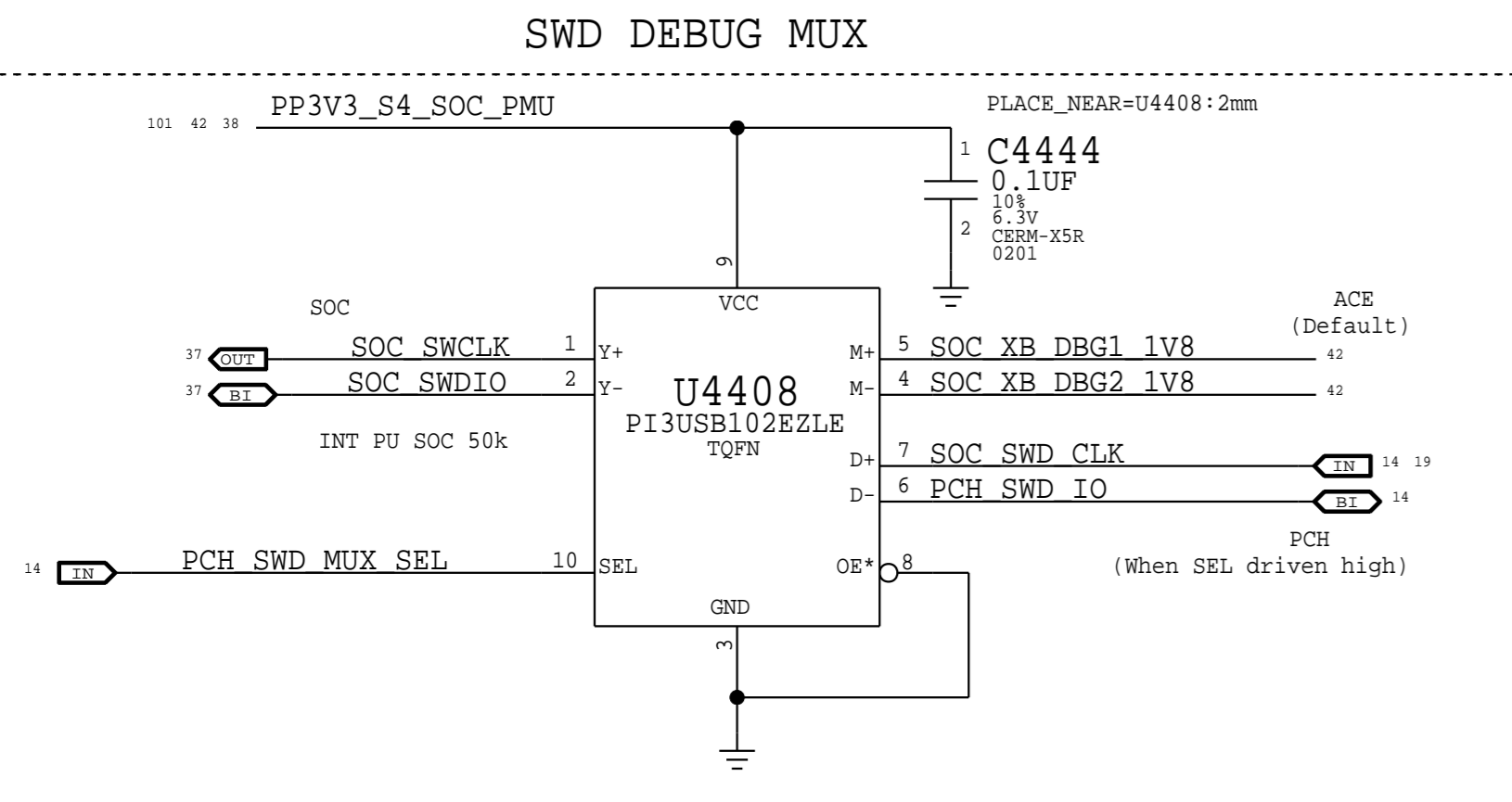
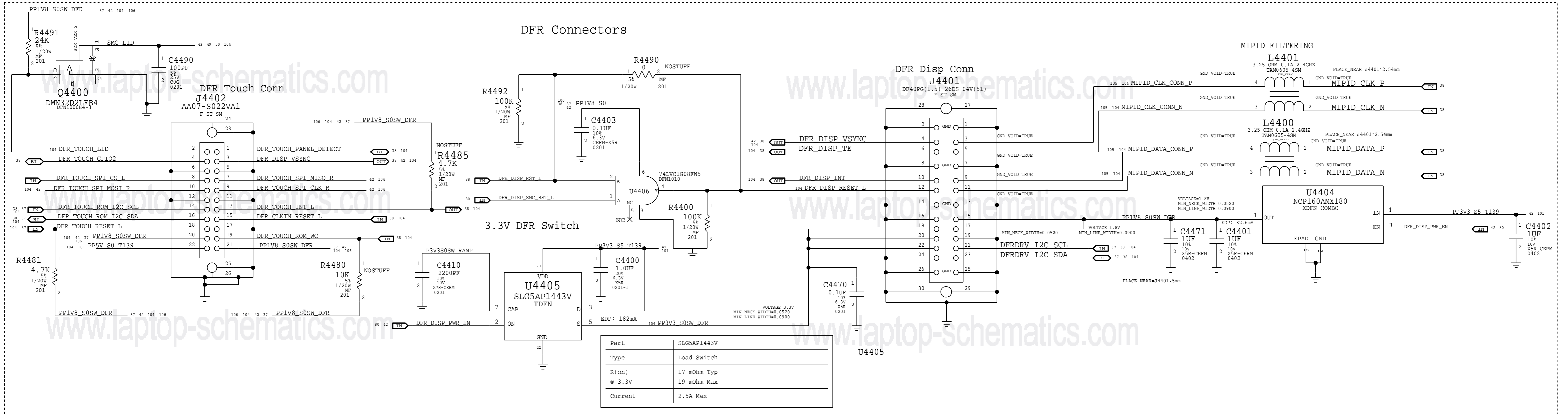


Signal Aliases



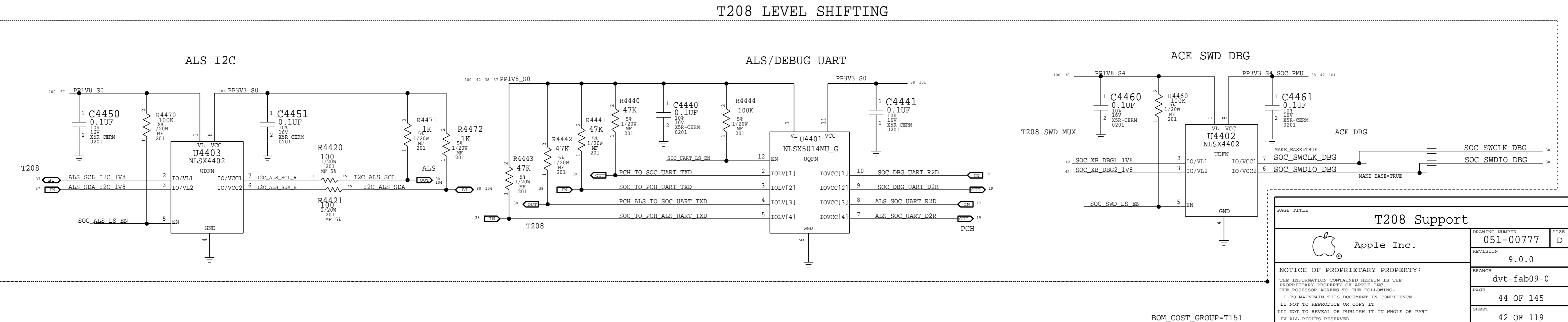
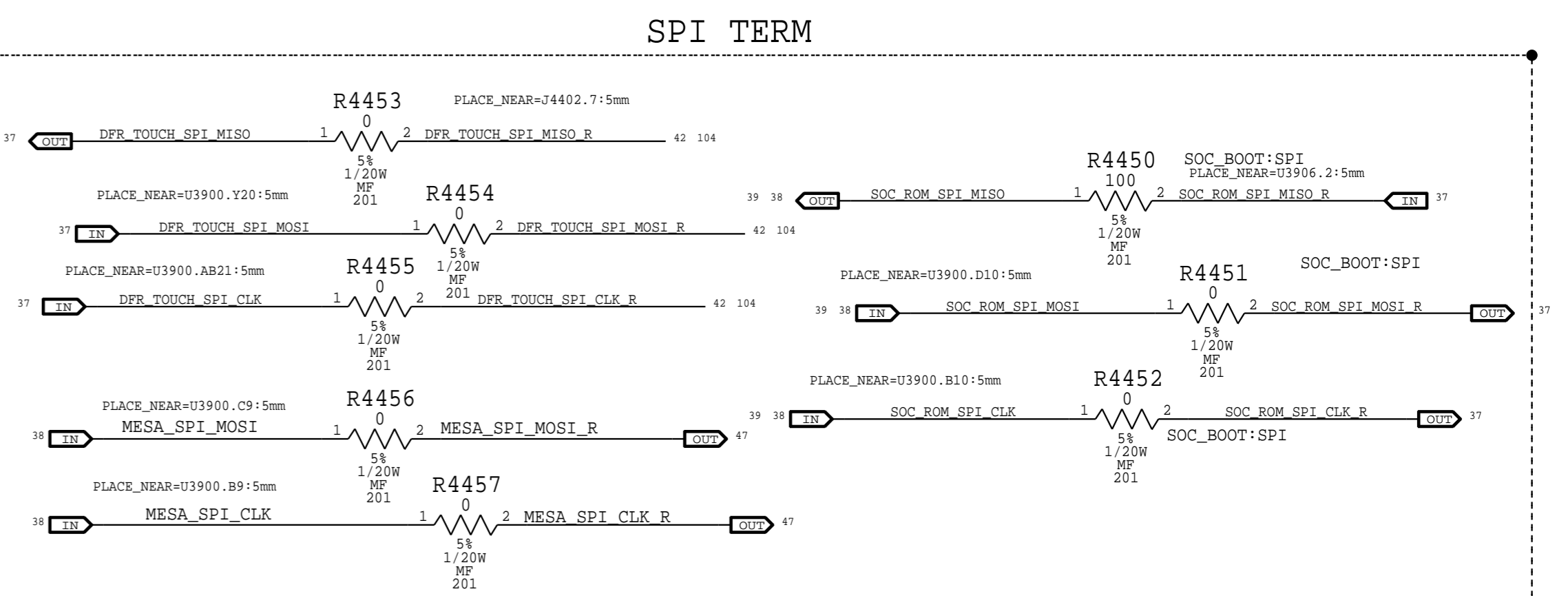
| | | |
|--|----------------|-----------|
| PAGE TITLE | | |
| Berkelium - 2 | | |
| | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: | | |
| <small>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:</small> | | |
| <small>1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE</small> | | |
| <small>11 NOT TO REPRODUCE OR COPY IT</small> | | |
| <small>111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART</small> | | |
| <small>11 ALL RIGHTS RESERVED</small> | | |
| BRANCH | dvt-fab09-0 | |
| PAGE | 43 OF 145 | |
| SHEET | 41 OF 119 | |

T208 Support



T208 I2C Mapping

| Bus | Device | 7-bit Address | 8-bit Address | |
|-------|---------------|---------------------|---------------|---------|
| | | | Read | Write |
| AP0 | PMU | 0011110 (0x3C) | 0x79 | 0x78 |
| AP1 | Touch EEPROM | 1010000 (0x50) | 0xA1 | 0xA0 |
| AP2_0 | Tesla | 1010100 (0x4C) | 0x99 | 0x98 |
| AOP0 | Mesa EEPROM | 101000x (0x50/0x51) | 0xA1/A3 | 0xA0/A2 |
| AOP1 | ALS | 0111001 (0x39) | 0x73 | 0x72 |
| SEP | M34128 EEPROM | 1010001 (0x51) | 0xA3 | 0xA2 |



T208 Support

Apple Inc.

DRAWING NUMBER: 051-00777

REVISION: 9.0.0

BRANCH: dvt-fab09-0

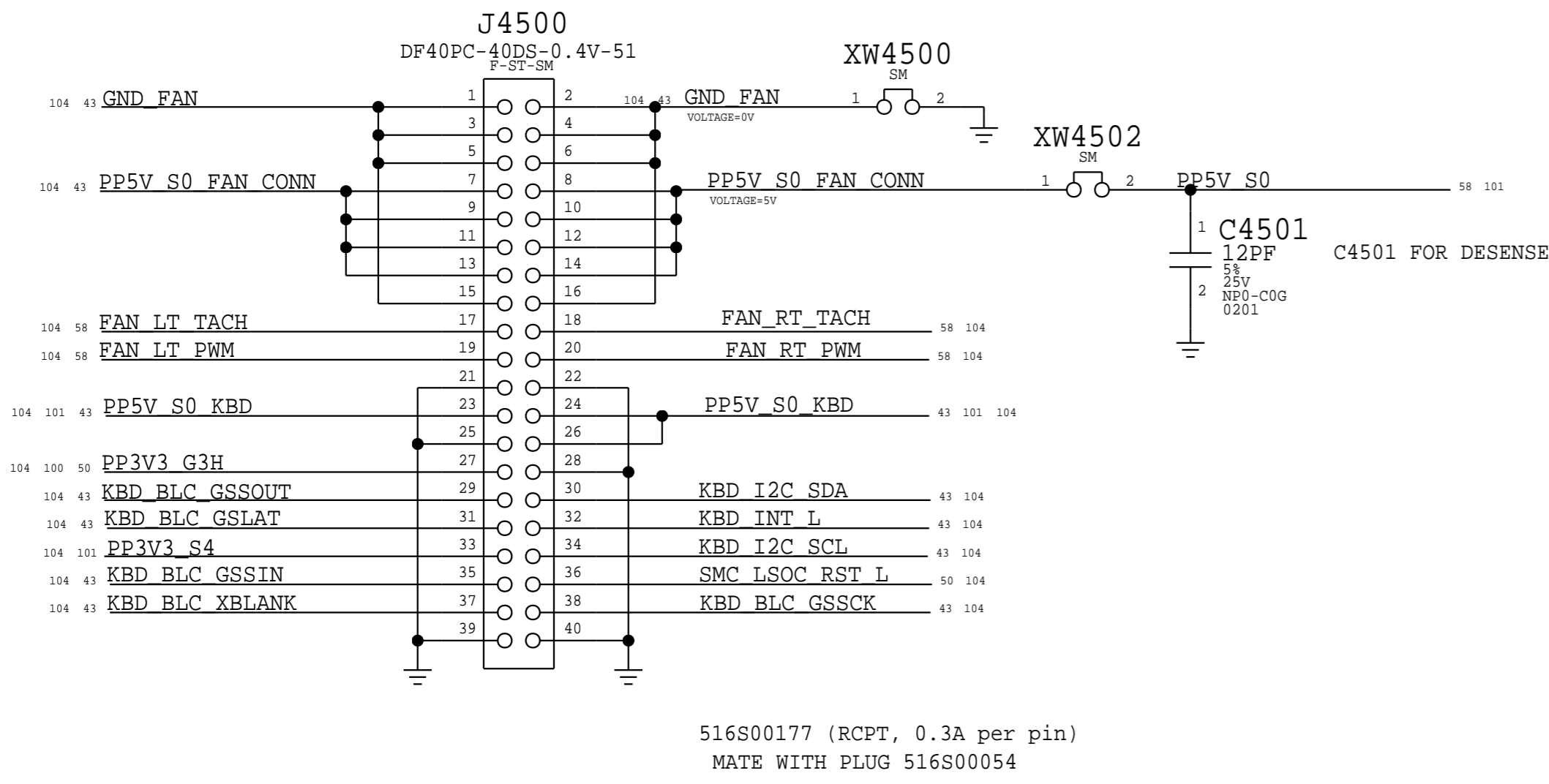
PAGE: 44 OF 145

SHEET: 42 OF 119

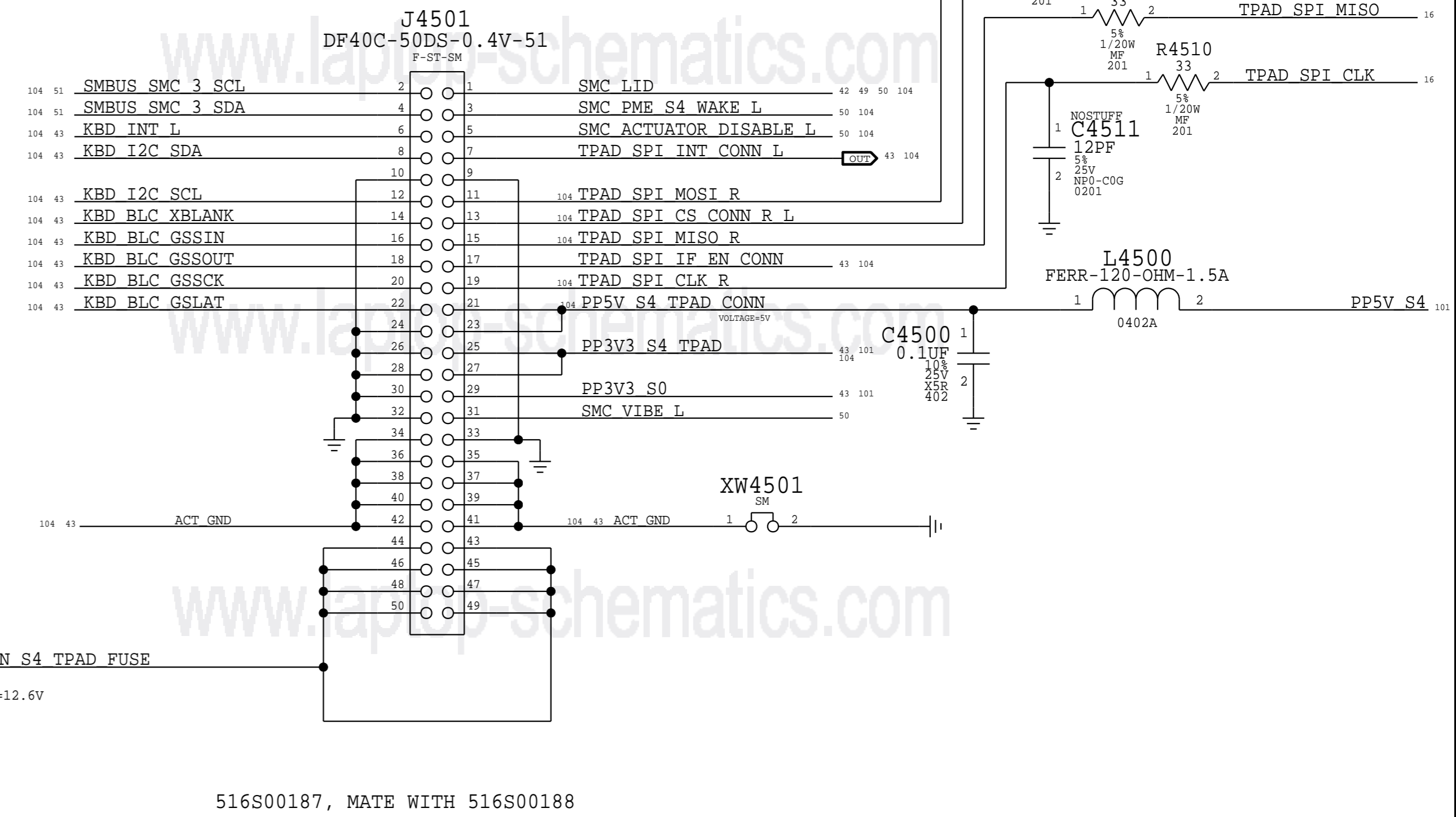
NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 1V ALL RIGHTS RESERVED

BOM_COST_GROUP=T151

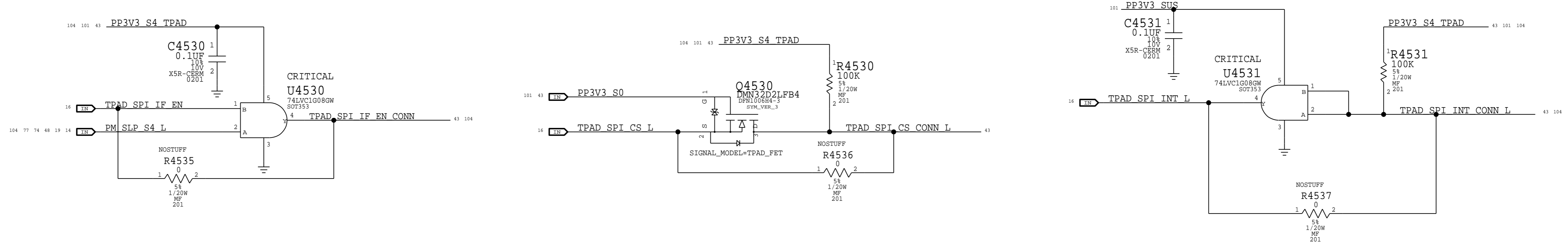
KBD CONNECTOR



TPAD CONNECTOR



TRACKPAD ISOLATION



| | | | |
|--|--|----------------------|-------------|
| EYNC_MASTER=79_GABN | | EYNC_DATE=11/21/2015 | |
| PAGE TITLE | | | |
| Connectors&ESD | | DRAWING NUMBER | 051-00777 |
| Apple Inc. | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 45 OF 145 |
| | | SHEET | 43 OF 119 |

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

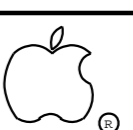
5

4

3

2

1

| | | | | |
|---|----------------|----------------------|-------------|---|
| SYNC_MASTER=J79_DAYU | | SYNC_DATE=05/26/2015 | | |
| PAGE TITLE | | | | |
| Empty | | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE | D |
| | REVISION | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 | |
| | | PAGE | 46 OF 145 | |
| | | SHEET | 44 OF 119 | |

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6


5

4

3

2

1

| | | | | |
|---|----------------|----------------------|-------------|---|
| SYNC_MASTER=J79_DAYU | | SYNC_DATE=05/26/2015 | | |
| PAGE TITLE | | | | |
| Empty | | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE | D |
| | REVISION | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 | |
| | | PAGE | 47 OF 145 | |
| | | SHEET | 45 OF 119 | |

8

7

6

5

4

3

2

1

D

D

C


C

B

B

A

A

| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=J79_DAYU | | SYNC_DATE=05/12/2015 | |
| PAGE TITLE | | | |
| Empty | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 48 OF 145 |
| | | SHEET | 46 OF 119 |

8

7

6

5

4

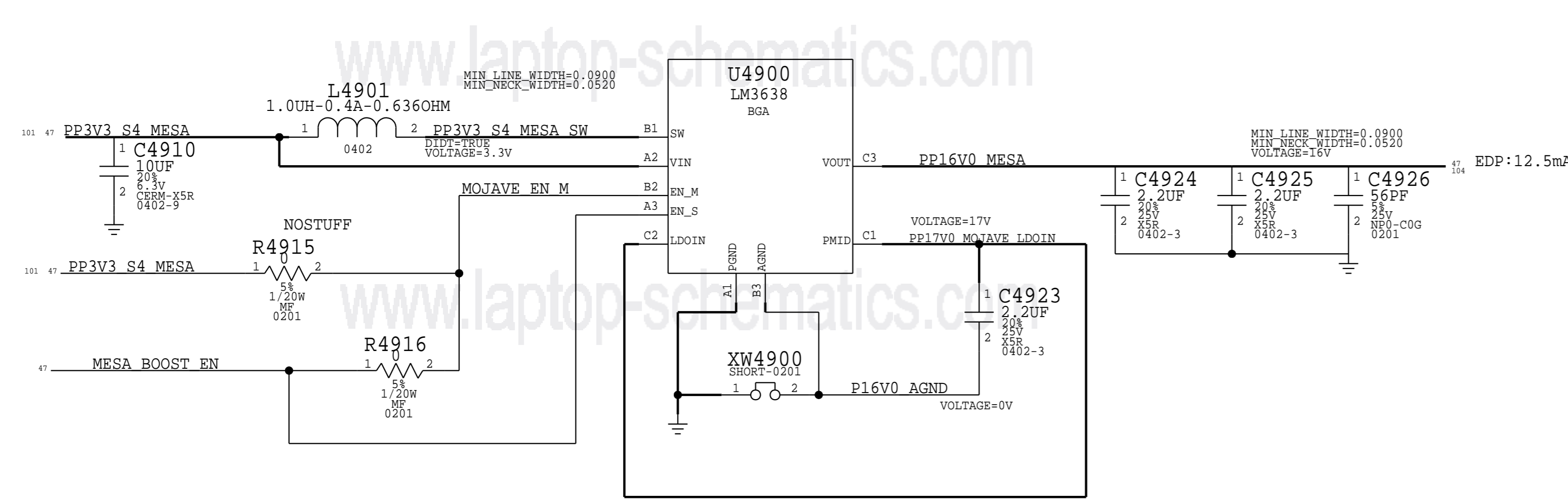
3

2

1

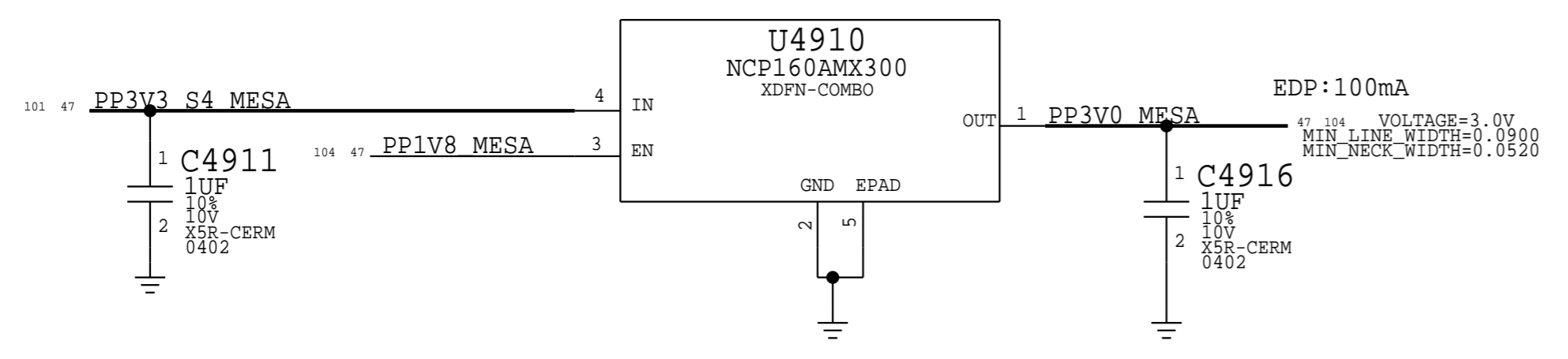
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

MOJAVE 16V BOOST

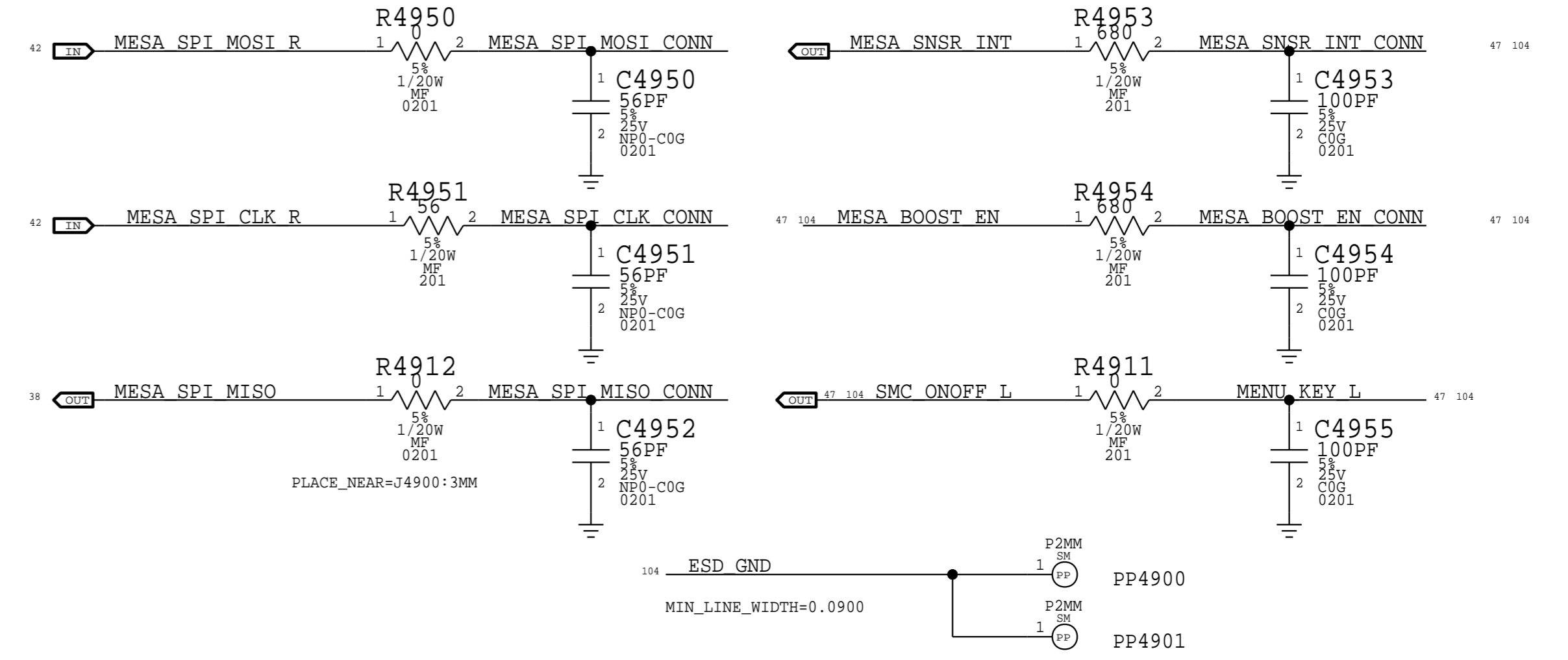
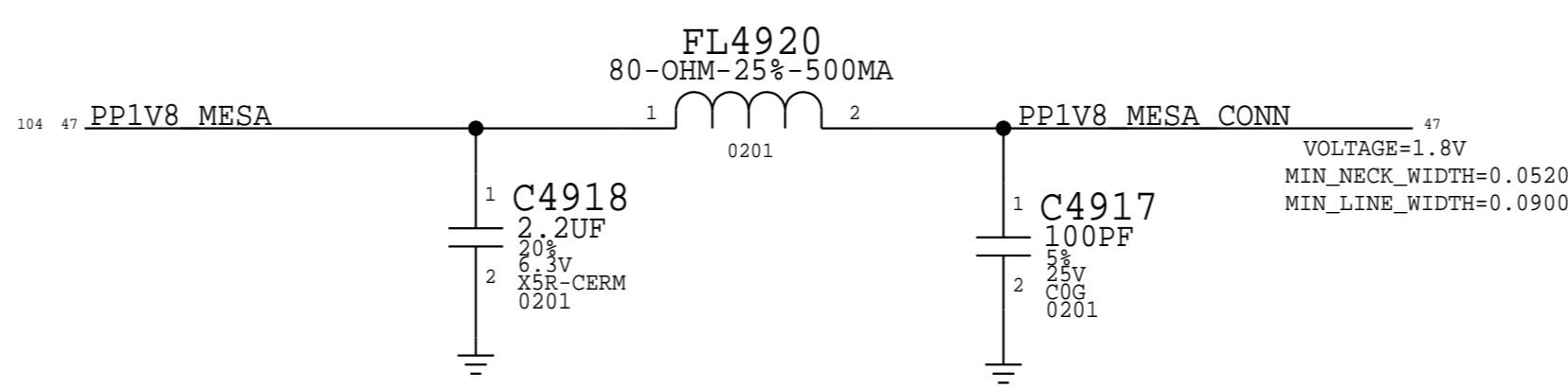
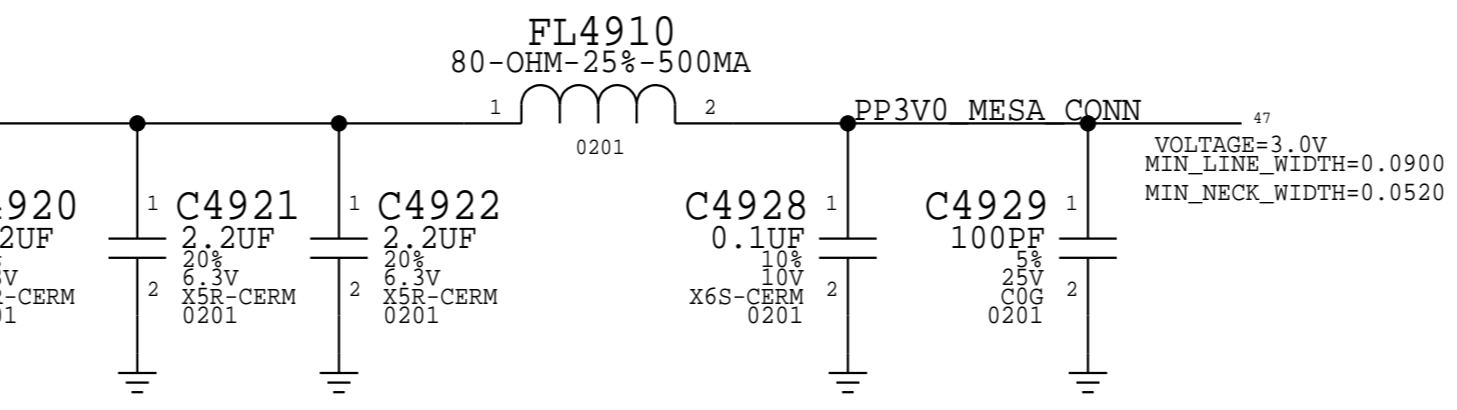
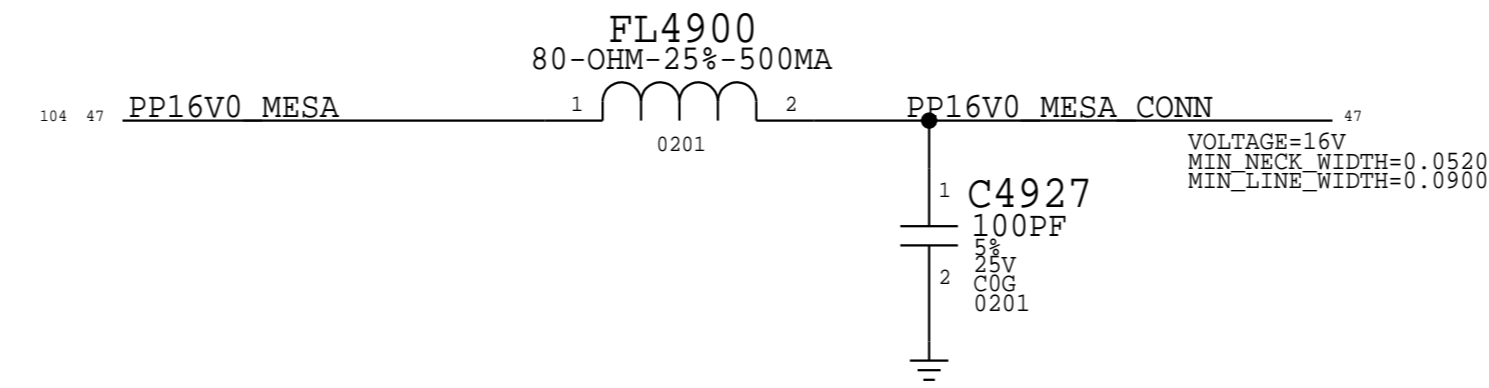
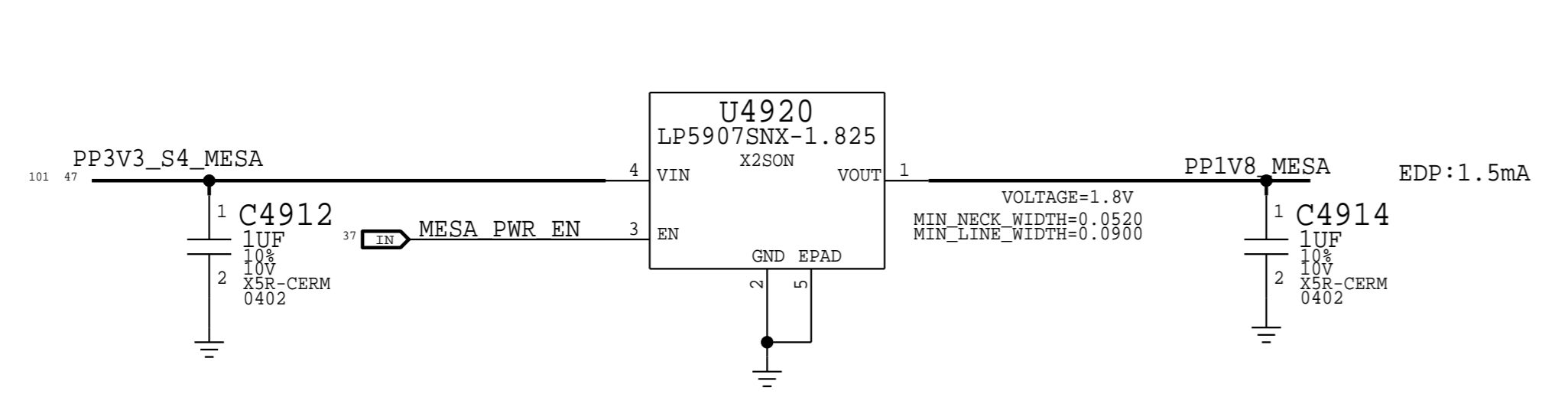


3.0V MESA

Option to feed LDO from 5V in case of dropout issue

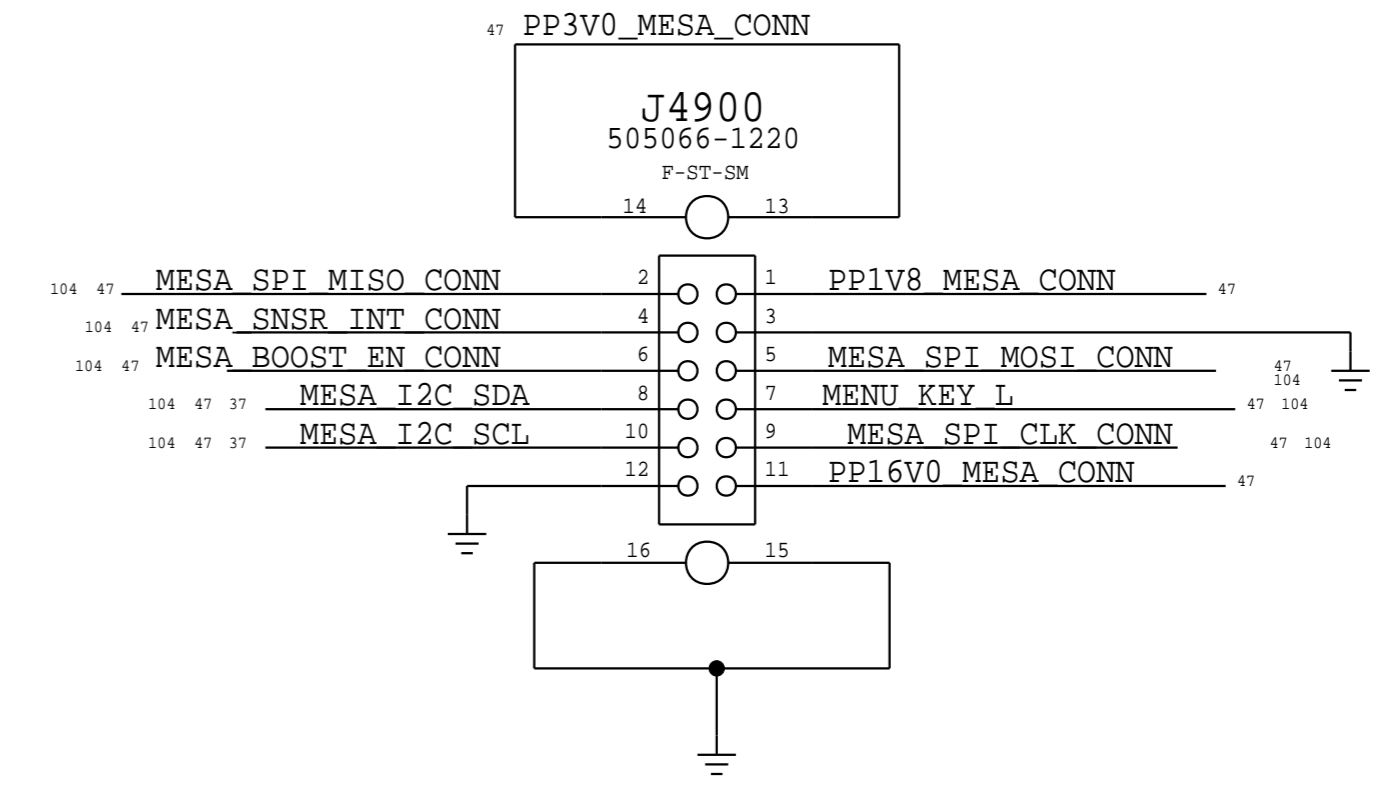


1.8V MESA



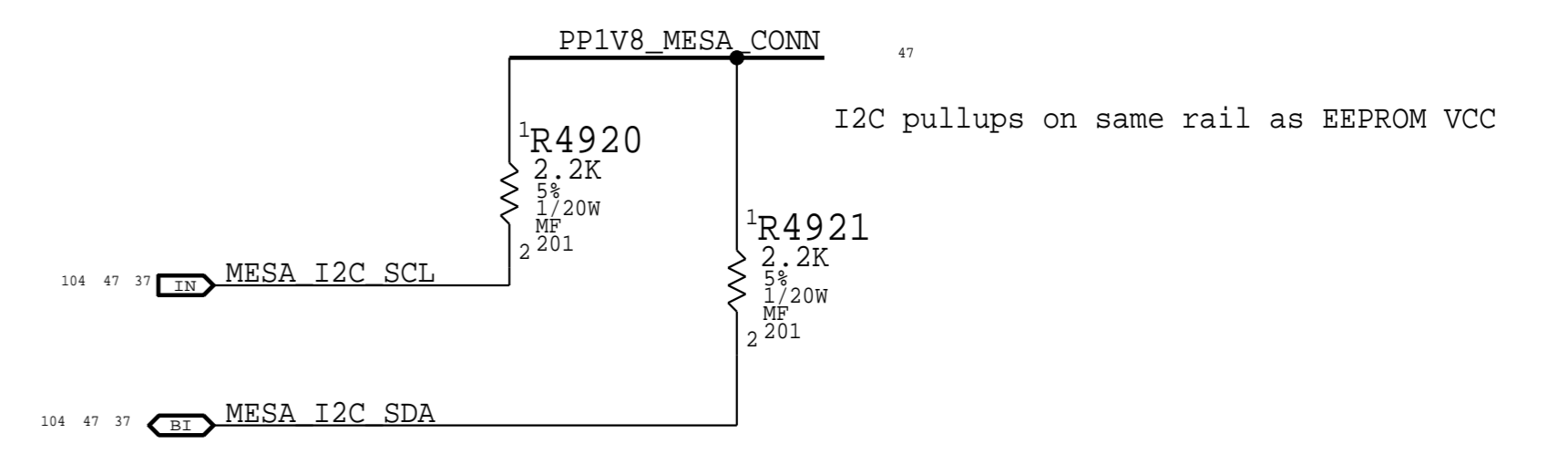
MESA FLEX CONNECTOR

Protol Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB



Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0



| | | | |
|---|--|----------------|-------------|
| PAGE TITLE | | MESA | |
| | | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 49 OF 145 |
| | | SHEET | 47 OF 119 |

BOM_COST_GROUP=T151

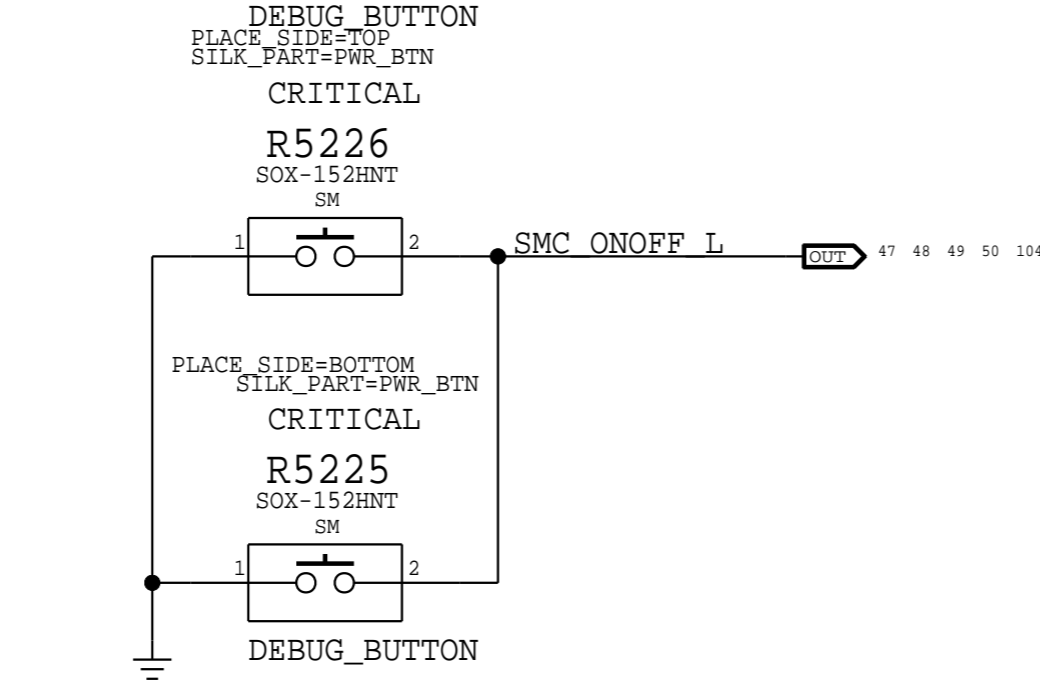
SMC12 ADC Assignments

| | | | |
|------------------------|------------------------|----|----|
| SMC CPU HI ISENSE | SMC CPU HI ISENSE | IN | 52 |
| SMC PBUS VSENSE | SMC PBUS VSENSE | IN | 52 |
| SMC BMON ISENSE | SMC BMON ISENSE | IN | 52 |
| SMC DCIN ISENSE | SMC DCIN ISENSE | IN | 52 |
| SMC DCIN VSENSE | SMC DCIN VSENSE | IN | 52 |
| SMC CPUGT ISENSE | SMC CPUGT ISENSE | IN | 55 |
| SMC CPU ISENSE | SMC CPU ISENSE | IN | 53 |
| SMC OTHER5V HI ISENSE | SMC OTHER5V HI ISENSE | IN | 52 |
| SMC OTHER3V3 HI ISENSE | SMC OTHER3V3 HI ISENSE | IN | 52 |
| SMC DDR1V2 ISENSE | SMC DDR1V2 ISENSE | IN | 53 |
| SMC CPUEDRAM ISENSE | SMC CPUEDRAM ISENSE | IN | 55 |
| SMC PCH ISENSE | SMC PCH ISENSE | IN | 53 |
| SMC TPAD ISENSE | SMC TPAD ISENSE | IN | 52 |
| SMC PICCOLO ISENSE | SMC PICCOLO ISENSE | IN | 52 |
| SMC SSDNAND ISENSE | SMC SSDNAND ISENSE | IN | 55 |
| SMC PCHPRIMCORE ISENSE | SMC PCHPRIMCORE ISENSE | IN | 55 |
| SMC DDR1V8 ISENSE | SMC DDR1V8 ISENSE | IN | 55 |
| SMC CPUSA ISENSE | SMC CPUSA ISENSE | IN | 55 |
| SMC CPUDDR ISENSE | SMC CPUDDR ISENSE | IN | 53 |
| SMC CPUSA VSENSE | SMC CPUSA VSENSE | IN | 55 |
| SMC CPU VSENSE | SMC CPU VSENSE | IN | 54 |
| SMC CPUGT VSENSE | SMC CPUGT VSENSE | IN | 54 |
| SMC CPU IMON ISENSE | SMC CPU IMON ISENSE | IN | 54 |
| SMC CPUGT IMON ISENSE | SMC CPUGT IMON ISENSE | IN | 54 |

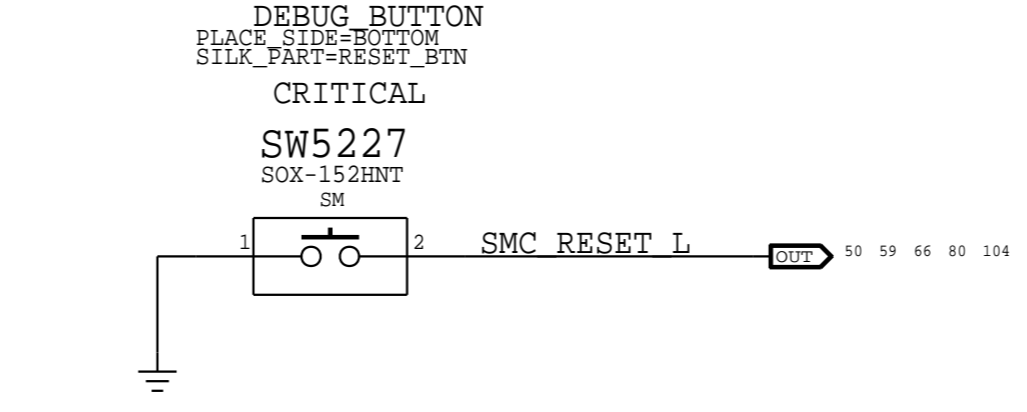
SMC12 Pin Assignments

| | | | |
|--------------------------|--------------------------|-----------|--------|
| NC SMC GFX THROTTLE L | NC SMC GFX THROTTLE L | NO_TEST=1 | |
| NC SMC GFX OVERTEMP | NC SMC GFX OVERTEMP | NO_TEST=1 | |
| NC SMC GFX SELF THROTTLE | NC SMC GFX SELF THROTTLE | NO_TEST=1 | |
| NC SMC DP HPD L | NC SMC DP HPD L | NO_TEST=1 | |
| NC SYS ONEWIRE | NC SYS ONEWIRE | NO_TEST=1 | |
| NC SMC DEBUGPRT EN L | NC SMC DEBUGPRT EN L | NO_TEST=1 | |
| SMC LID RIGHT | SMC LID RIGHT | | 50 |
| NC SPI SMC MISO | NC SPI SMC MISO | NO_TEST=1 | TRUE |
| NC SPI SMC MOSI | NC SPI SMC MOSI | NO_TEST=1 | TRUE |
| NC SPI SMC CLK | NC SPI SMC CLK | NO_TEST=1 | TRUE |
| NC SPI SMC CS L | NC SPI SMC CS L | NO_TEST=1 | TRUE |
| SMC VIBE L | SMC VIBE L | | 43 |
| SMC PCH SUSWARN L | SMC PCH SUSWARN L | | 14 |
| SMC PCH SUSACK L | SMC PCH SUSACK L | | 14 |
| SMC SENSOR PWR EN | SMC SENSOR PWR EN | | 78 |
| WLAN UART RX | WLAN UART RX | | 35 |
| WLAN UART TX | WLAN UART TX | | 35 |
| SMC AUX OK | SMC AUX OK | | 49 |
| PM PWRBTN L | PM PWRBTN L | | 14 |
| SMC AUX OK | SMC AUX OK | | 52 |
| SMBUS SMC 4 G3H SCL | SMBUS SMC 4 G3H SCL | | 48 |
| SMBUS SMC 4 G3H SDA | SMBUS SMC 4 G3H SDA | | 48 |
| SMBUS SMC 2 S4 SCL | SMBUS SMC 2 S4 SCL | | 48 |
| SMBUS SMC 2 S4 SDA | SMBUS SMC 2 S4 SDA | | 48 |
| SMC OOB1 D2R L | SMC OOB1 D2R L | | 88 |
| SMC OOB1 R2D L | SMC OOB1 R2D L | | 88 |
| SMC ACTUATOR DISABLE L | SMC ACTUATOR DISABLE L | | 43 104 |
| SMC CHGR INT L | SMC CHGR INT L | | 66 |

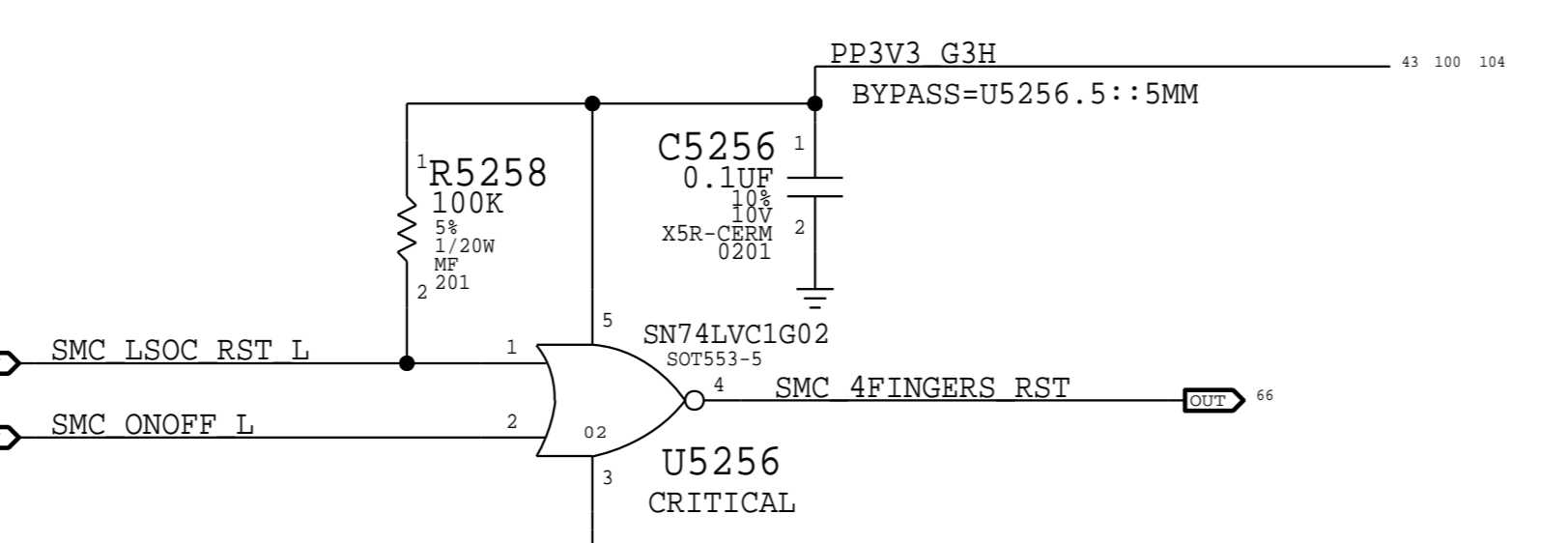
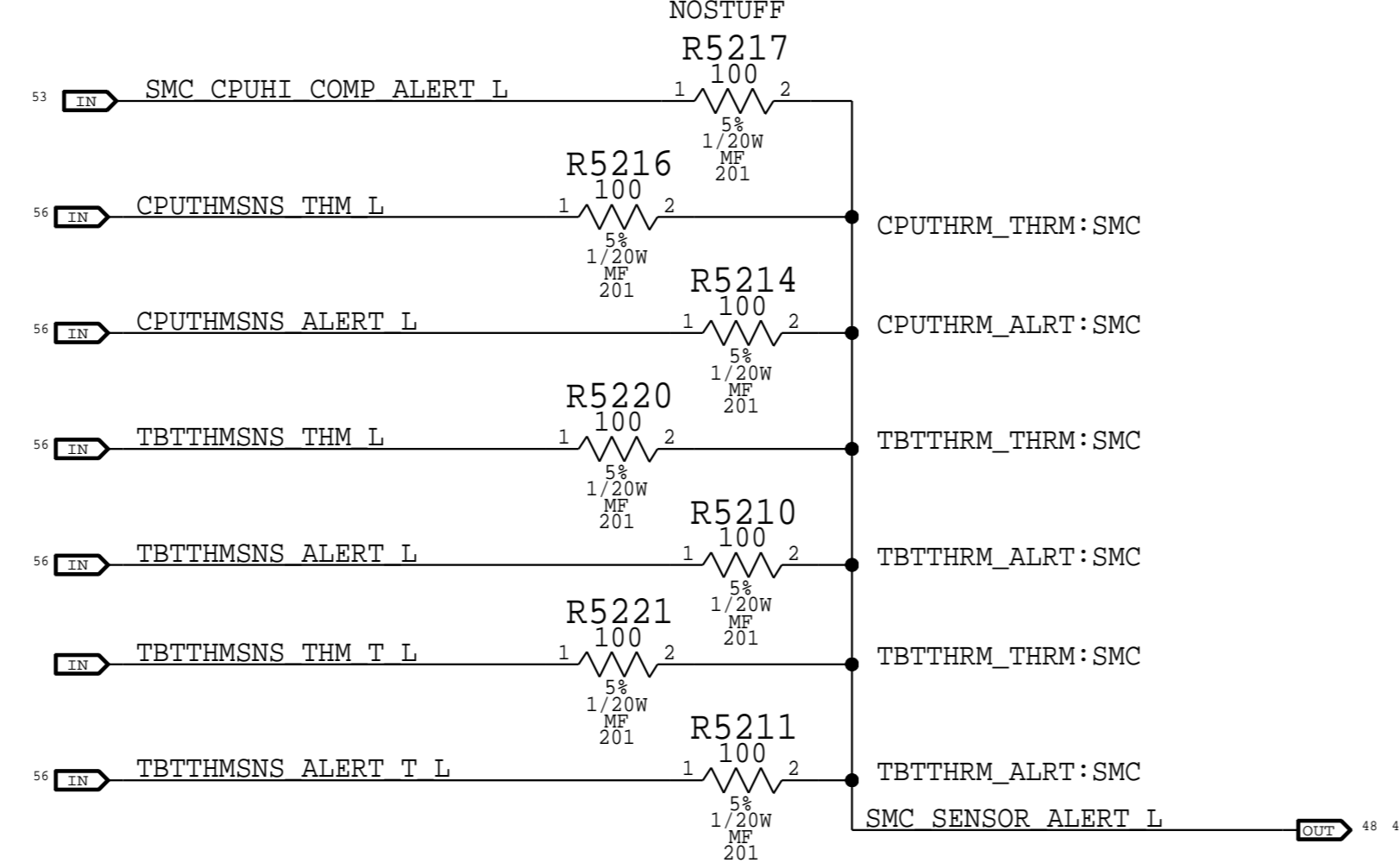
Debug Power "Buttons"



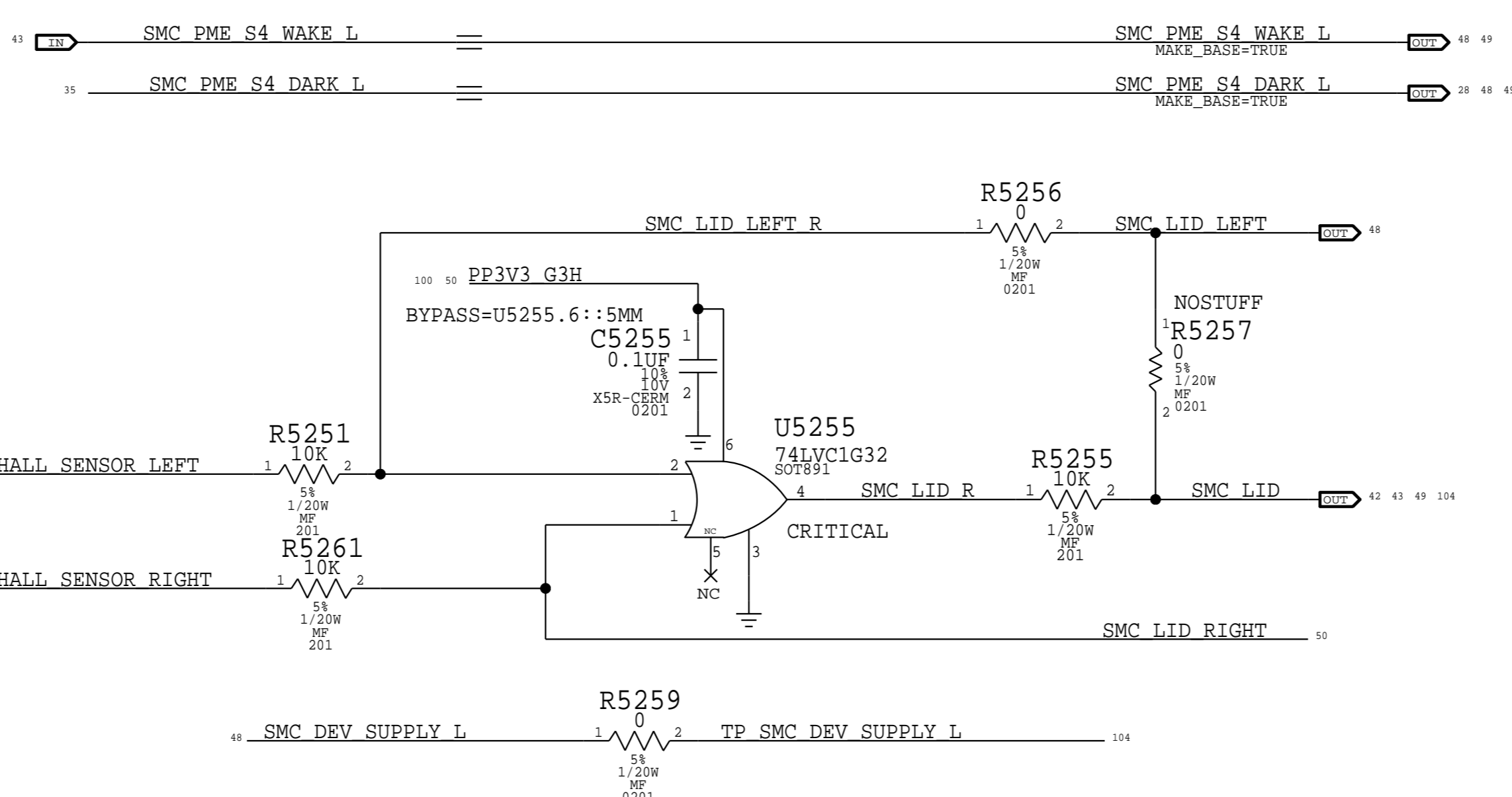
Debug RESET "Buttons"



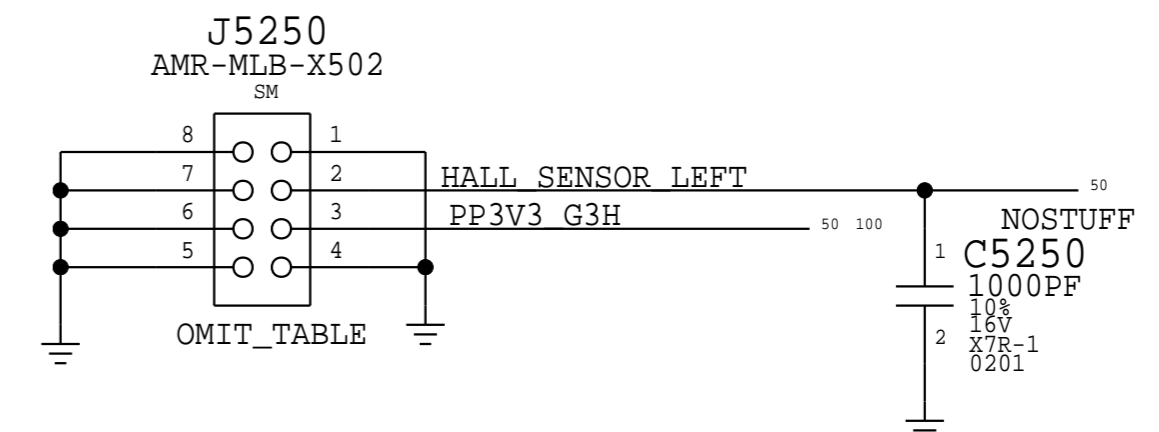
Thermal Alerts



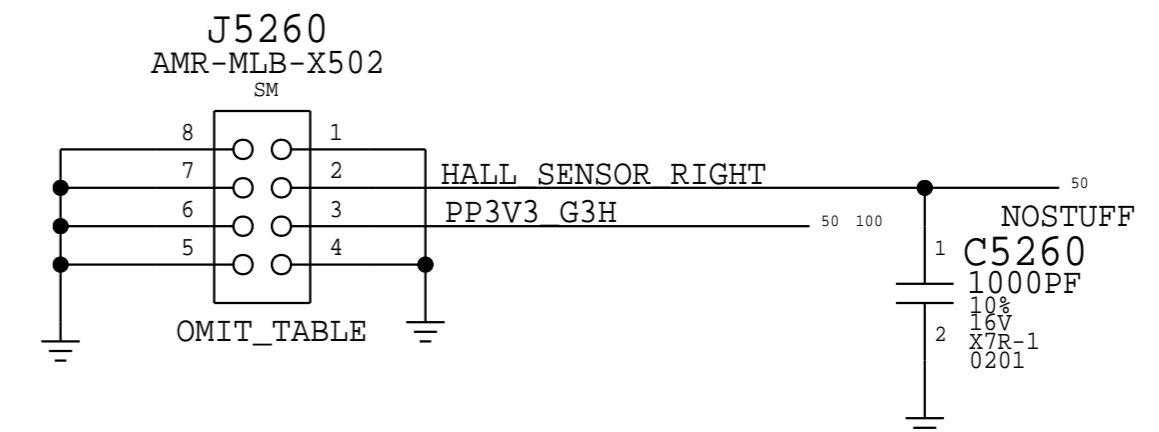
S4 SMC Wake Sources



Hall Effect Pads - Left



Hall Effect Pads - Right



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--|---------------|----------|------------|
| 677-04255 | 2 | SUBASSY (T&R) PCBA,HES INTERPOSER,X502 | J5250, J5260 | CRITICAL | |

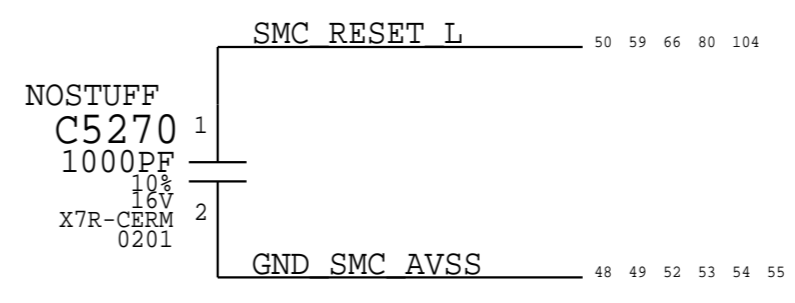
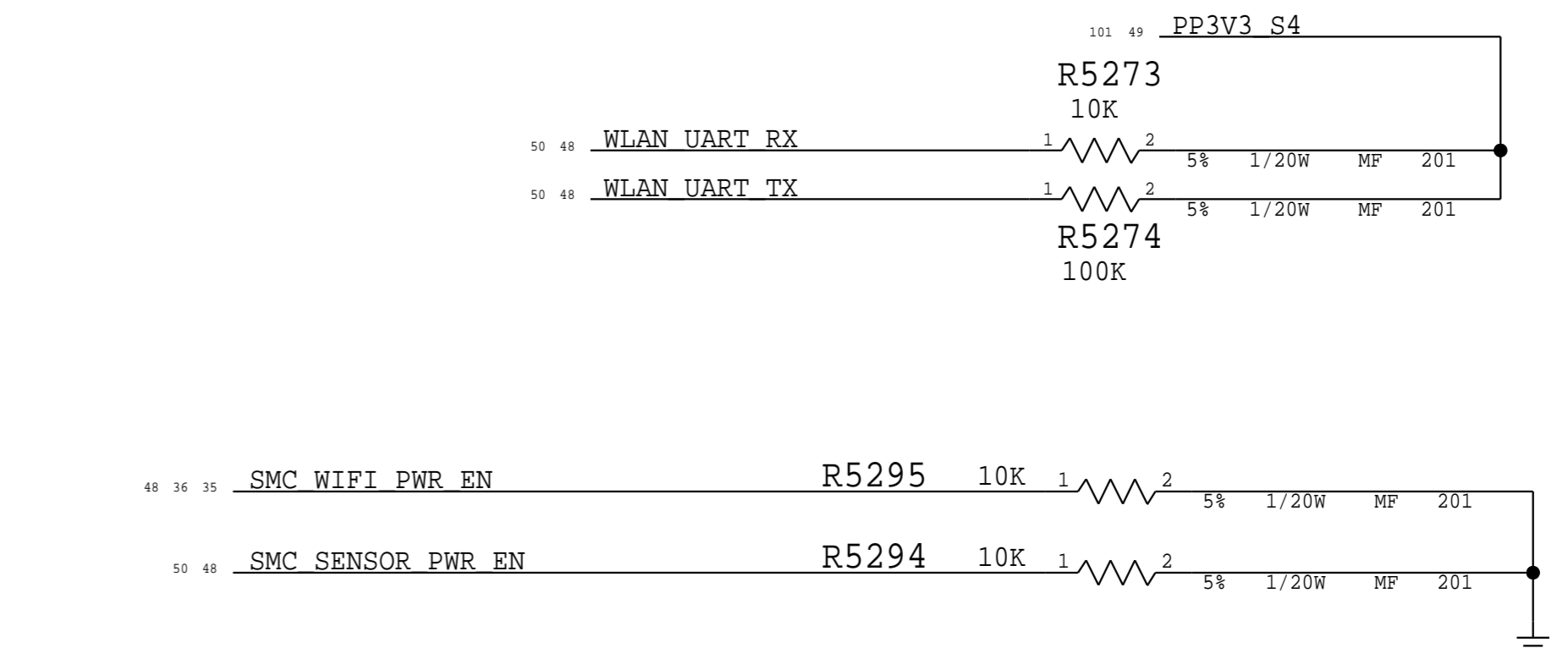
Specify one of these BOM GROUPS.

| BOM GROUP | BOM OPTIONS |
|--------------|-----------------------------------|
| CPUTHRM:BOTH | CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC |
| CPUTHRM:THRM | CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU |
| CPUTHRM:ALRT | CPUTHRM_ALRT:SMC |
| CPUTHRM:NONE | CPUTHRM_ALRT:PU |

Specify one of these BOM GROUPS.

| BOM GROUP | BOM OPTIONS |
|--------------|-----------------------------------|
| TBTTHRM:BOTH | TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC |
| TBTTHRM:THRM | TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU |
| TBTTHRM:ALRT | TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC |
| TBTTHRM:NONE | TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU |

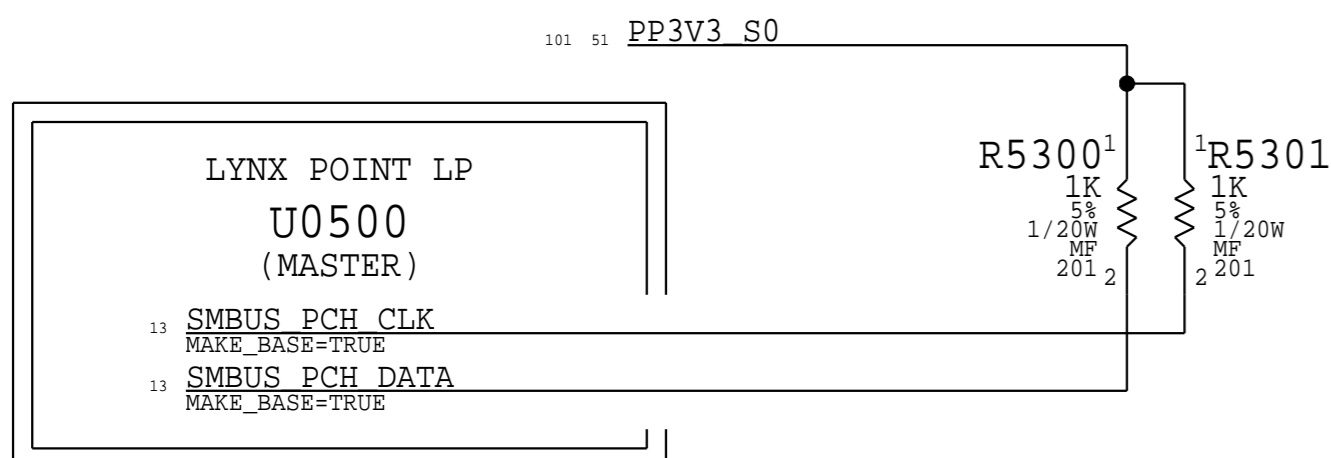
Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.



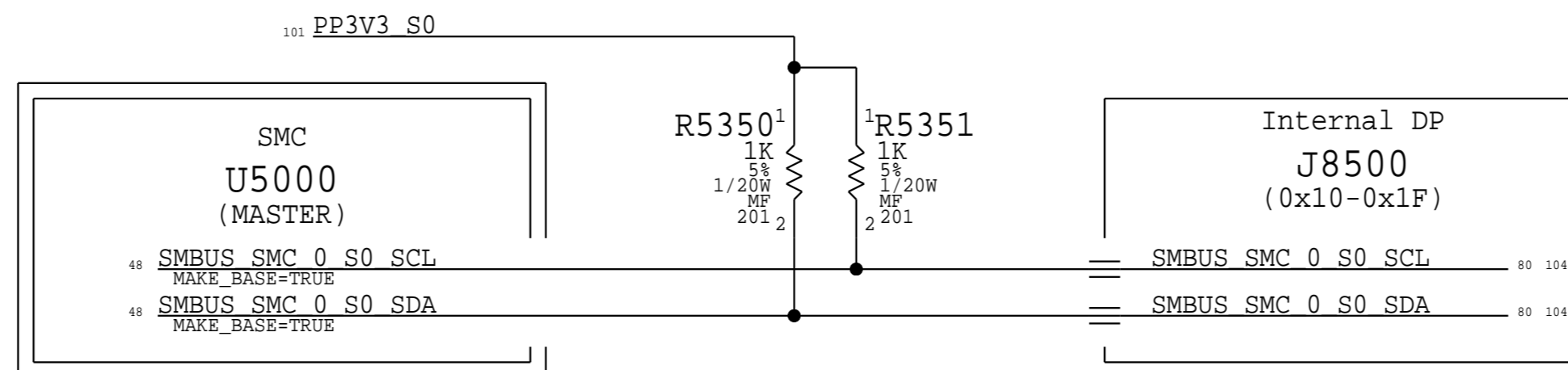
| | | | |
|----------------|--|--------------------------------|-------|
| PAGE TITLE | | PAGE_TITLE=SMC Project Support | |
| DRAWING NUMBER | | 051-00777 | STR D |
| REVISION | | 9.0.0 | |
| BRANCH | | dvt-fab09-0 | |
| PAGE | | 52 OF 145 | |
| SHEET | | 50 OF 119 | |

BOM_COST_GROUP=SMC

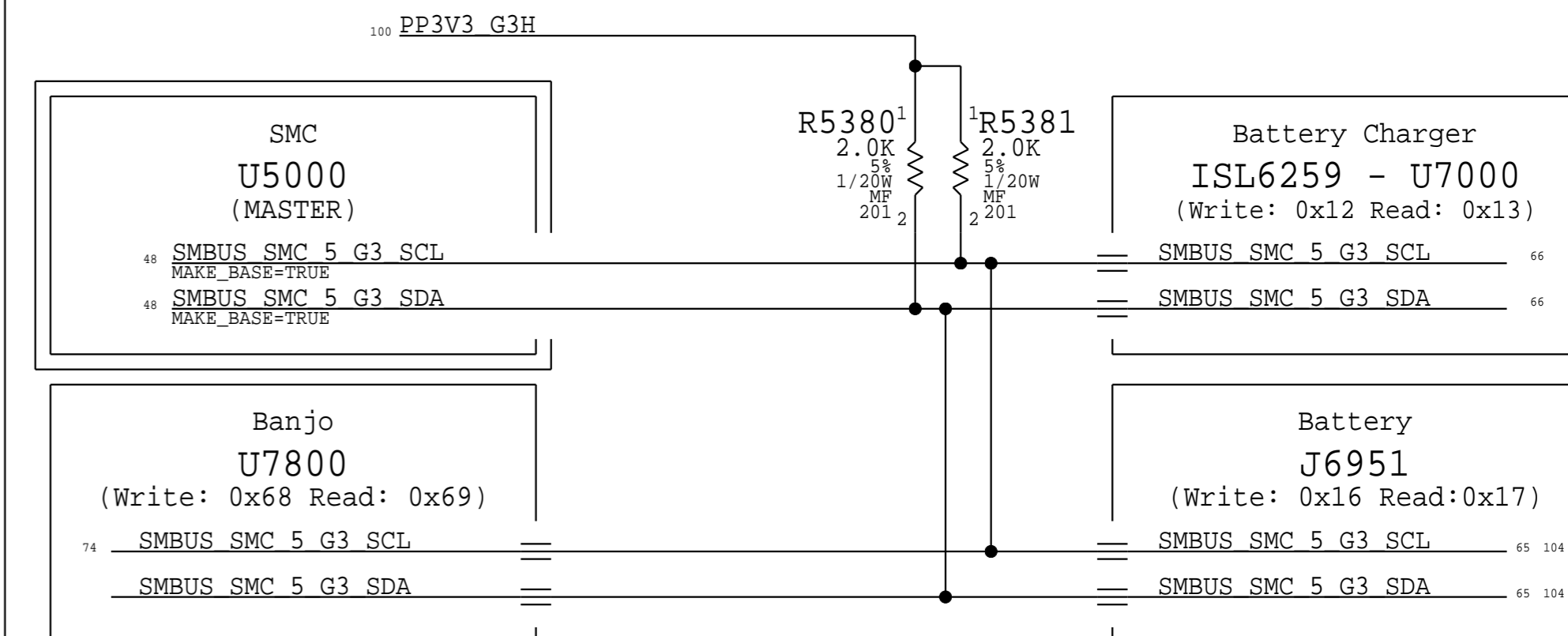
LYNX POINT LP S0 "SMBus 0" Connections



SMC SMBus "0" S0 Connections



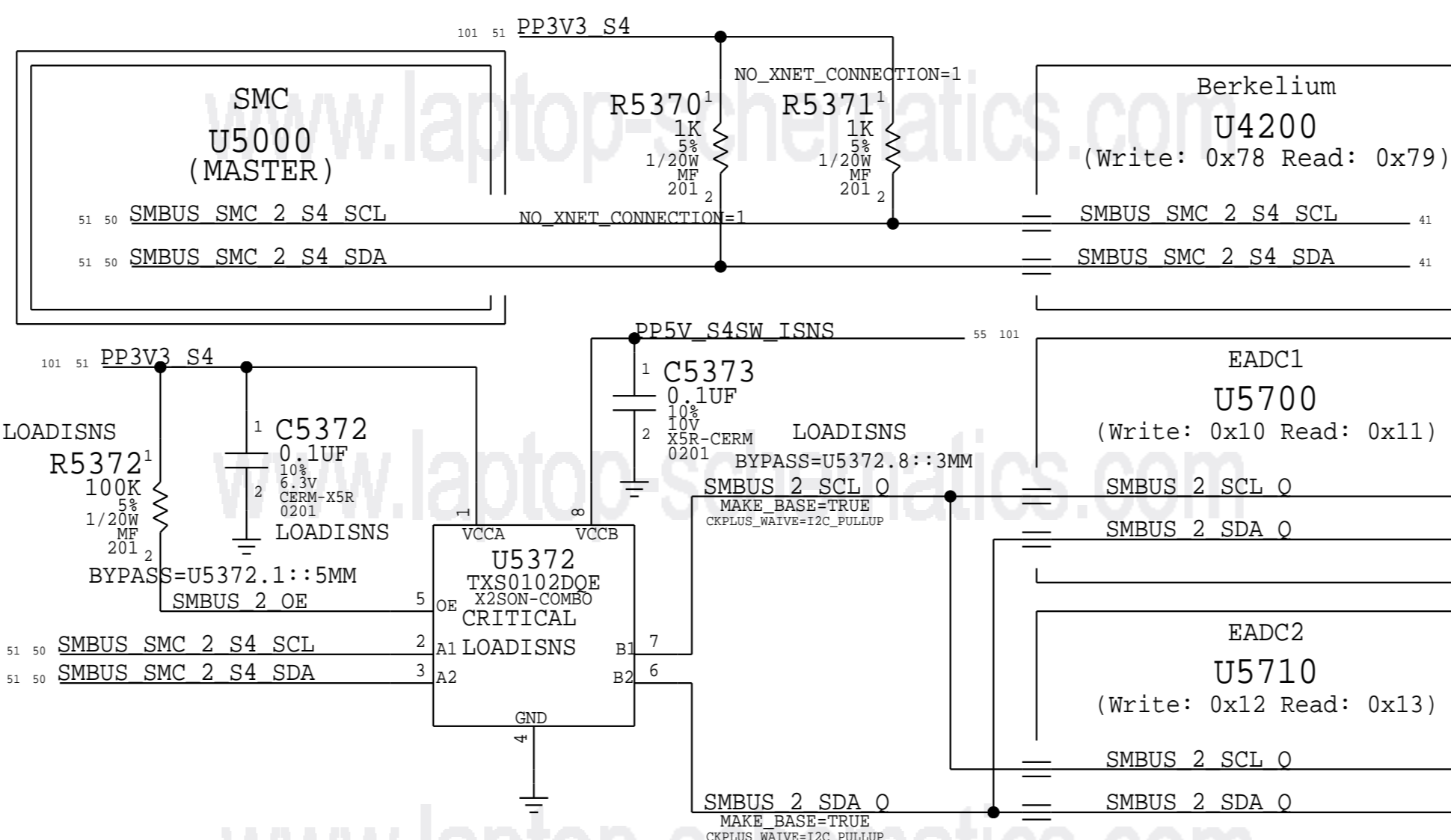
SMC SMBus "5" G3H Connections



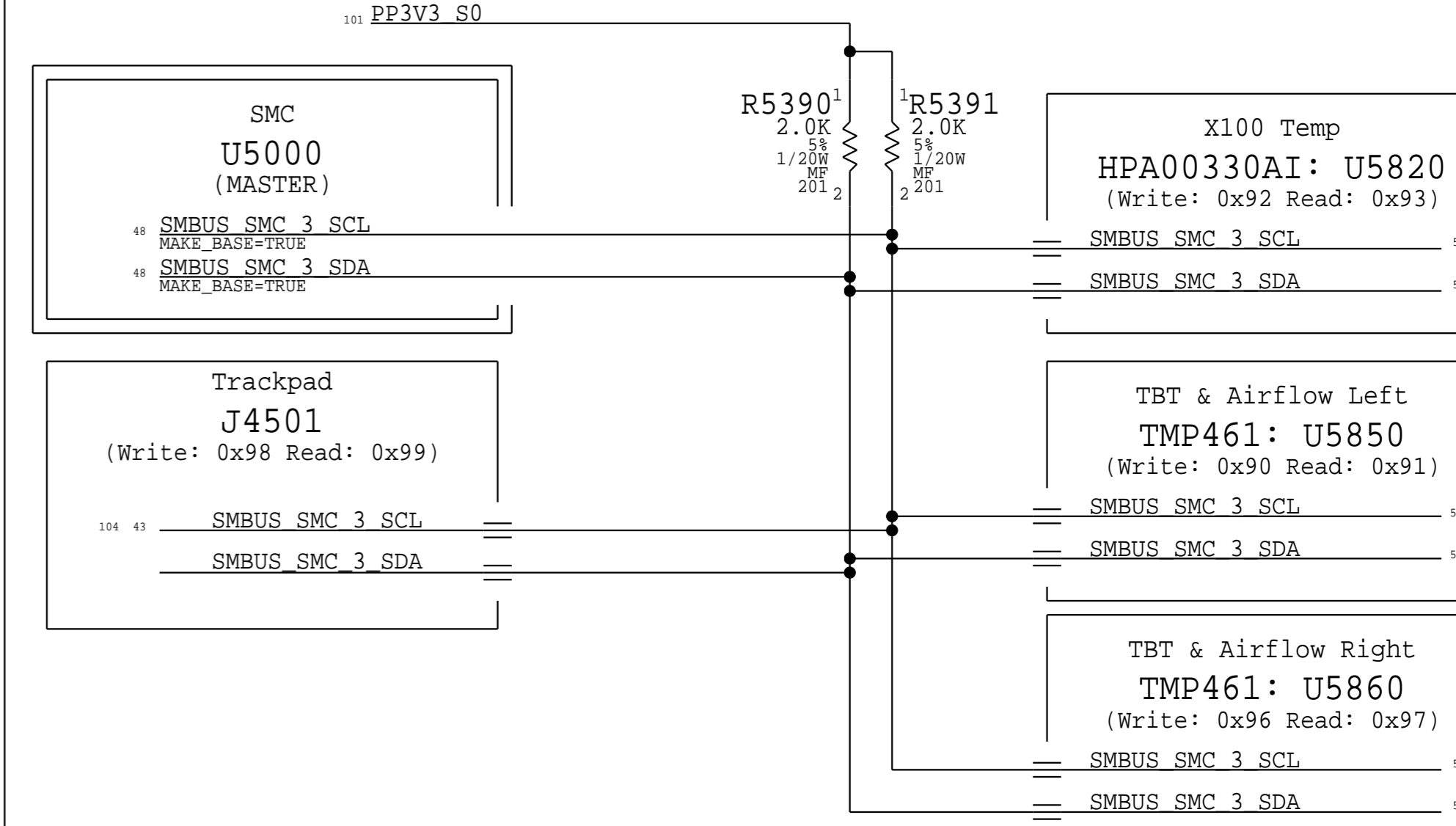
ACE I2C Interrupt



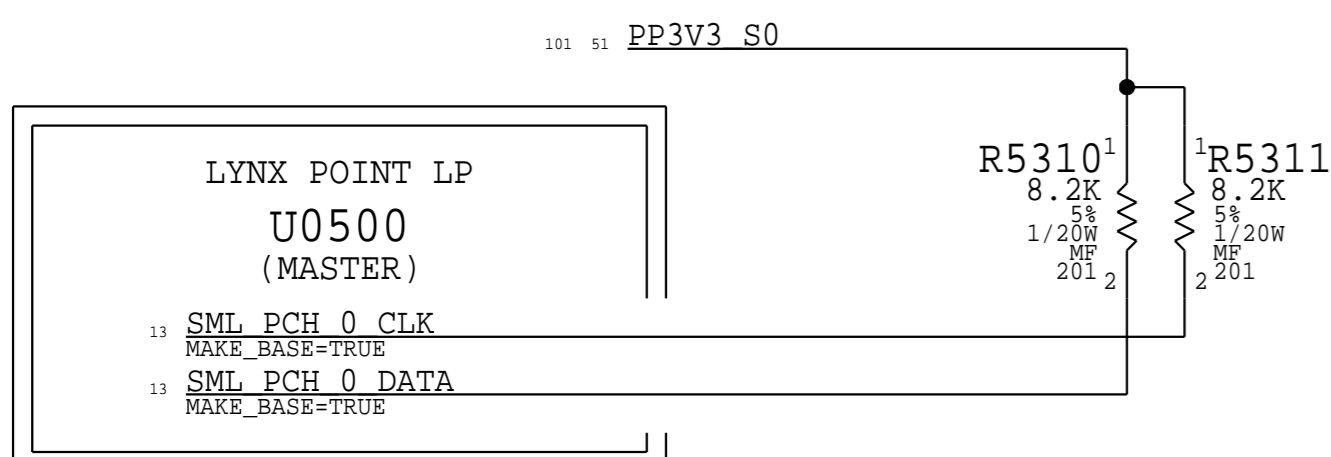
SMC SMBus "2" S4 Connections



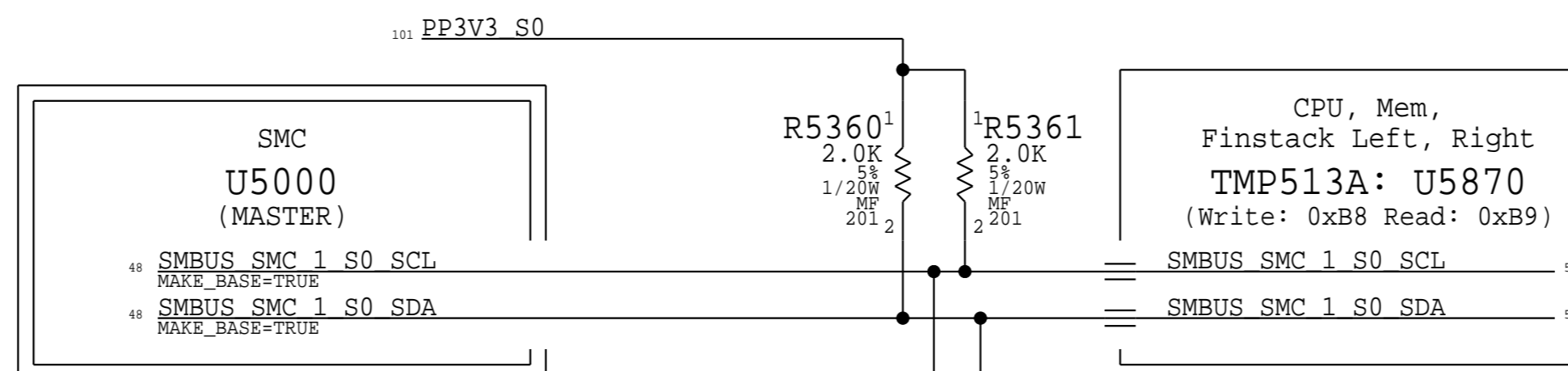
SMC SMBus "3" S0 Connections



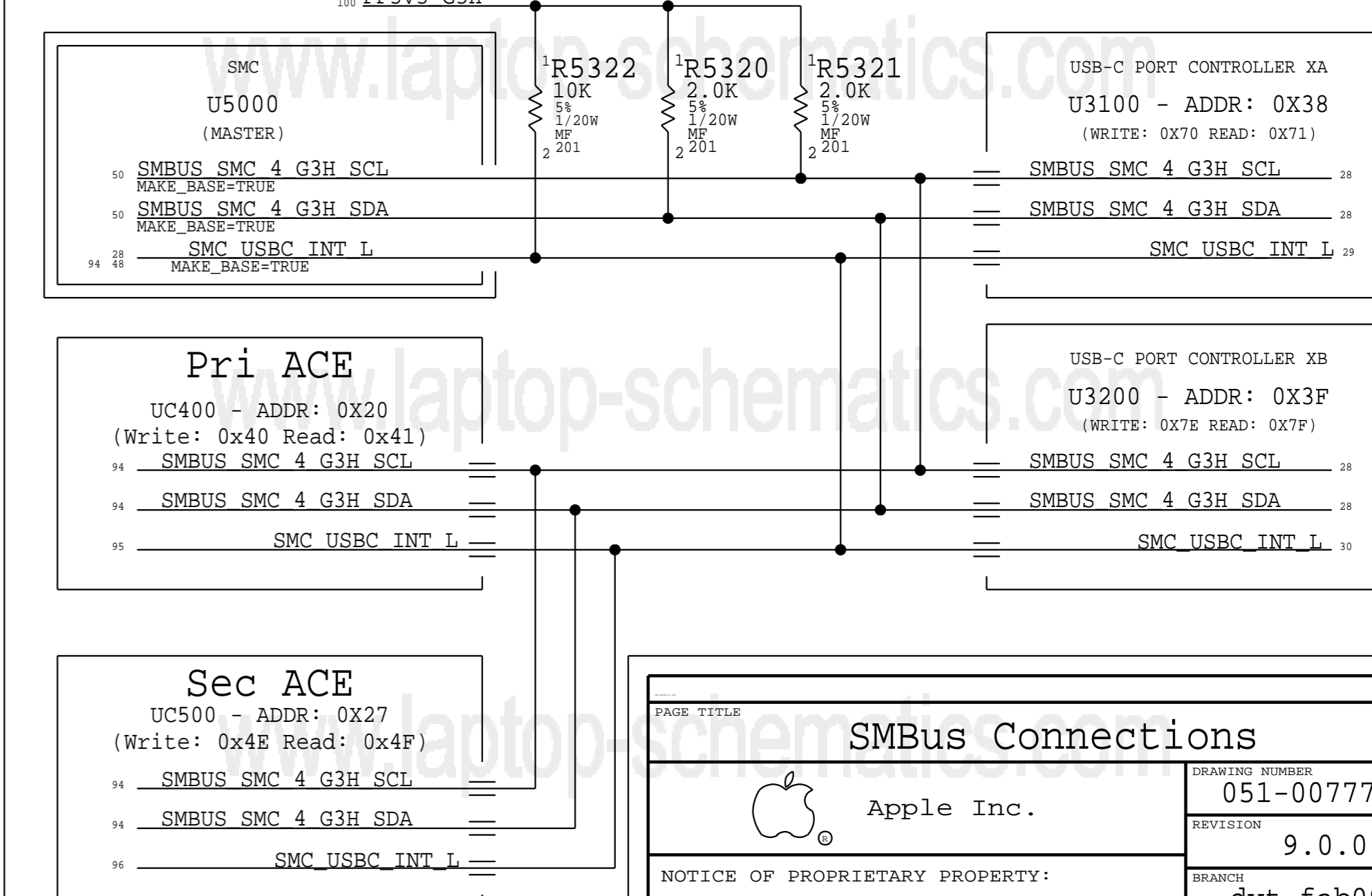
LYNX POINT LP S0 "SMLink 0" Connections



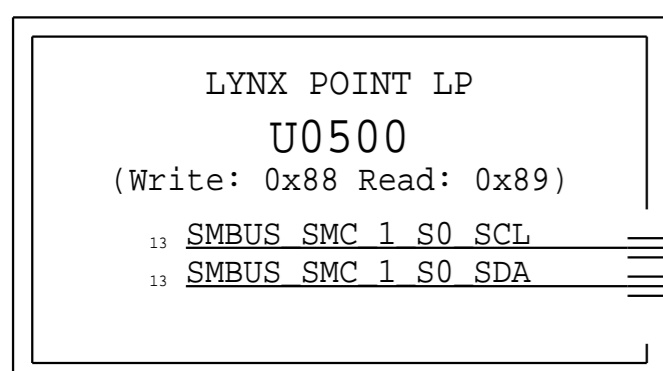
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



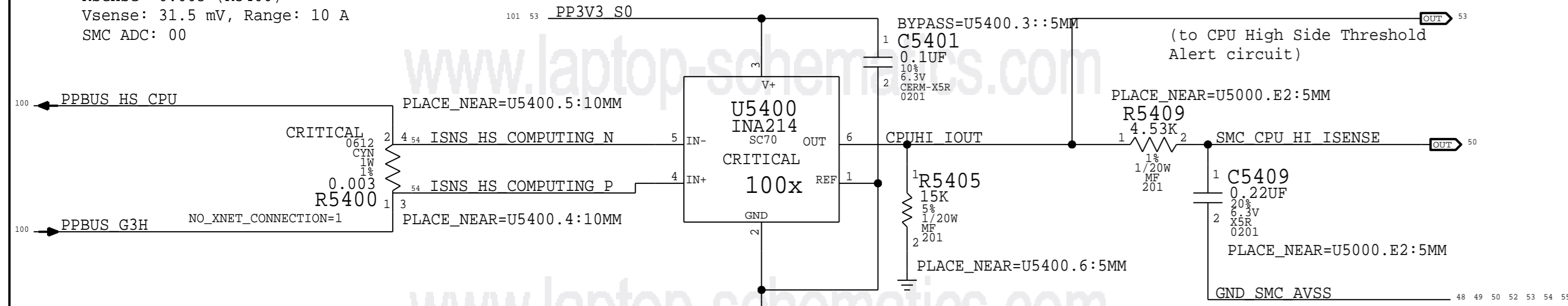
SMLink 1 is slave port to access PCH.

SMBus Connections

| | | | | | |
|------------|--|----------------|-------------|------|---|
| Apple Inc. | | DRAWING NUMBER | 051-00777 | STEP | D |
| | | REVISION | 9.0.0 | | |
| | | BRANCH | dvt-fab09-0 | | |
| | | PAGE | 53 OF 145 | | |
| | | SHEET | 51 OF 119 | | |

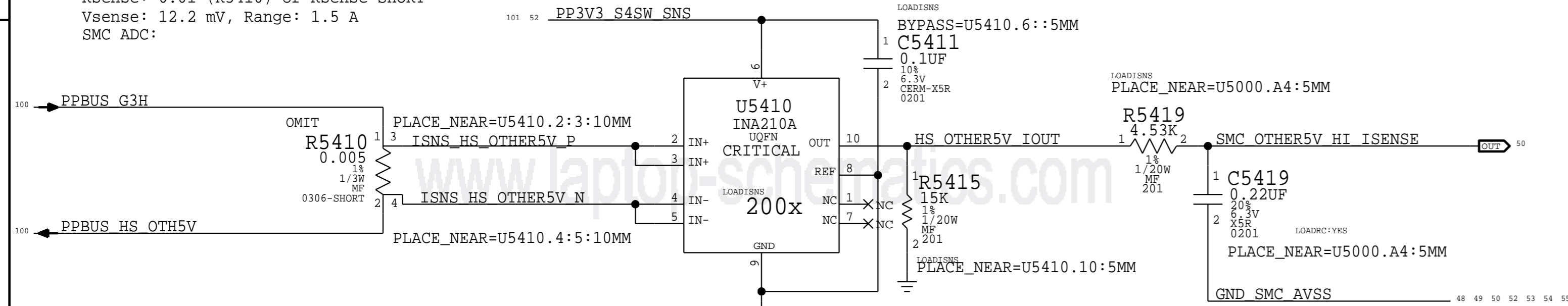
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
Rsense: 0.003 (R5400)
Vsense: 31.5 mV, Range: 10 A
SMC ADC: 00



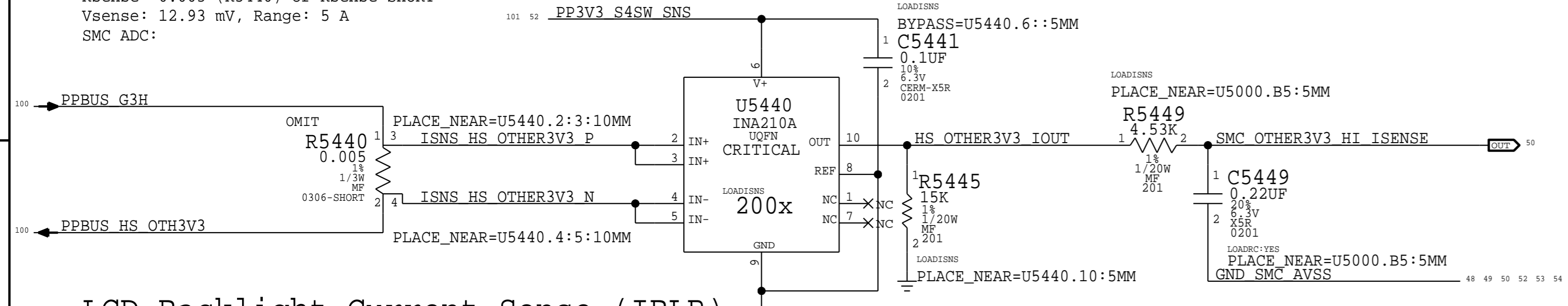
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:



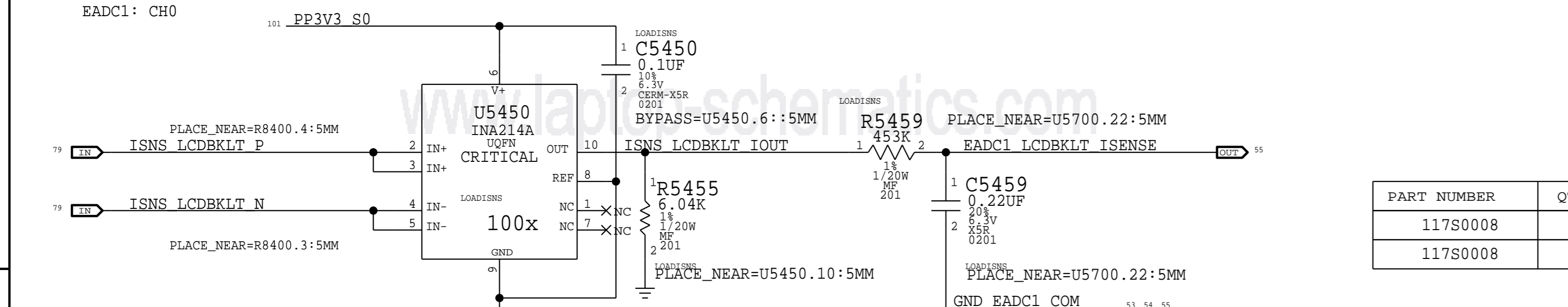
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:



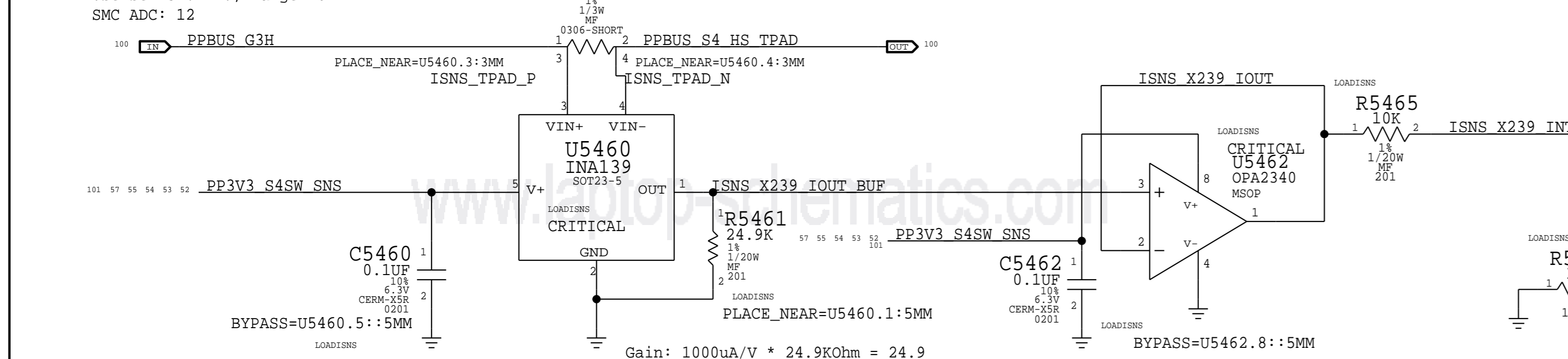
LCD Backlight Current Sense (IBLR)

Gain: 100x, EDP: 1 A
Rsense: 0.025 (R8400)
Vsense: 25 mV, Range: 2.4 A
EADC1: CH0



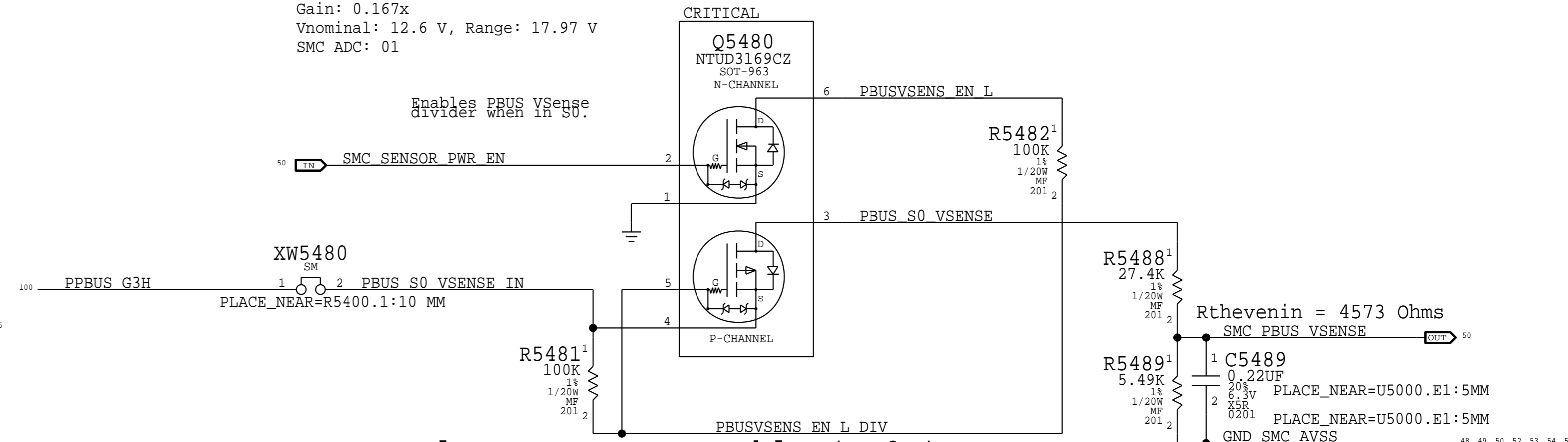
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 24.9x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 6 A
SMC ADC: 12



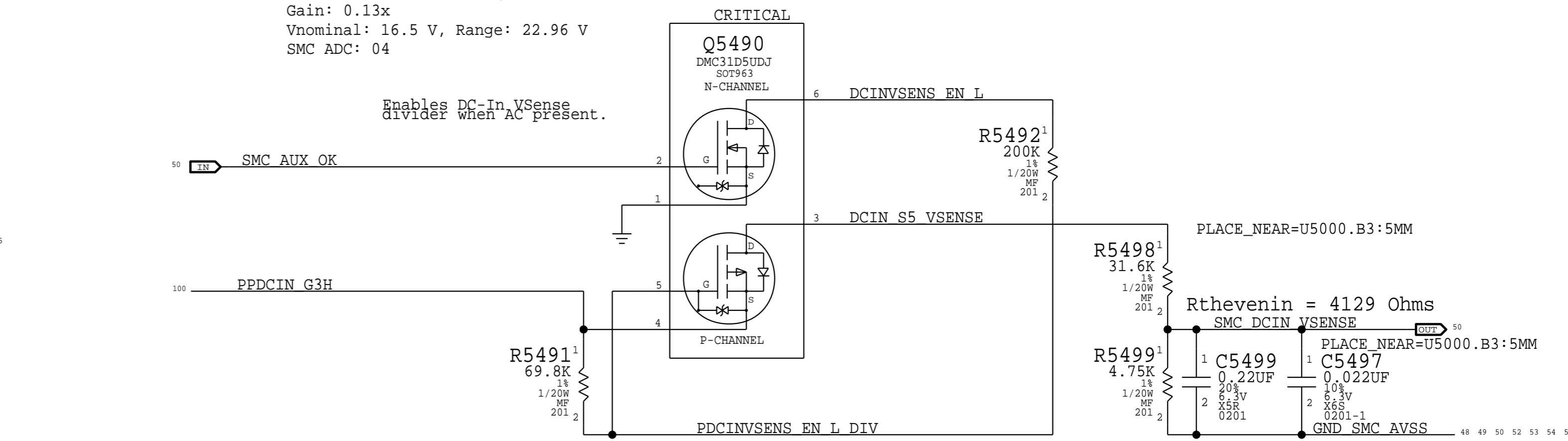
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01



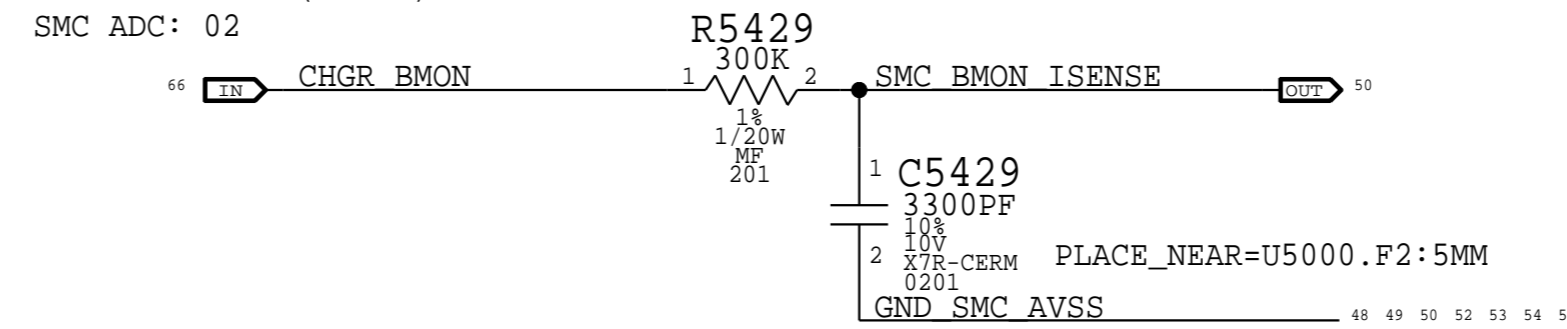
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13x
Vnominal: 16.5 V, Range: 22.96 V
SMC ADC: 04



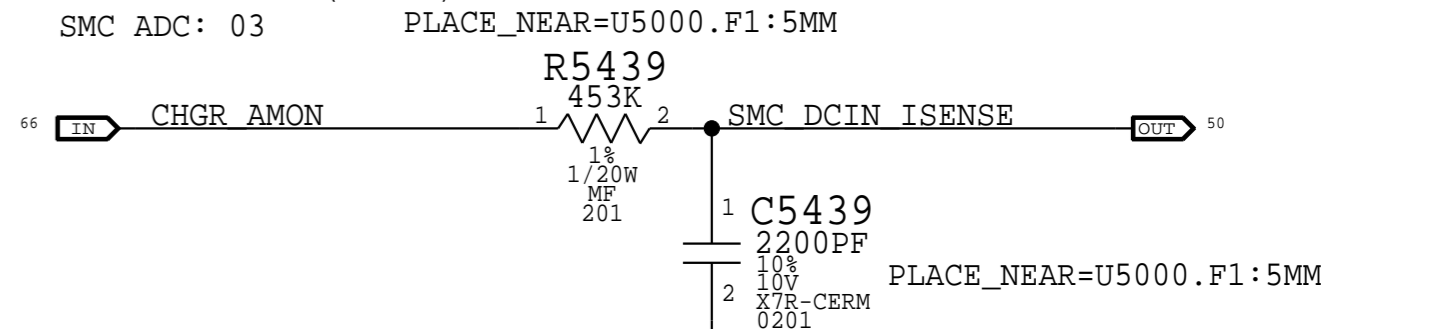
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 03



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------------------------|---------------|----------|------------|
| 117S0008 | 2 | RES_MTL FLIM,100K,1/16W,0201,SMD,LF | C5419,C5449 | | LOADRC:NO |
| 117S0008 | 1 | RES_MTL FLIM,100K,1/16W,0201,SMD,LF | C5469 | | LOADRC:NO |

Power Sensors: High Side

Apple Inc.

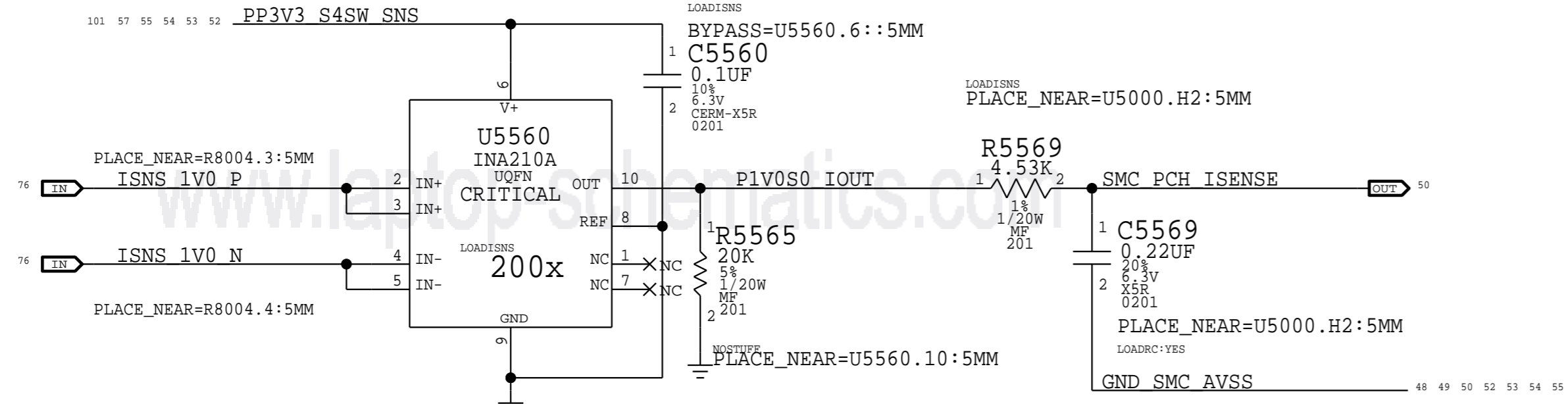
DRWING NUMBER: 051-00777
REVISION: 9.0.0

BRANCH: dvt-fab09-0
PAGE: 54 OF 145
SHEET: 52 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
11V ALL RIGHTS RESERVED

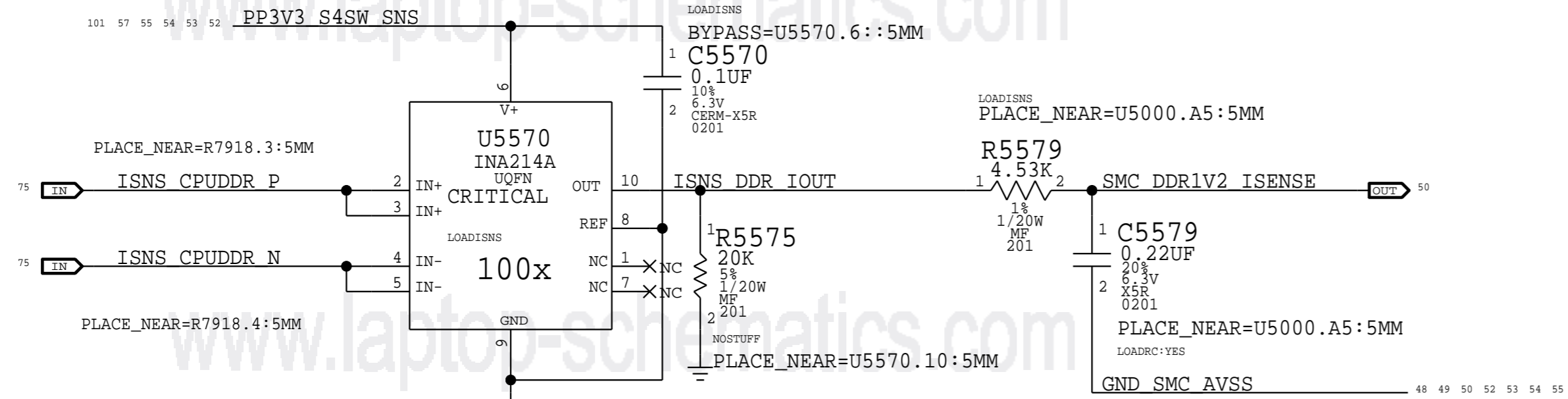
PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 3.29 A
Rsense: 0.003 (R8004) or Rsense SHORT
Vsense: 9.87 mV, Range: 5 A
SMC ADC: 11



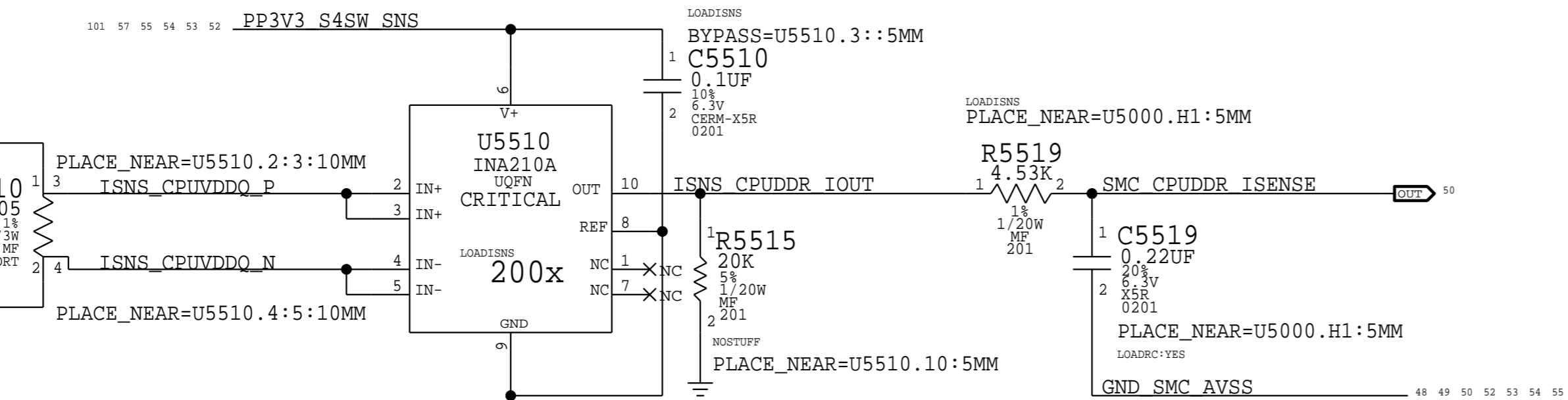
DDR 1.2V S3 (CPU & Memory) Current Sense (IMOC)

Gain: 100x, EDP: 8.21 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 24.63 mV, Range: 10 A
SMC ADC: 09



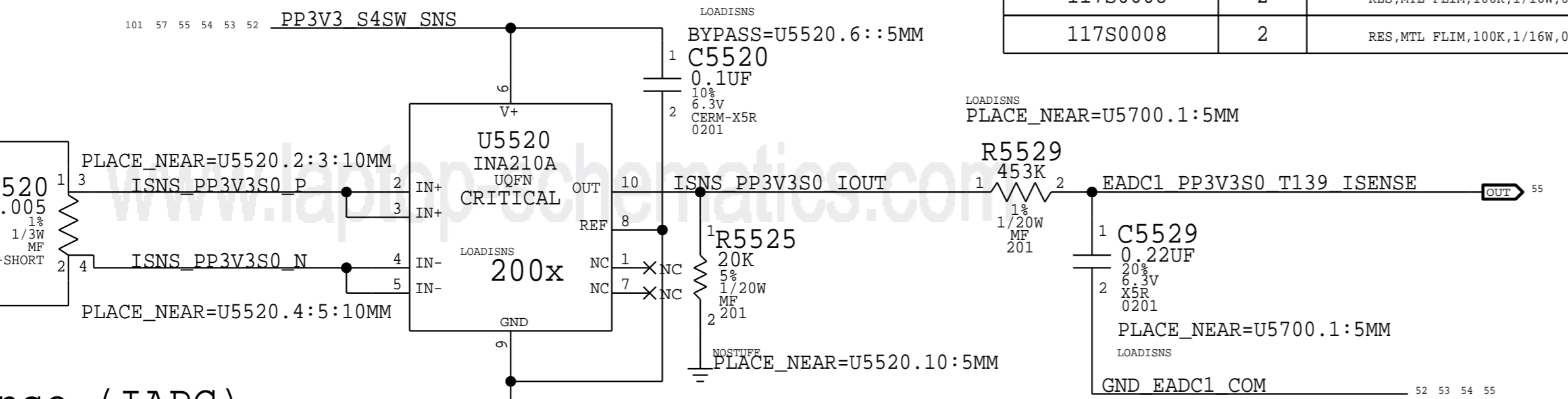
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



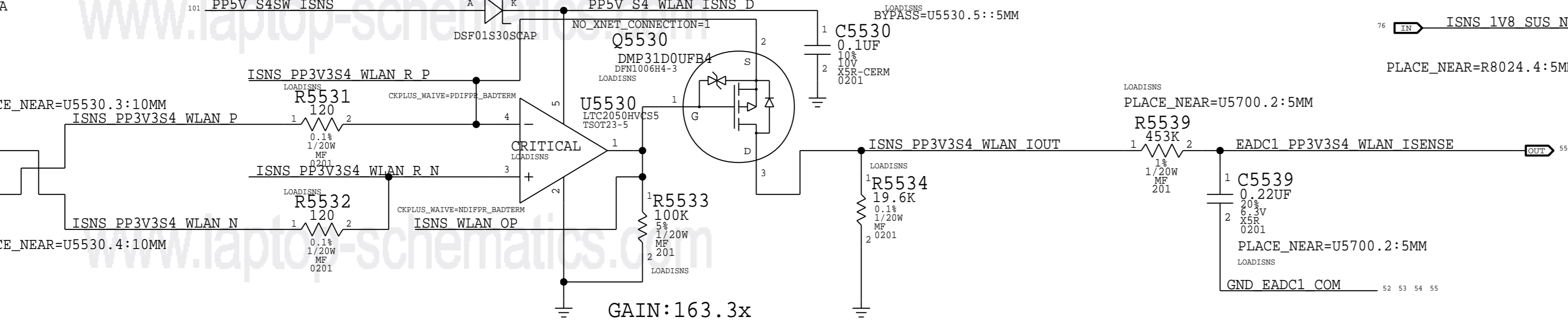
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



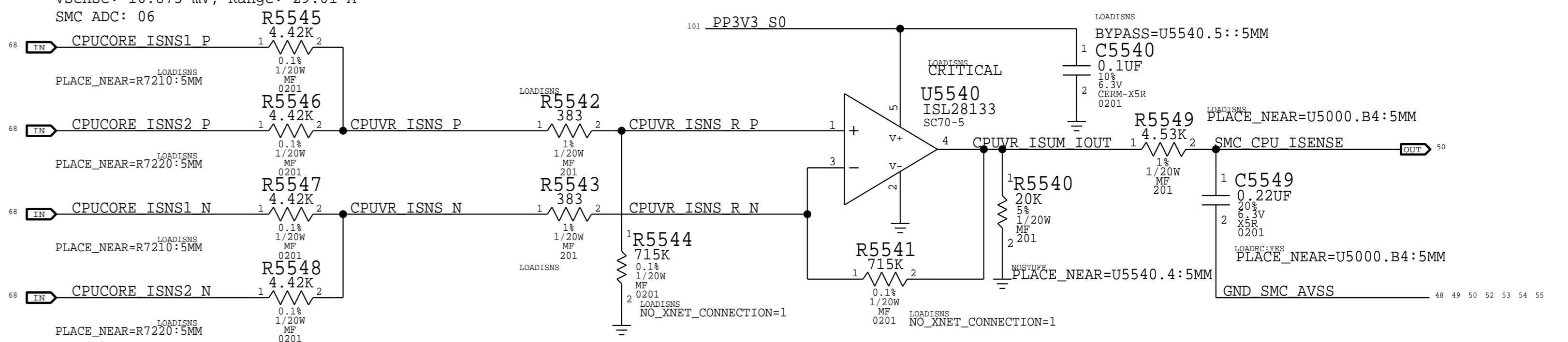
WLAN Current Sense (IAPC)

Gain: 163.3x, EDP: 1.67 A
Rsense: 0.015 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.67 A
EADC1: CH4



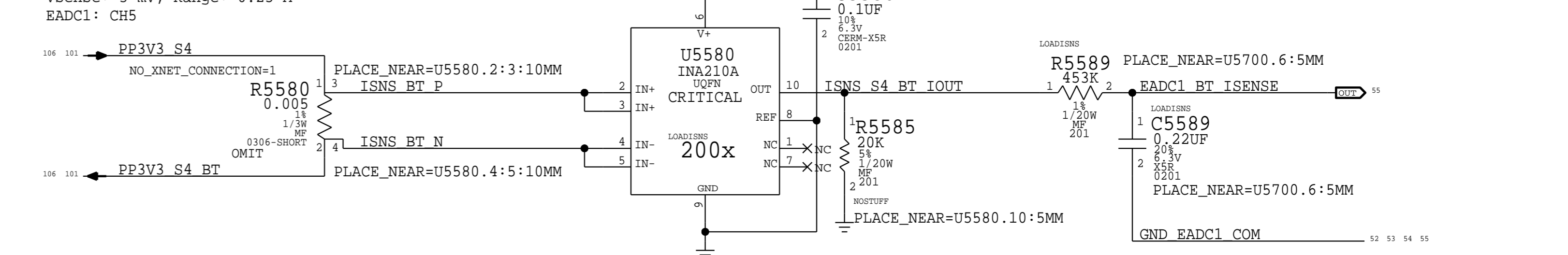
CPU Fixed Current Sense (ICAC)

Gain: 275.74x, EDP: 29 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 10.875 mV, Range: 29.01 A
SMC ADC: 06



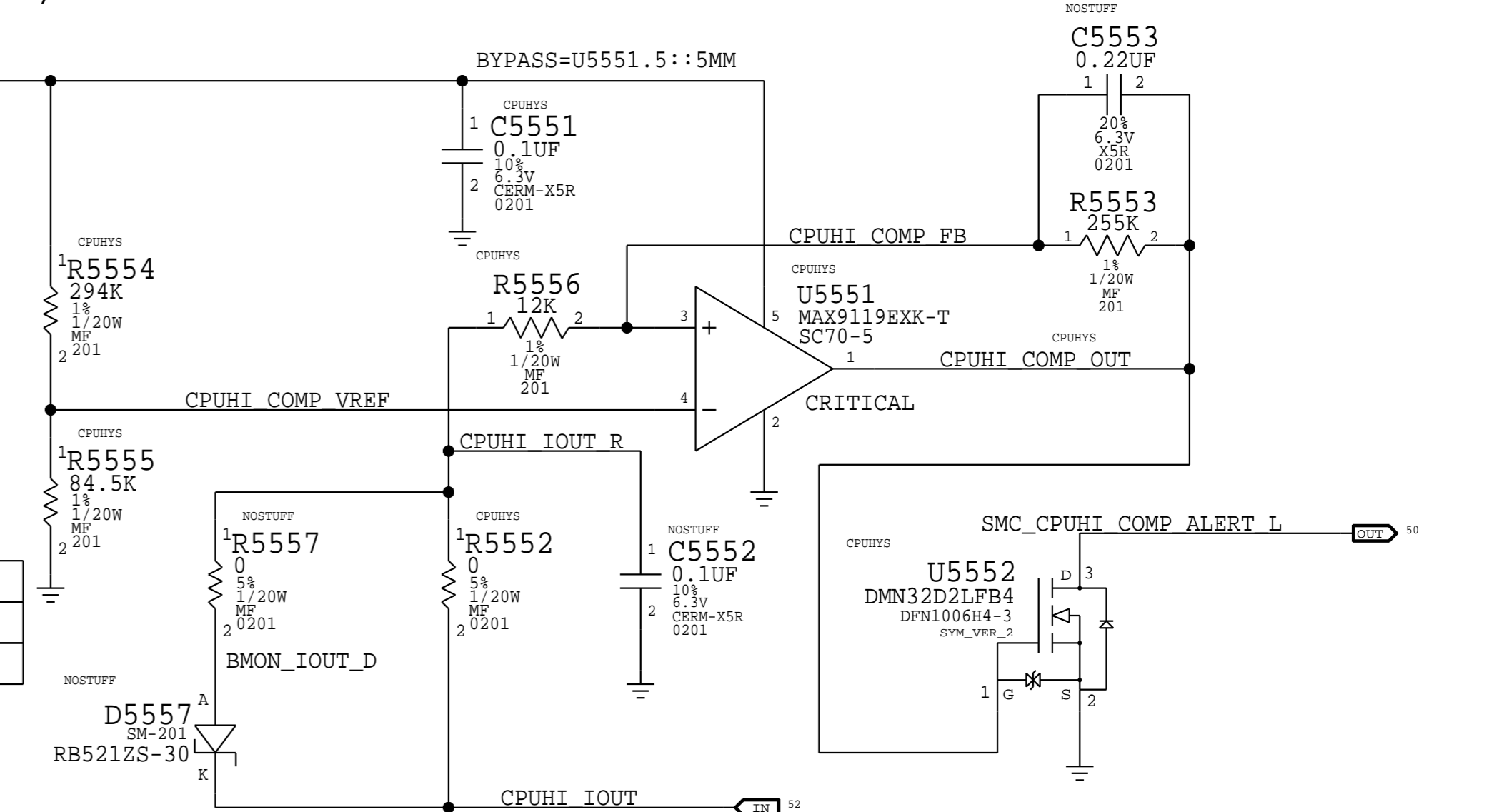
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580)
Vsense: 3 mV, Range: 0.25 A
EADC1: CH5



CPU High Side Current (ICOR) Threshold Alert

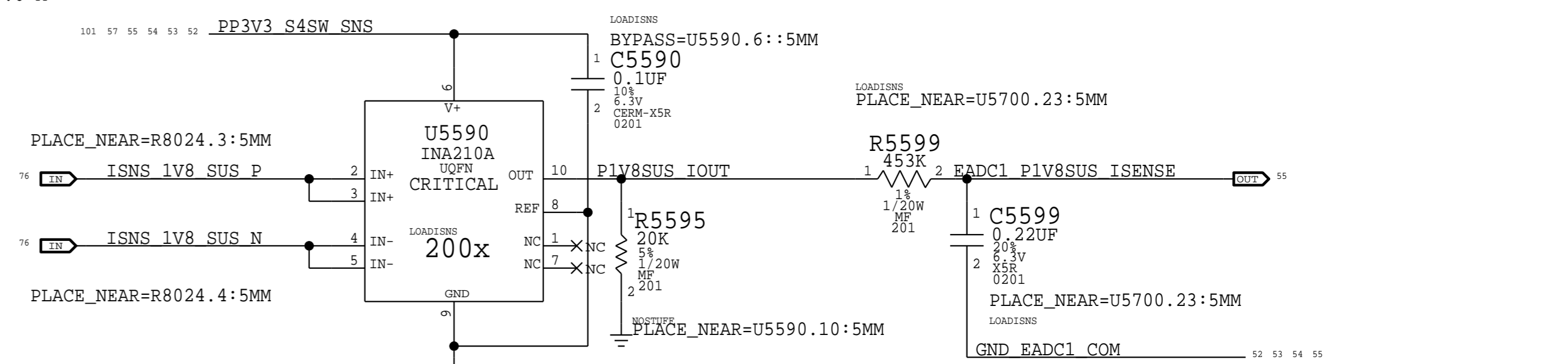
Gain: 100x
Rsense: 0.003 (R5400)
Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vt1 = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------------------------|---------------|----------|------------|
| 117S0008 | 2 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | C5569,C5519 | | LOADRC:NO |
| 117S0008 | 2 | RES,MTL FLIM,100K,1/16W,0201,SMD,LF | C5549,C5579 | | LOADRC:NO |

1.8V Current Sense (I18C)

Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
SMC ADC: 16



Power Sensors: Load Side

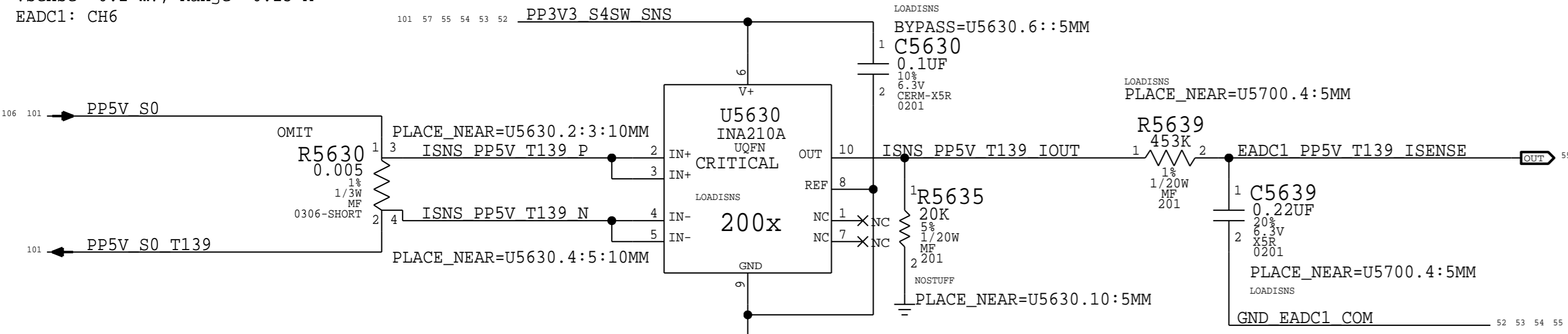
Apple Inc.

DRAGGING NUMBER: 051-00777
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 55 OF 145
SHEET: 53 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
11V ALL RIGHTS RESERVED

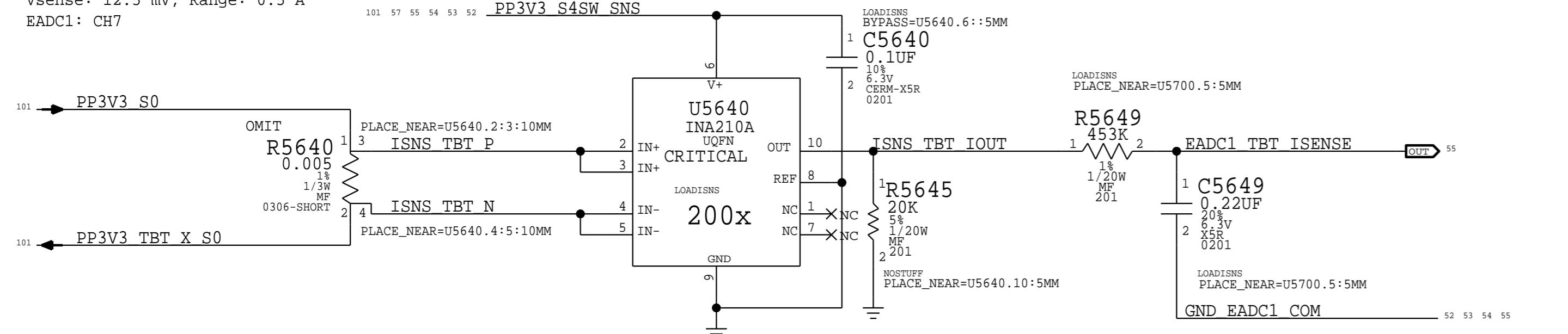
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



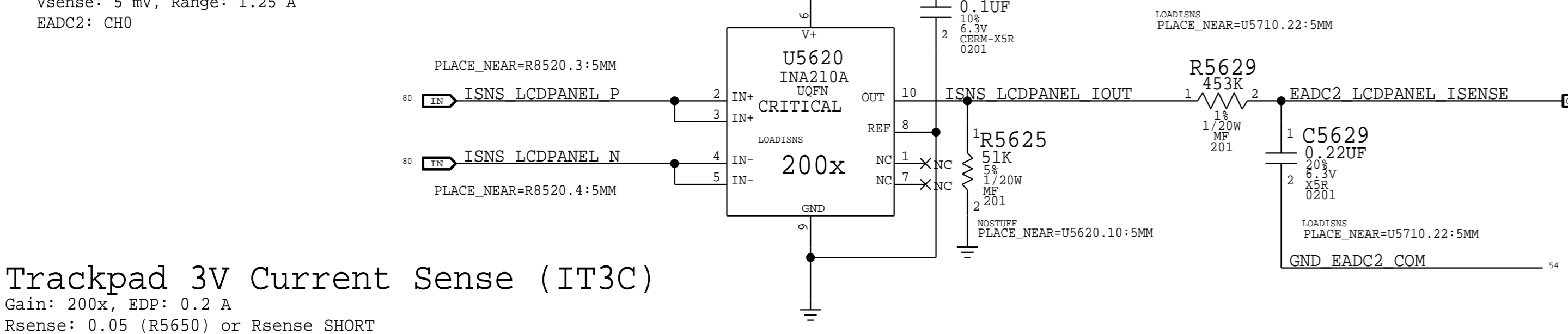
Thunderbolt TBT Current Left (IULC)

Gain: 200x, EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



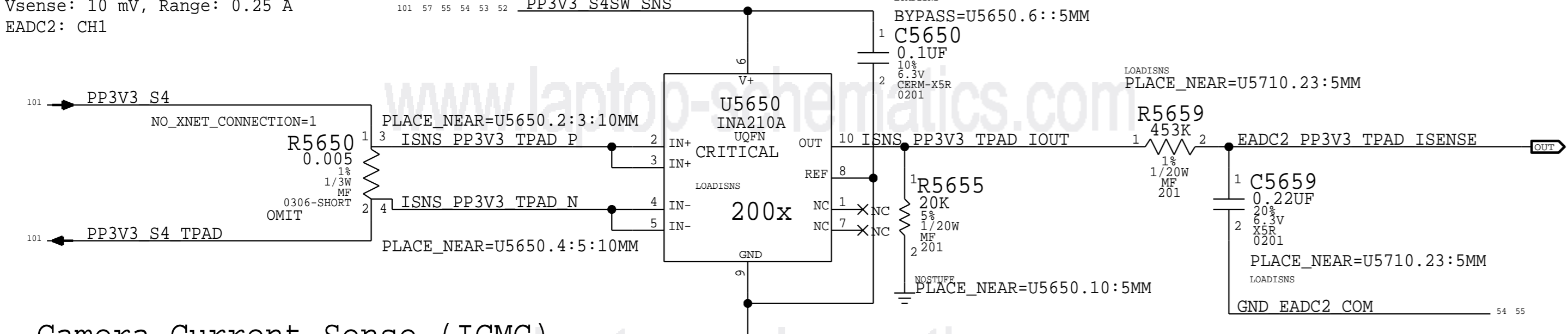
LCD Panel Current Sense (ILDC)

Gain: 200x, EDP: 1 A
RSNSE: 0.01 (R5620) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



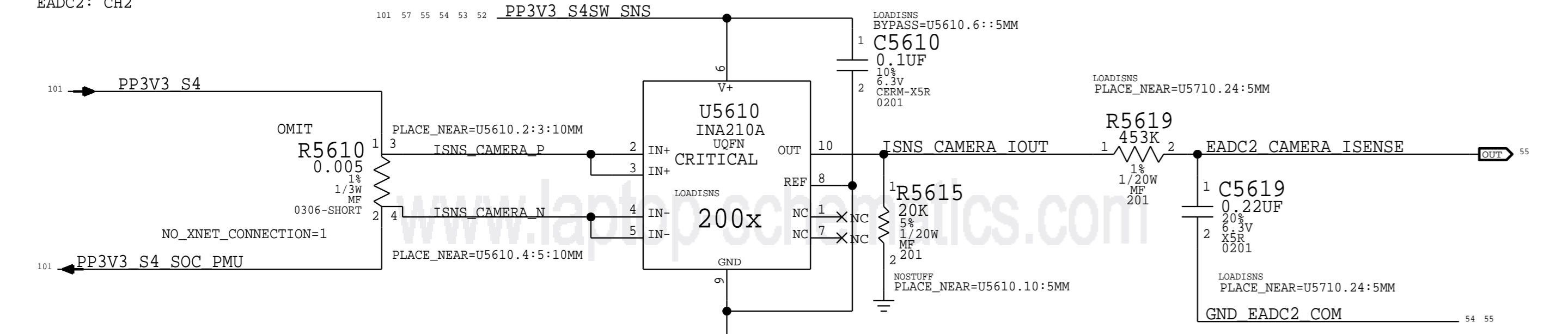
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

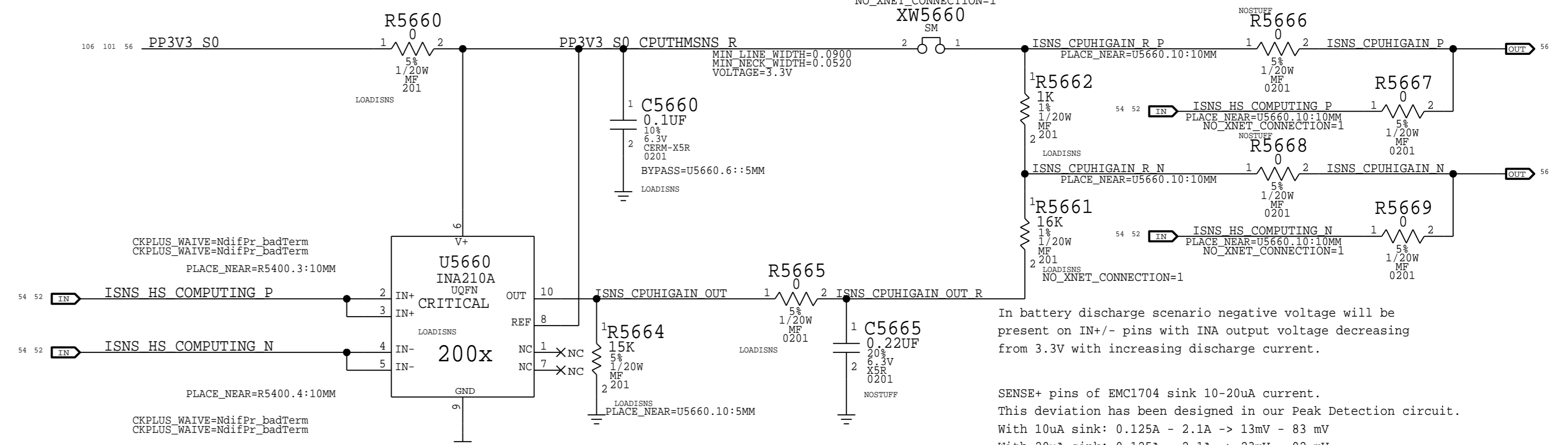


Camera Current Sense (ICMC)

Gain: 200x, EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2

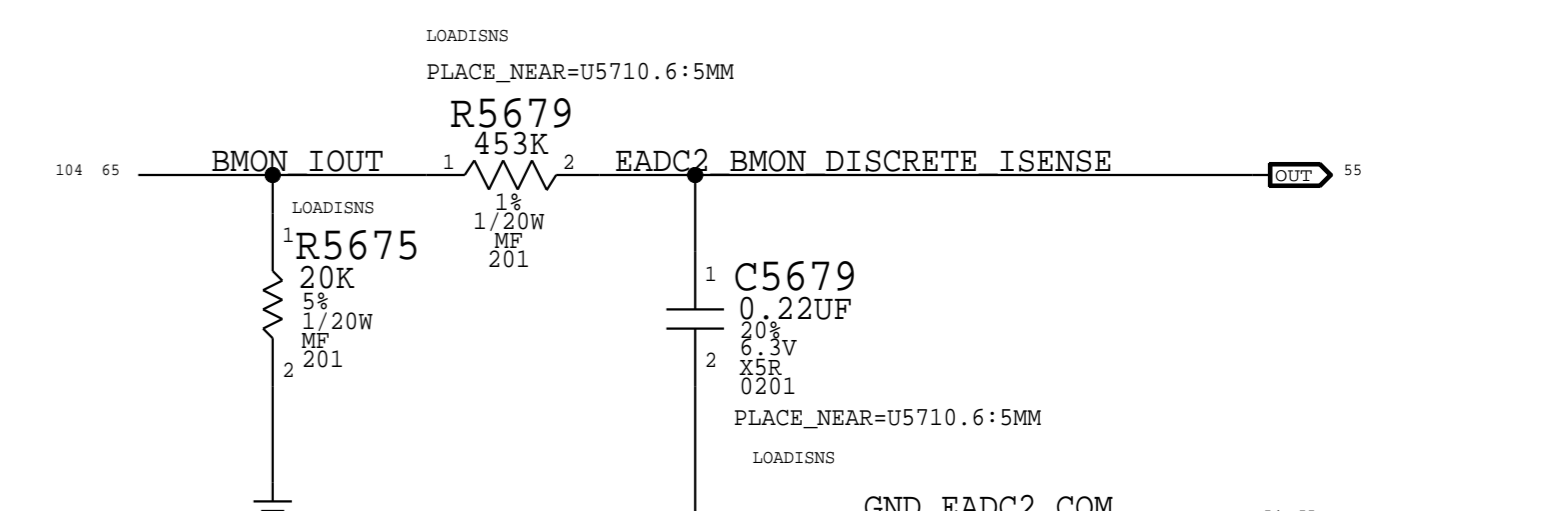


CPU High Side (IC0R) Peak Detection Support



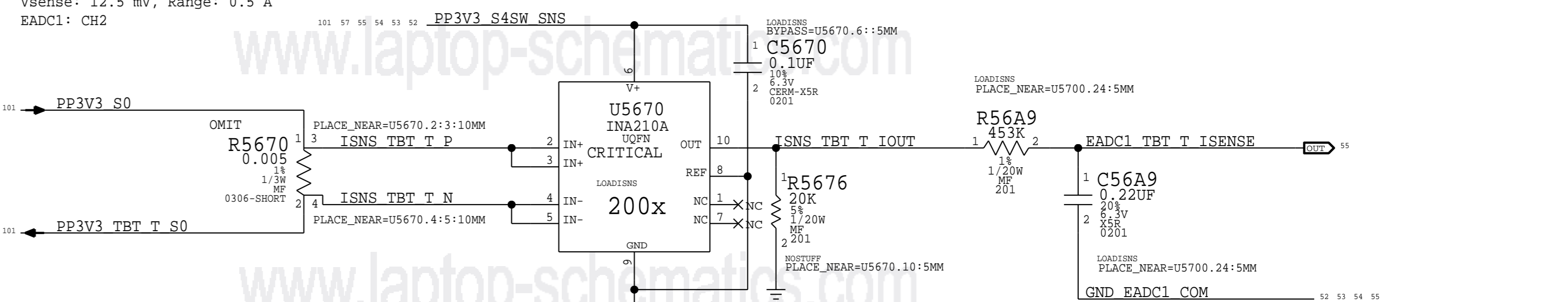
Battery Discrete Current Sense (IBOL)

Gain: 2940x, EDP: 8 A
Rsense: 0.003 (R501/R502)
Vsense: 24 mV, Range: 0.28 A
EADC2: CH5



Thunderbolt TBT Current Right (IURC)

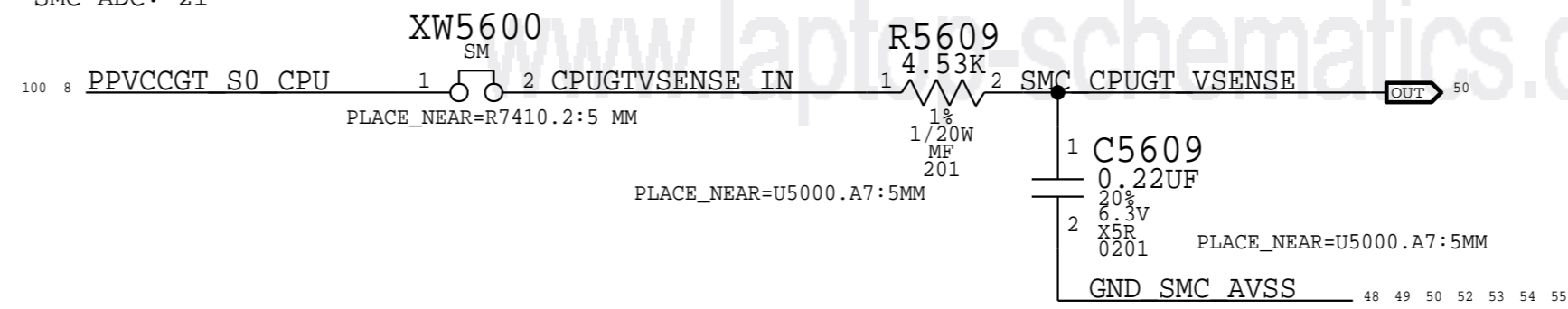
Gain: 200x, EDP: 0.5 A
Rsense: 0.025 (R5670) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|------------------------------------|---------------|----------|------------|
| 117S0008 | 2 | RES,MTL,FLM,100K,1/16W,0201,SMD,LF | C5608, C5699 | | LOADRC:NO |

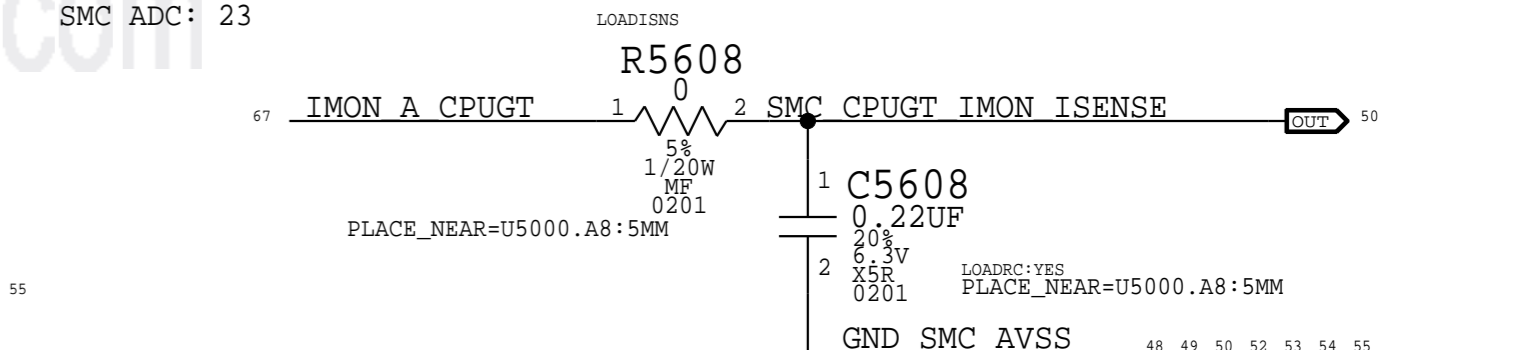
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



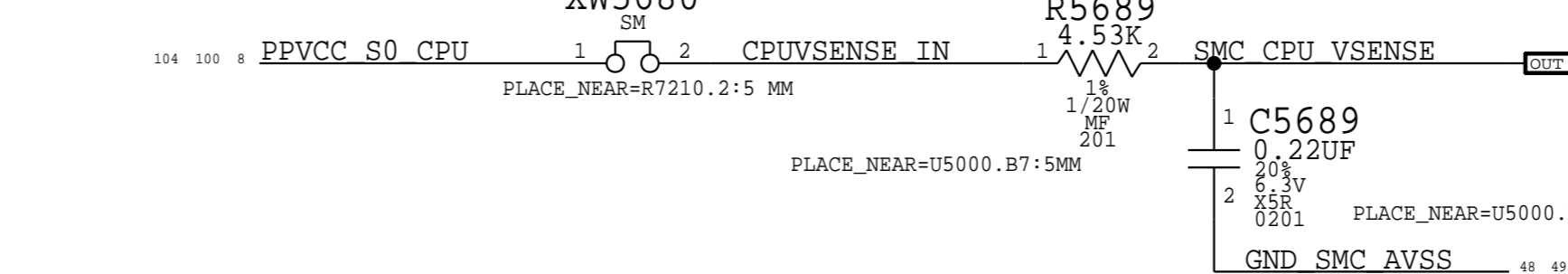
CPU GT IMON Current Sense (ICGM)

Gain: 1 A / 17.963 mV, Range: 64 A.
SMC ADC: 23



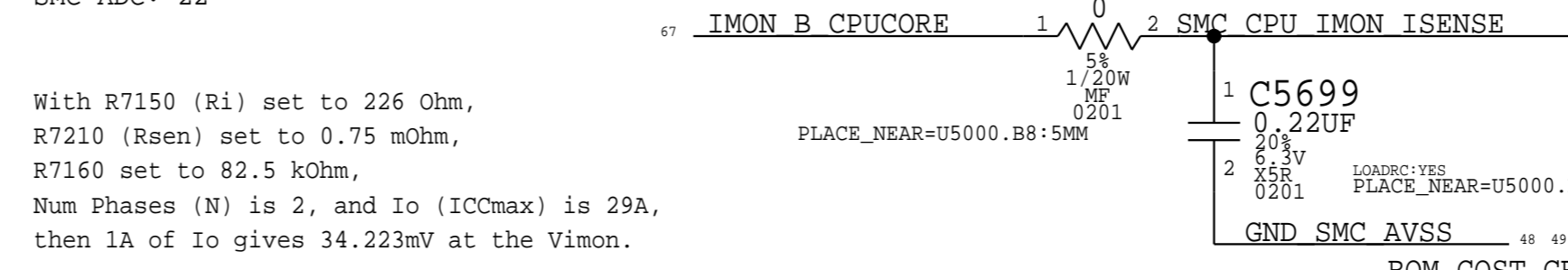
CPU Core Voltage Sense (VCAC)

SMC ADC: 20



CPU Core IMON Current Sense (ICAM)

Gain: 1 A / 34.223 mV, Range: 29 A.
SMC ADC: 22



With R7154 (Ri) set to 294 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7194 set to 84.5 kOhm,
Num Phases (N) is 3, and Io (ICmax) is 64A,
then 1A of Io gives 17.963mV at the Vimon.

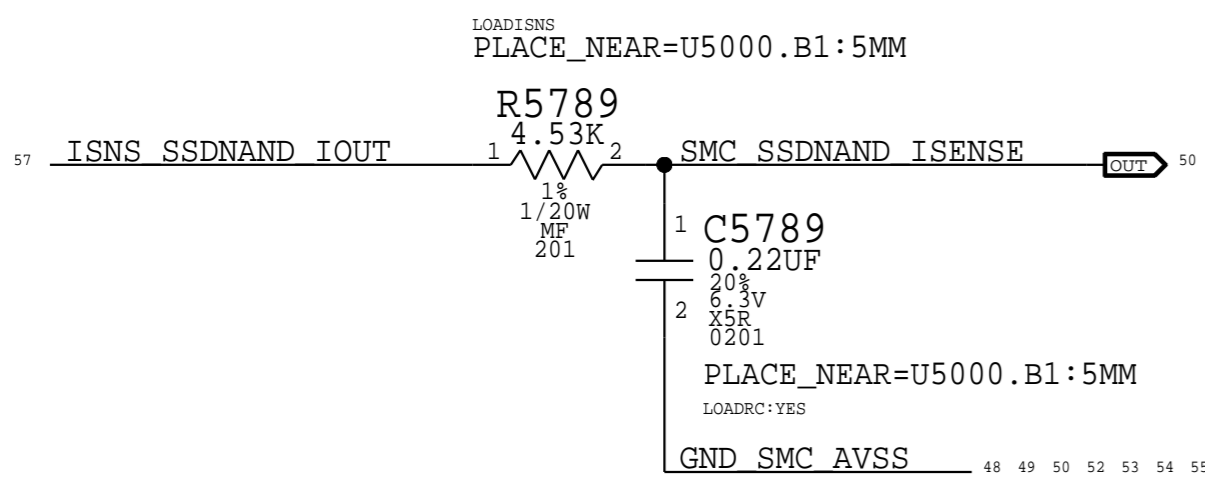
Power Sensors: Extended

Apple Inc.

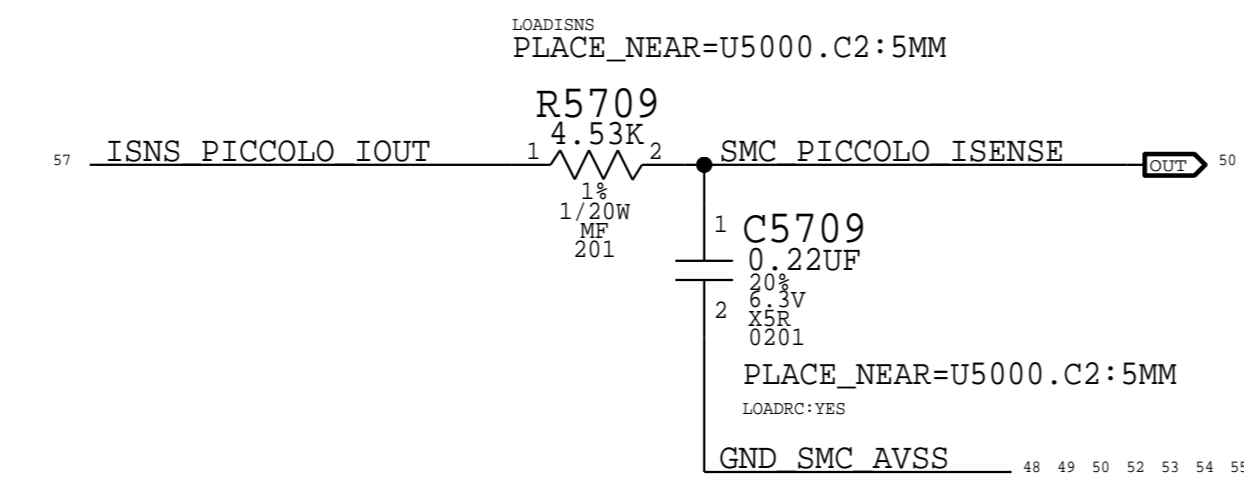
| | | | |
|----------------|-----------|--------|-------------|
| DRAWING NUMBER | 051-00777 | STR | D |
| REVISION | 9.0.0 | BRANCH | dvt-fab09-0 |
| PAGE | 56 OF 145 | SHEET | 54 OF 119 |

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
11V ALL RIGHTS RESERVED

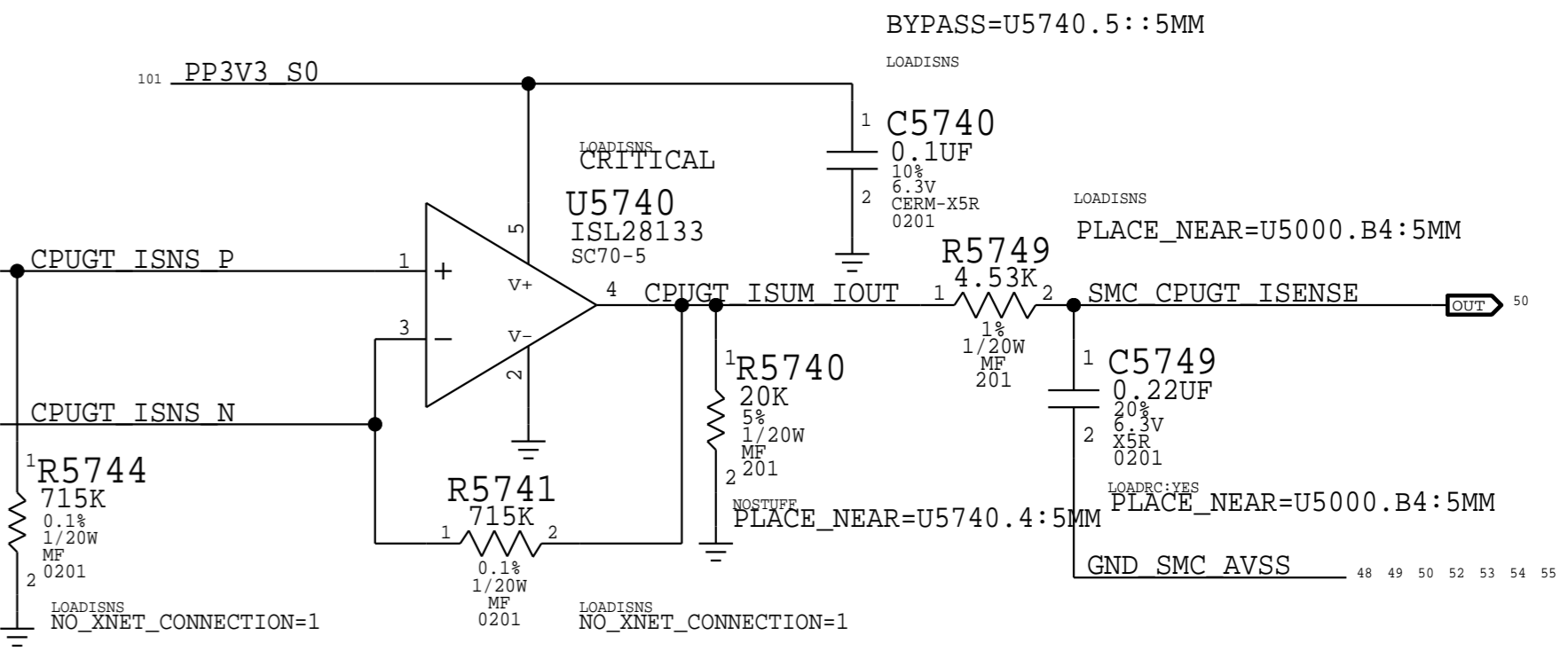
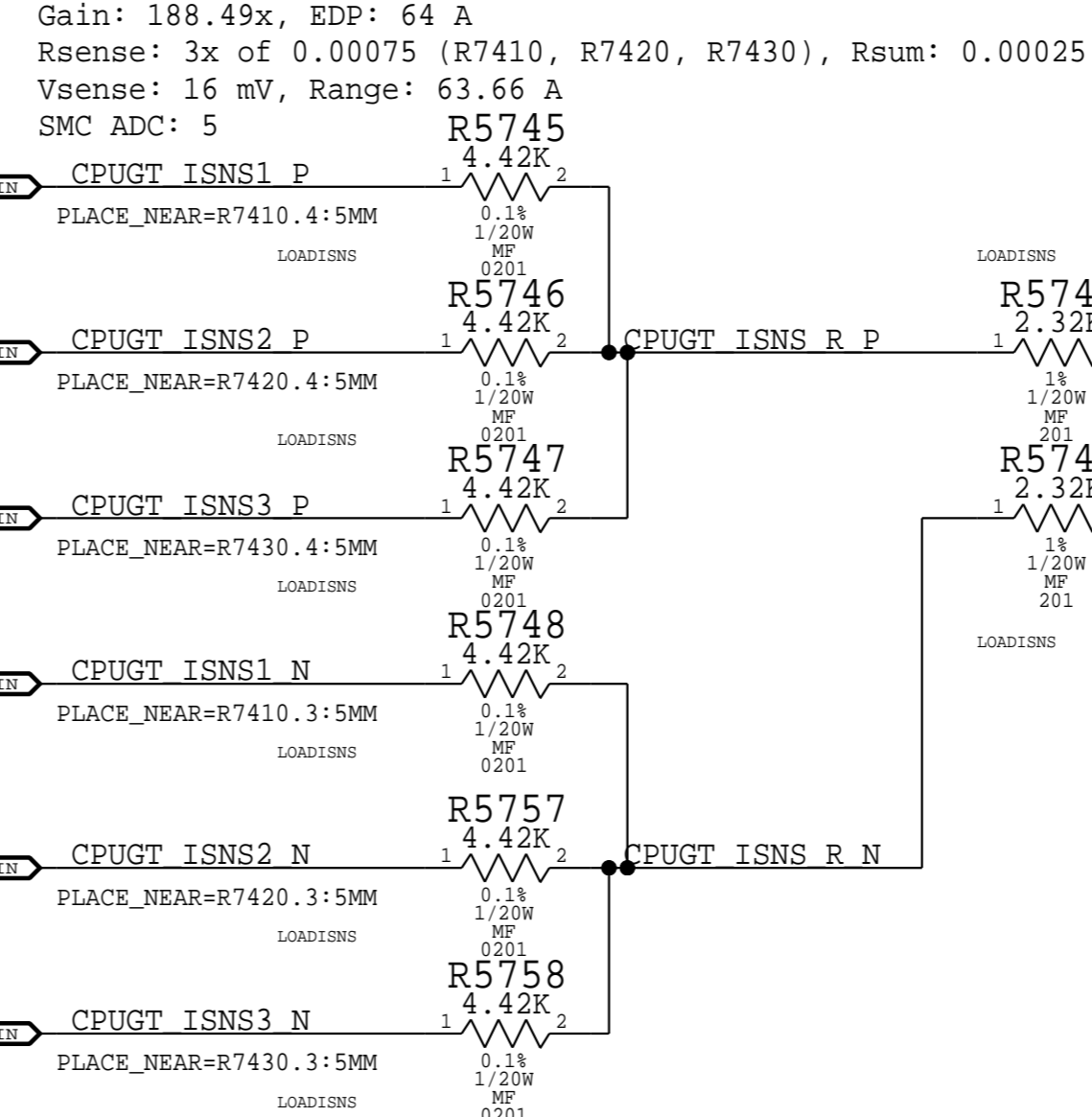
NAND Current Sense (IHNC)



PICCOLO Current Sense (IHCC)

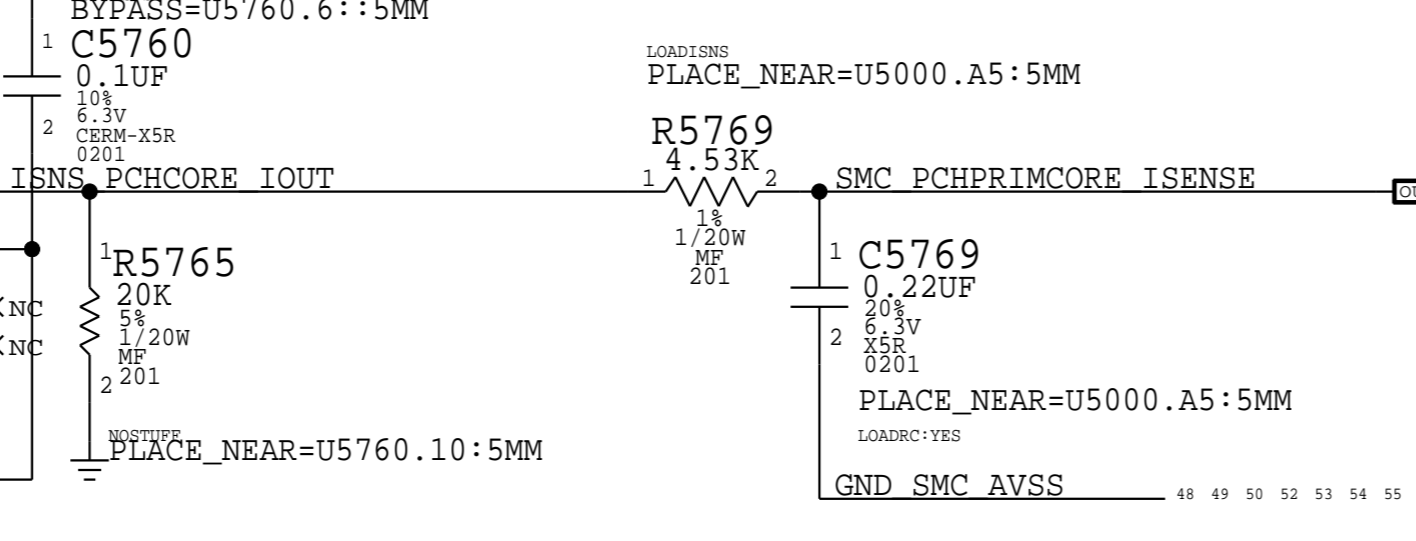
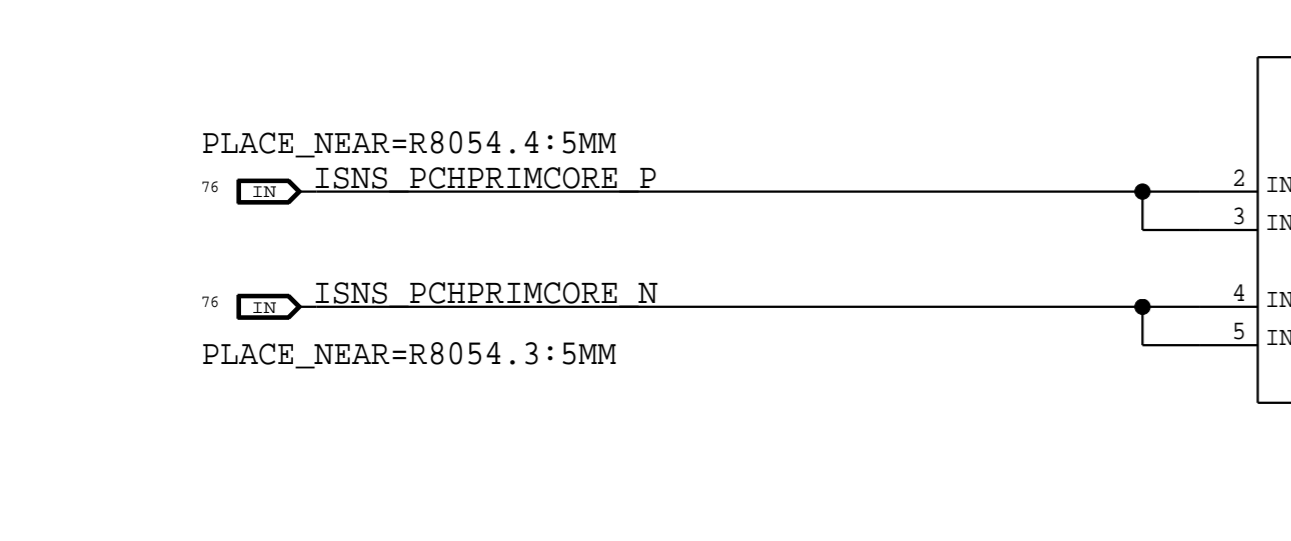


CPU GT+GTX Current Sense (ICGC)



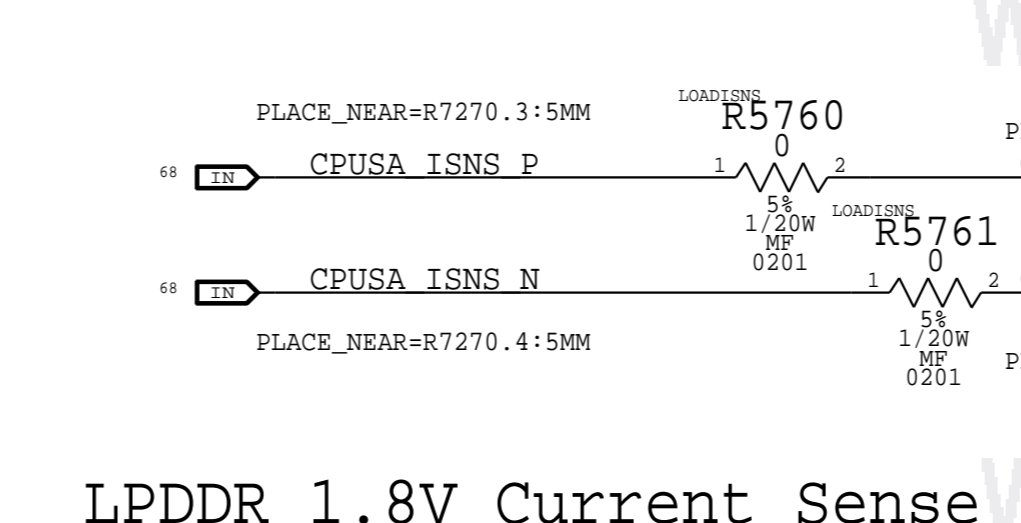
PCH PrimeCore Current Sense (ISCC)

Gain: 200x, EDP: 2.574 A
Rsense: 0.005 (R8054)
Vsense: 12.87 mV, Range: 3 A
SMC ADC: 15



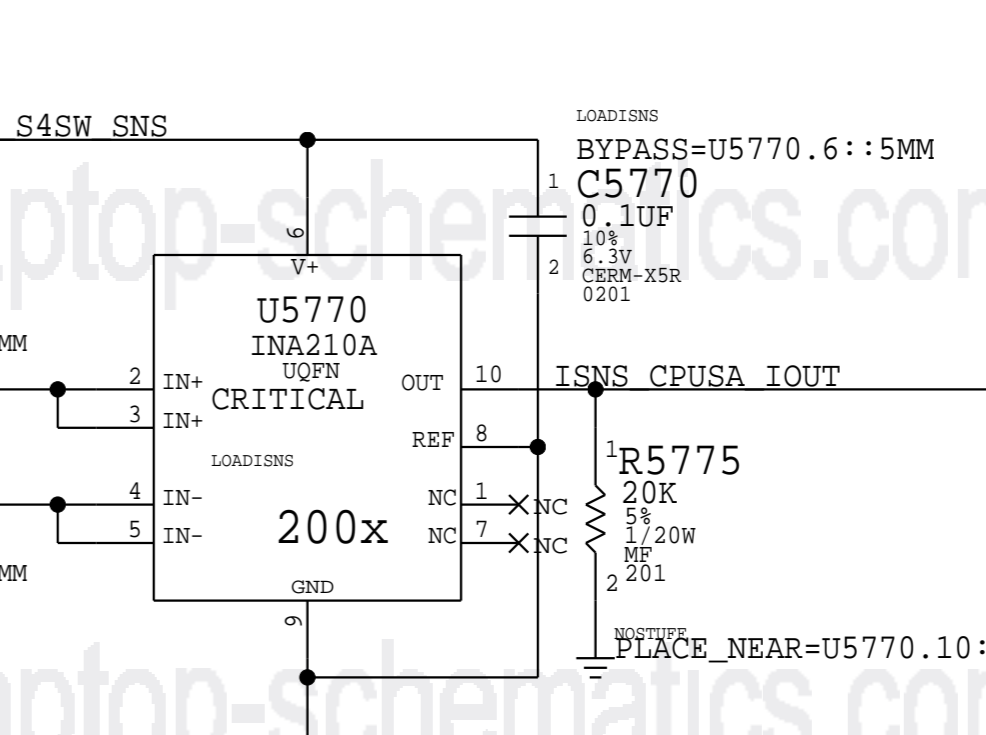
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 5.1 A
Rsense: 0.002 (R7270)
Vsense: 10.2 mV, Range: 7.5 A
SMC ADC: 19



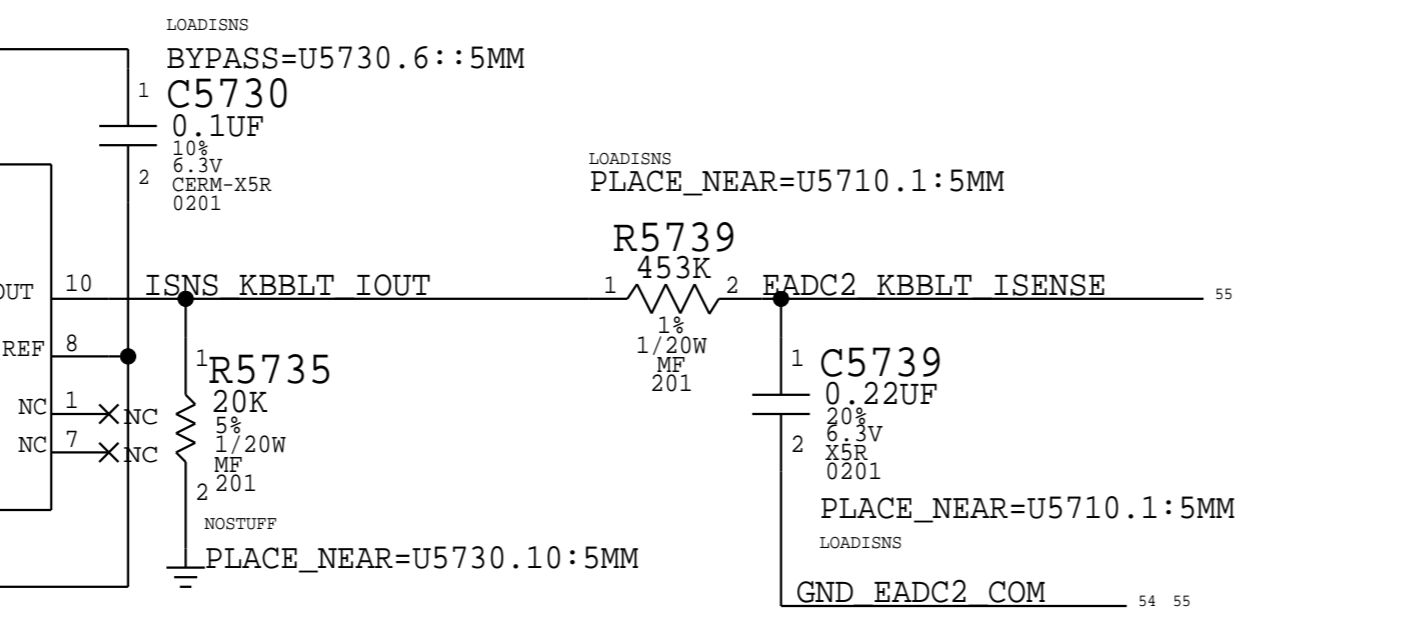
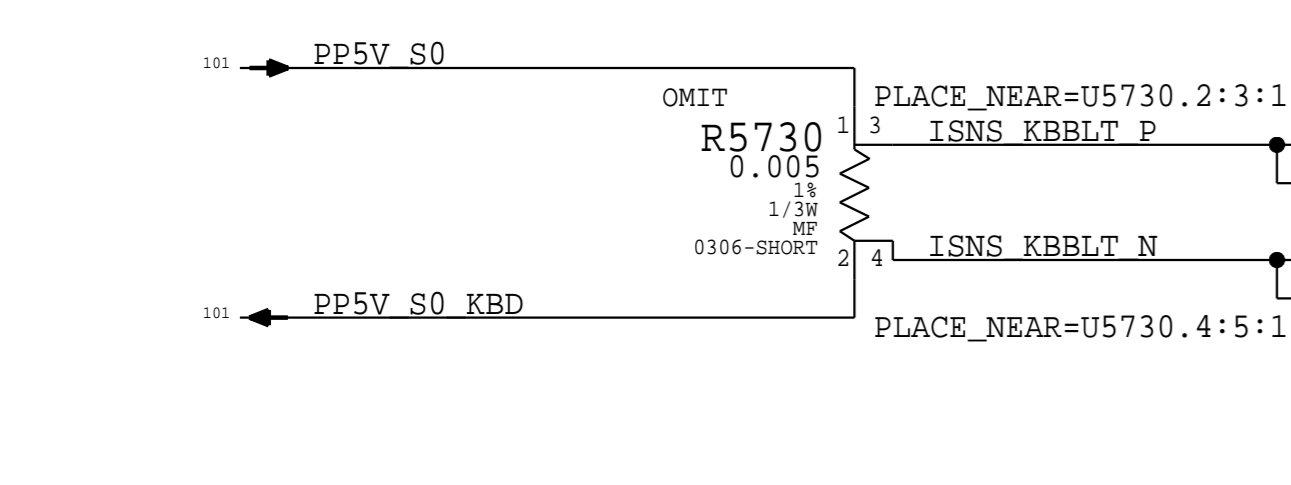
CPU SA Voltage Sense (VCSC)

SMC ADC: 17



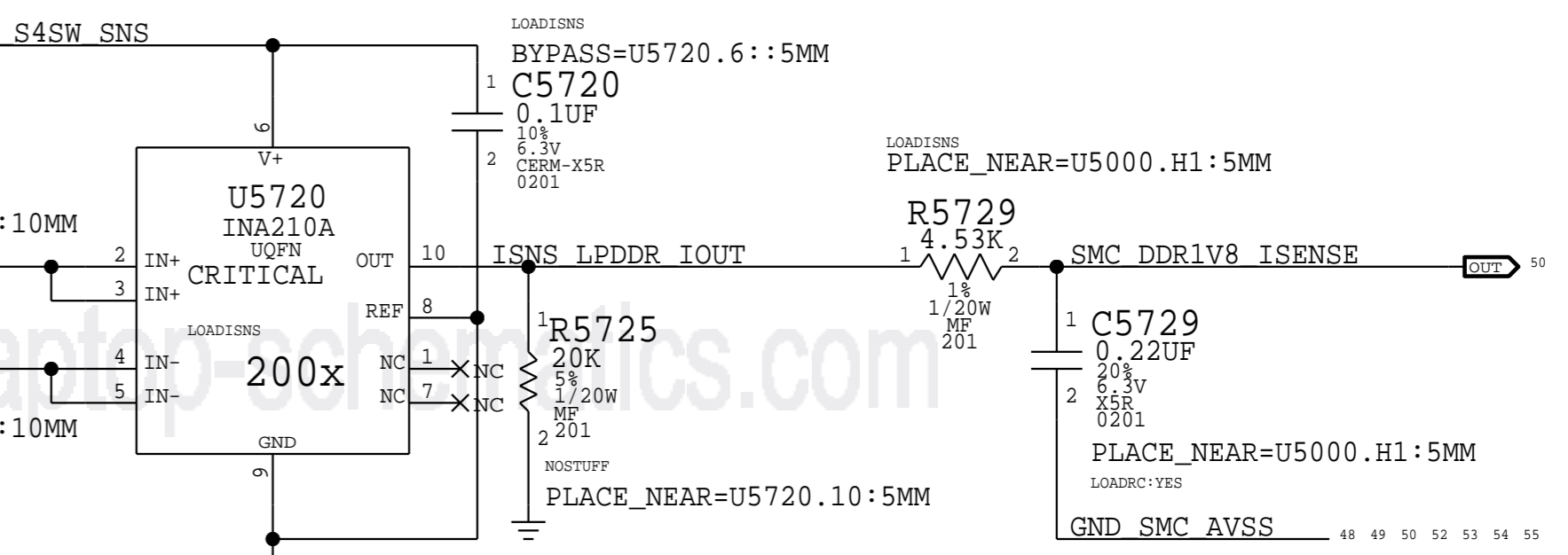
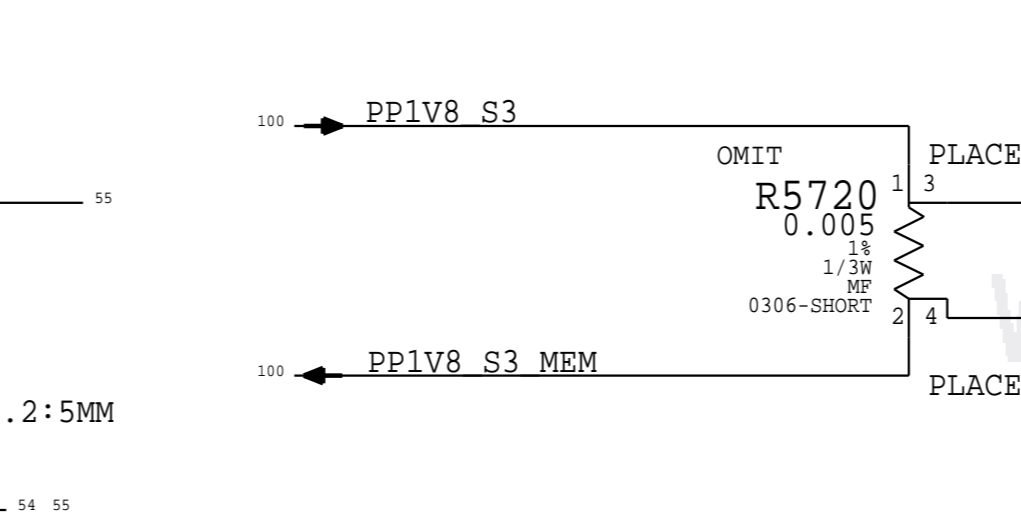
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



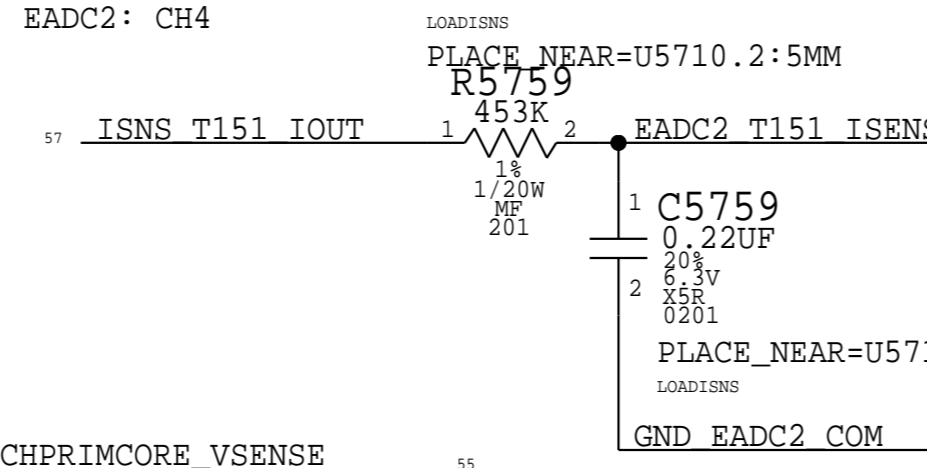
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 16



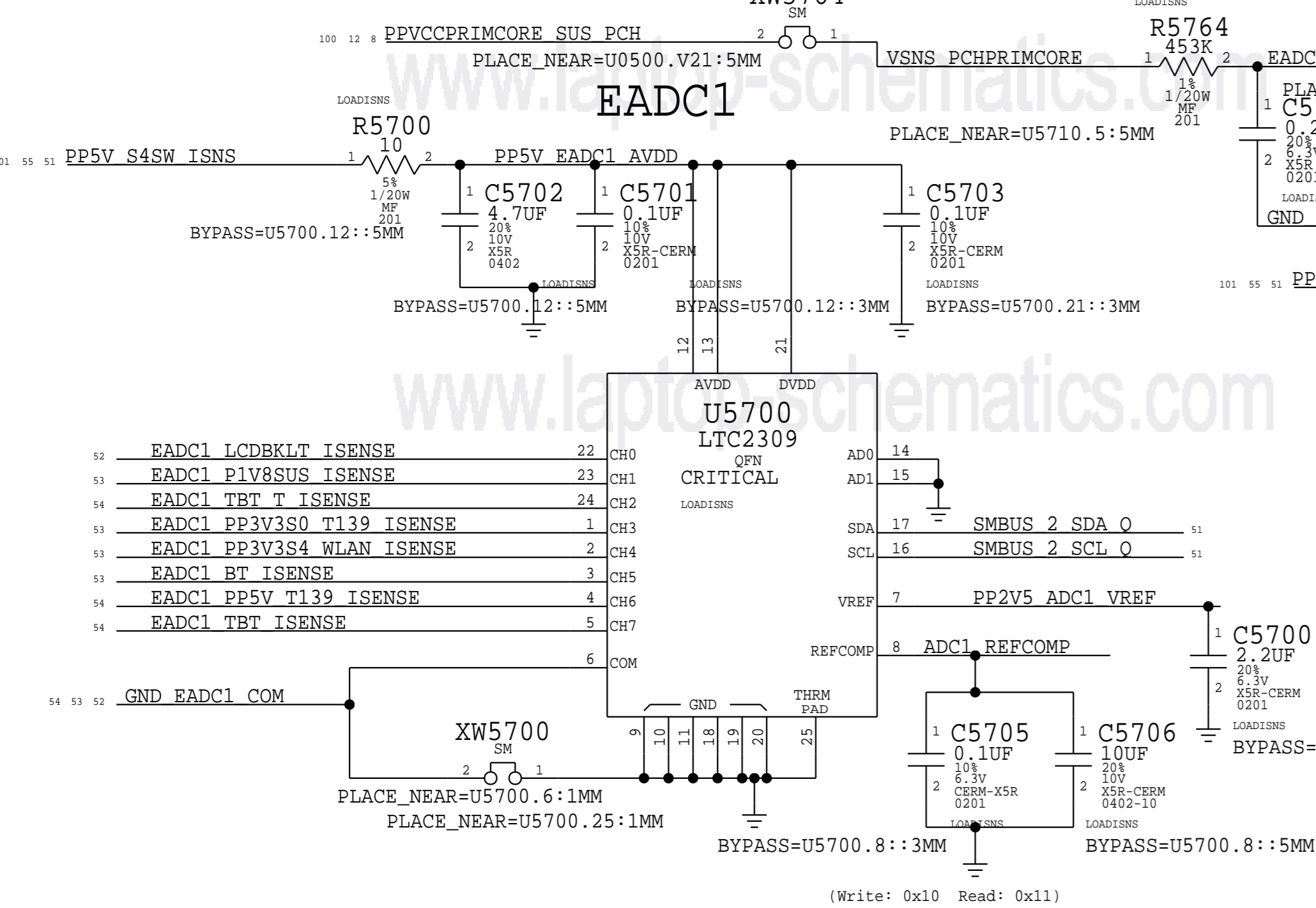
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------------------------|---------------|----------|------------|
| 117S0008 | 2 | RES,MTL,FLIM,100K,1/16W,0201,SMD,LF | C5769,C5778 | | LOADRC:NO |
| 117S0008 | 2 | RES,MTL,FLIM,100K,1/16W,0201,SMD,LF | C5749,C5779 | | LOADRC:NO |
| 117S0008 | 2 | RES,MTL,FLIM,100K,1/16W,0201,SMD,LF | C5729,C5799 | | LOADRC:NO |
| 117S0008 | 2 | RES,MTL,FLIM,100K,1/16W,0201,SMD,LF | C5709,C5789 | | LOADRC:NO |

T151 Current Sense (I1DC)

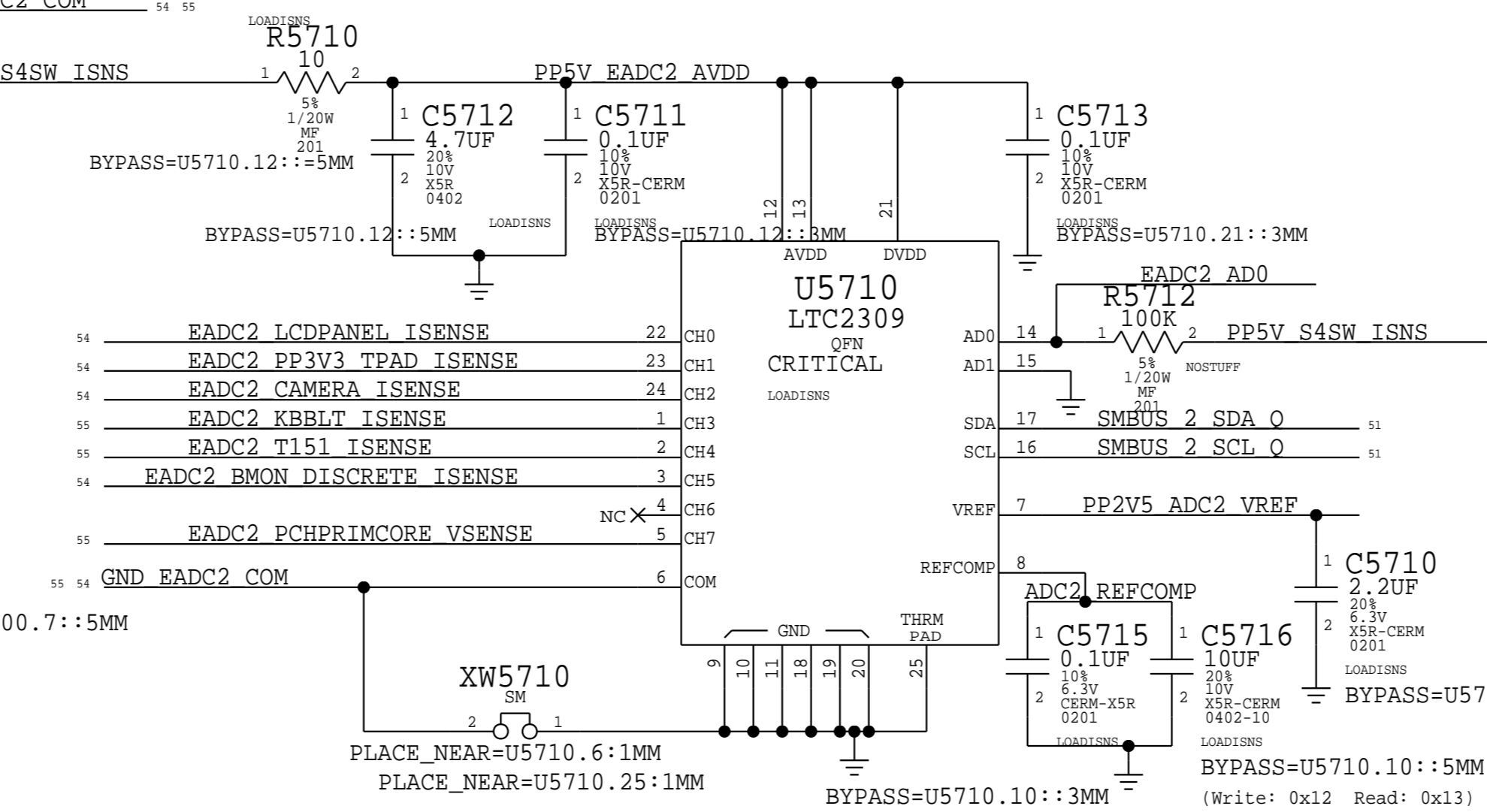


PCH PrimeCore Voltage Sense (VSCC)

EADC2: CH7

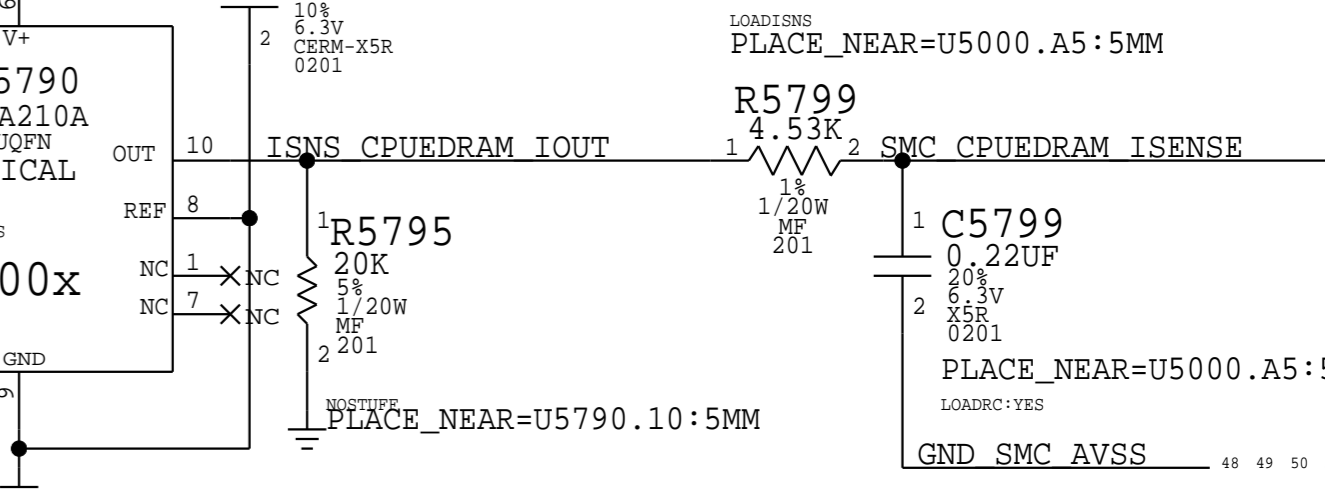


EADC2



CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 4.5 A
Rsense: 0.003 (R7718)
Vsense: 13.5 mV, Range: 5 A
SMC ADC: 10



Power Sensors: Extended 2

Apple Inc.

051-00777

9.0.0

dvt-fab09-0

57 OF 145

55 OF 119

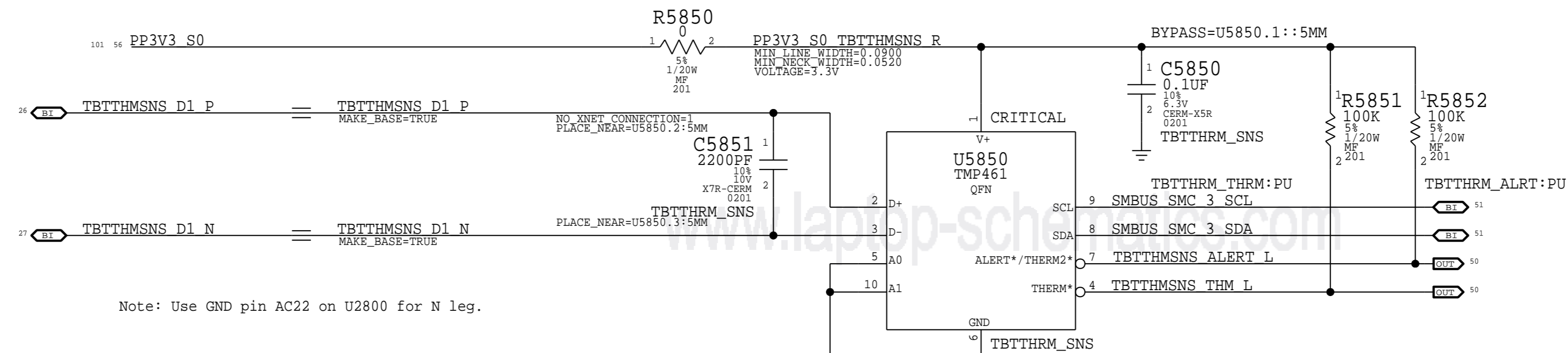
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED

Thermal Sensor A: Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TBT1)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5850 I2C Address: TMP461 is 0x90/0x91.

Note: Use GND pin AC22 on U2800 for N leg.

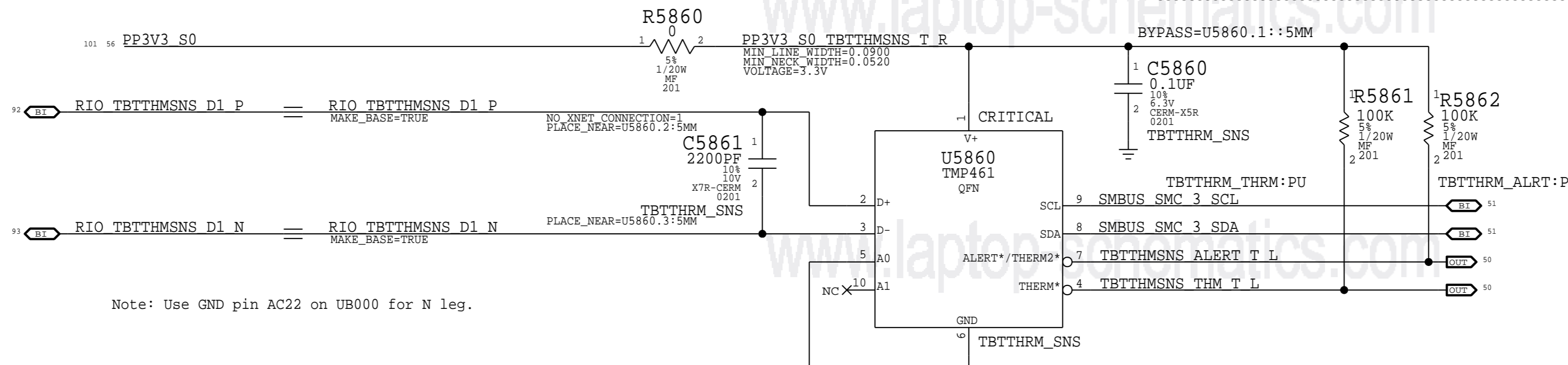
Placement Note:
Place U5850 on the BOTTOM side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C: Thunderbolt Die, Air Flow Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TBT2)

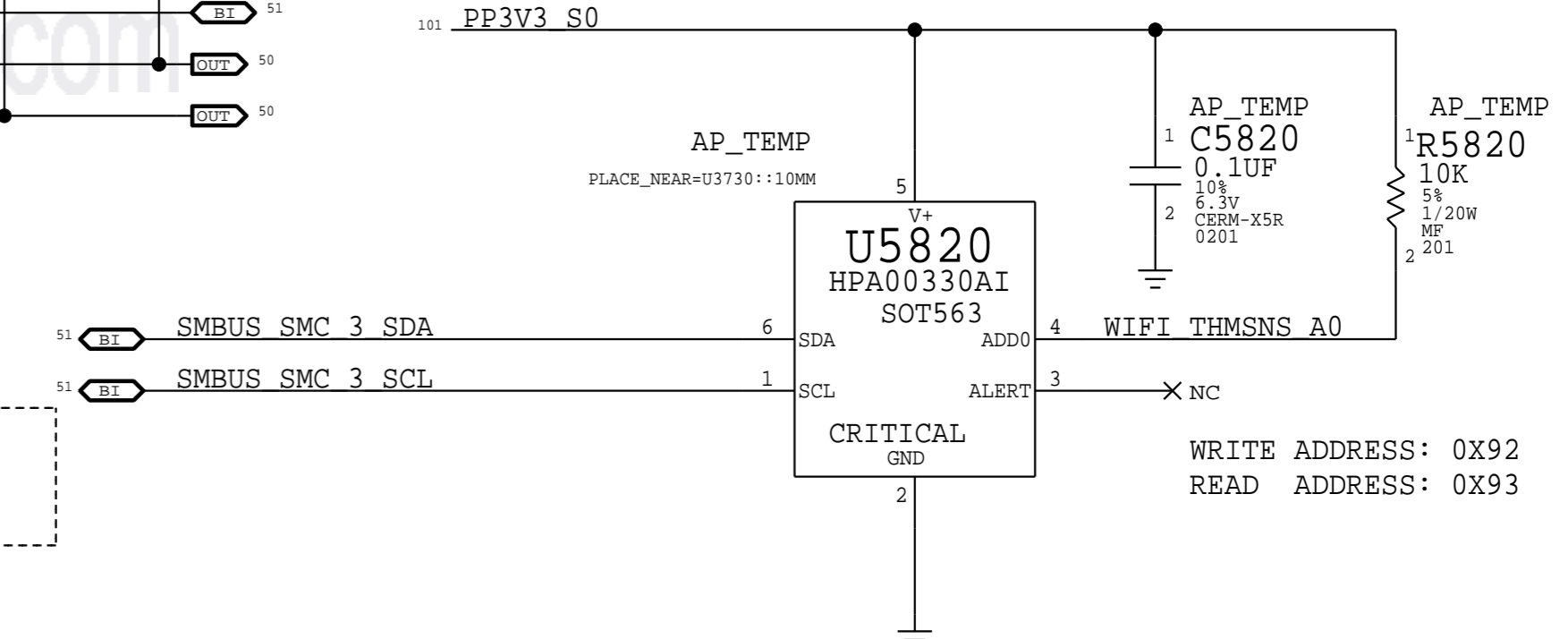
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



U5860 I2C Address: TMP461 is 0x96/0x97.

Placement Note:
Place U5860 on the BOTTOM side, on the right portion of the board, 1" to the left of USB connector.

X100 PROXIMITY



WRITE ADDRESS: 0x92
READ ADDRESS: 0x93

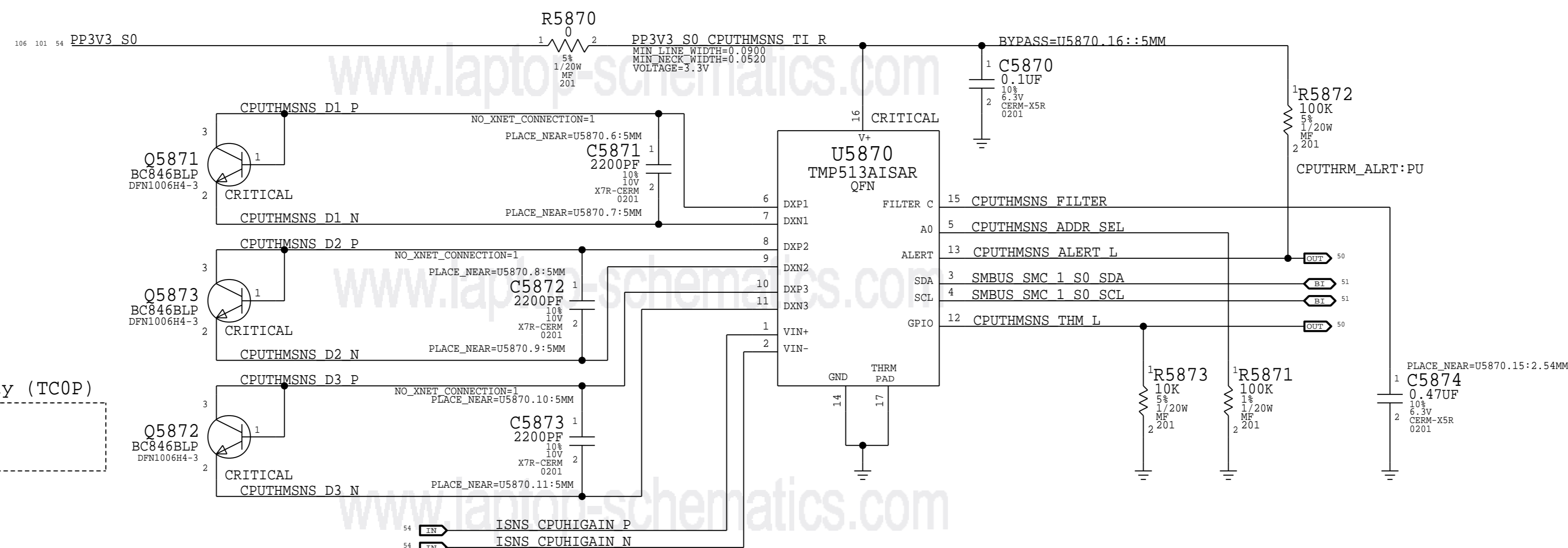
Placement note:
PLACE U5820 ON BOTTOM NEAR X100

Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.



Thermal Diode: CPU Proximity (TCOP)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Diode: Memory Proximity (TMOP)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Sensor: Fin Stack Right (Th1H)

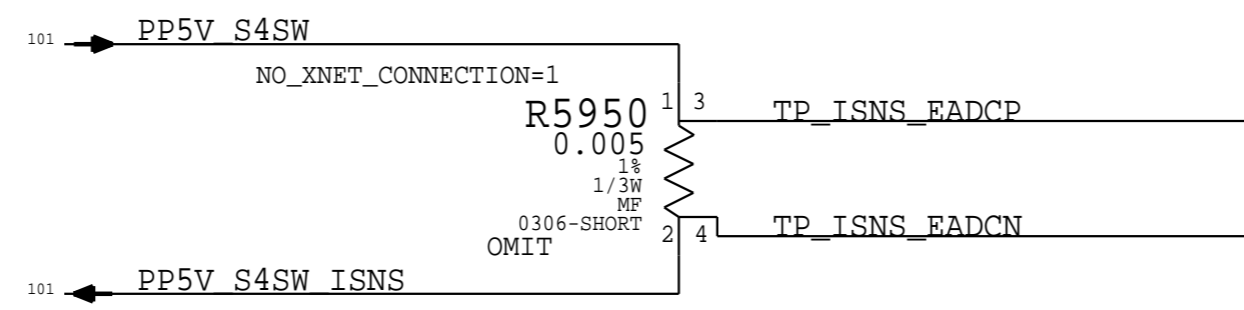
Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

BOM_COST_GROUP=SENSORS

| Thermal Sensors | | DRAWING NUMBER | STR |
|---|--|----------------|-----------|
| Apple Inc. | | 051-00777 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED | | REVISION | PAGE |
| | | 9.0.0 | 58 OF 145 |
| | | BRANCH | SHEET |
| | | dvt-fab09-0 | 56 OF 119 |

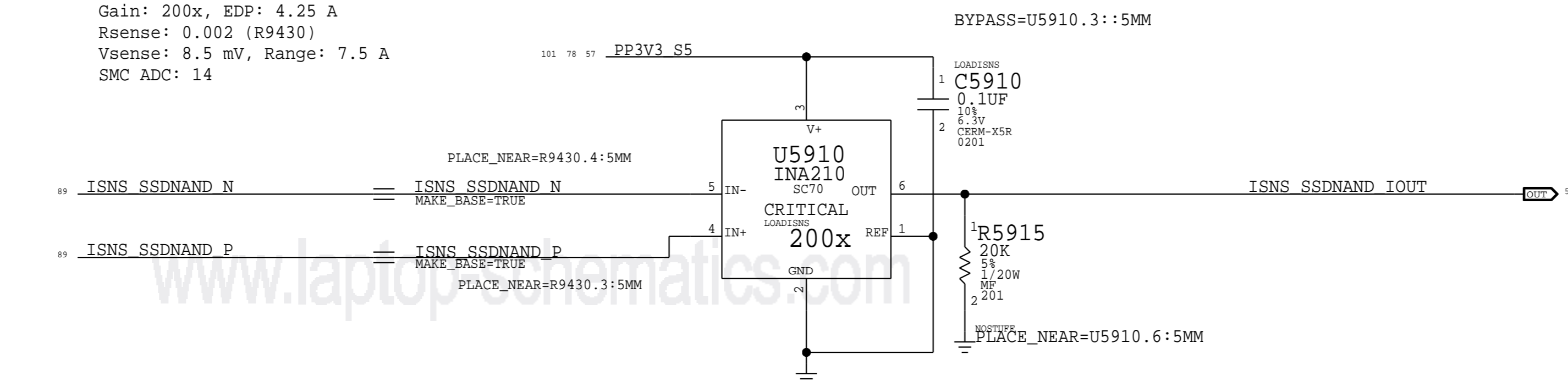
EADC Current Sense (IADC)

Gain: 200x, EDP: 200m A
Rsense: 0.050 (R5950) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH7



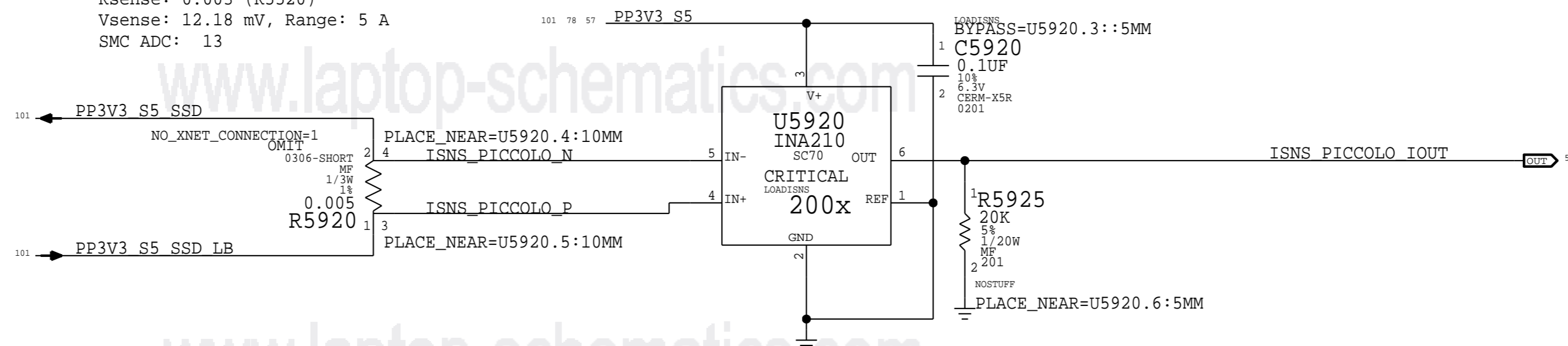
NAND Current Sense (IHNC)

Gain: 200x, EDP: 4.25 A
Rsense: 0.002 (R9430)
Vsense: 8.5 mV, Range: 7.5 A
SMC ADC: 14



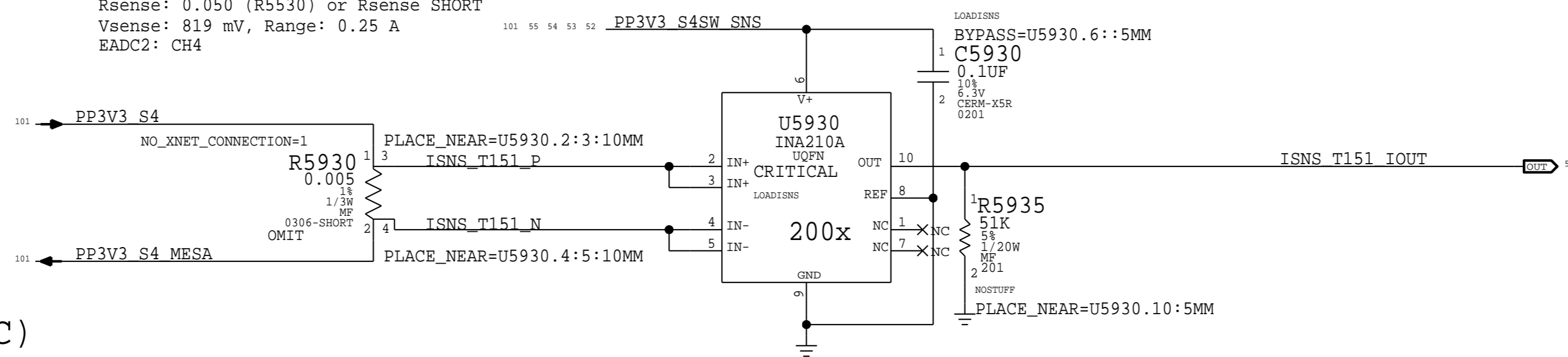
Piccolo Current Sense (IHCC)

Gain: 200x, EDP: 4.06 A
Rsense: 0.003 (R5520)
Vsense: 12.18 mV, Range: 5 A
SMC ADC: 13



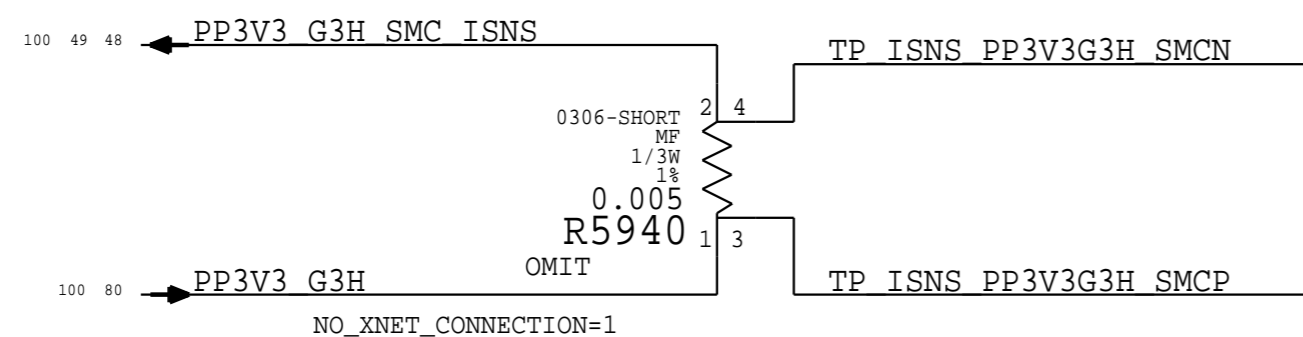
T151 Current Sense (IICD)

Gain: 200x, EDP: 163.8m A
Rsense: 0.050 (R5530) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



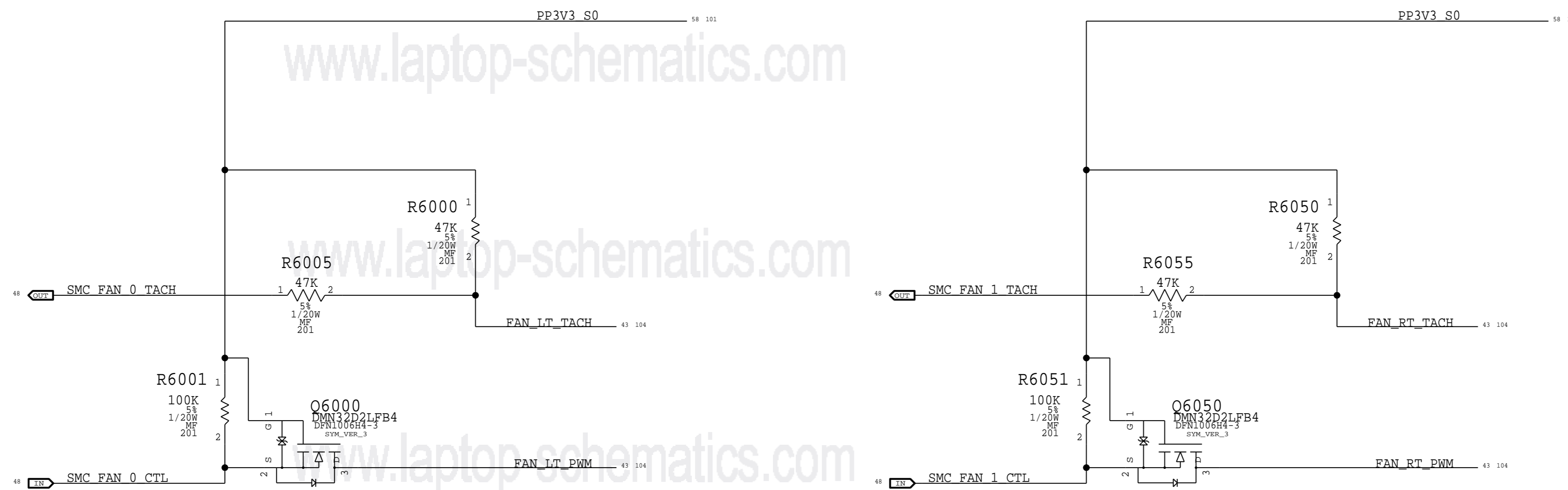
SMC Current Sense (ISMC)

Gain: 391.67x, EDP: 0.2 A
Rsense: 0.05 (R5940) or Rsense SHORT
Vsense: 10 mV, Range: 0.21A
EADC2: CH6

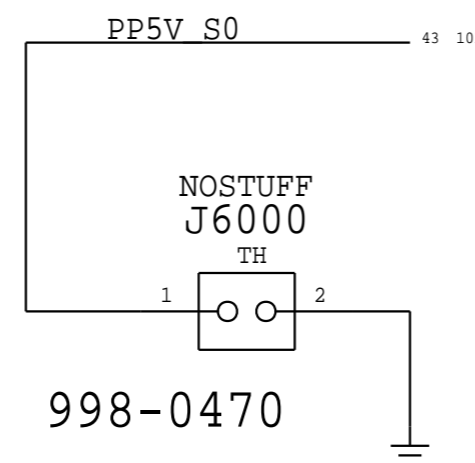


| | | |
|---|----------------|-------------|
| PAGE TITLE Power Sensors:Extended 3 | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 59 OF 145 |
| | SHEET | 57 OF 119 |

FAN CONTROL



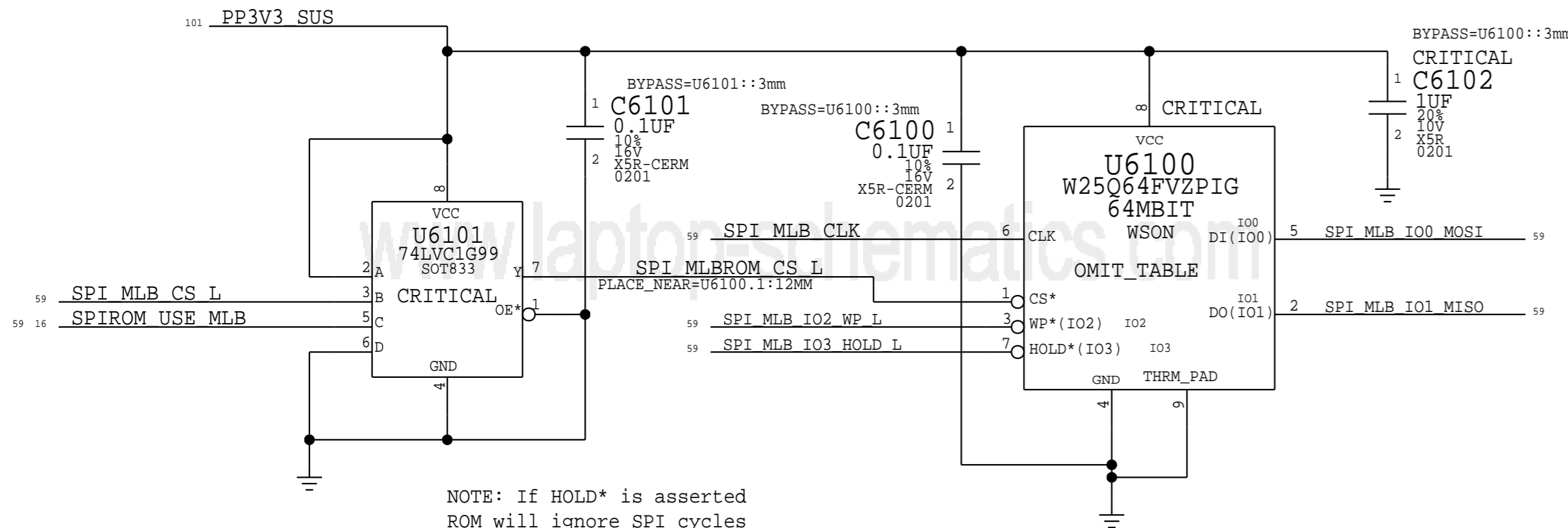
FOR DEBUG FAN POWER



| | | | |
|---|--|----------------------|-------------|
| EVM_MASTER=079 JACK | | SYMC_DATE=08/21/2015 | |
| PAGE TITLE | | | |
| Fans | | DRAWING NUMBER | SIZE |
| Apple Inc. | | 051-00777 | D |
| | | REVISION | |
| | | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | |
| | | PAGE | dvt-fab09-0 |
| | | | 60 OF 145 |
| | | SHEET | 58 OF 119 |

SPI ROM

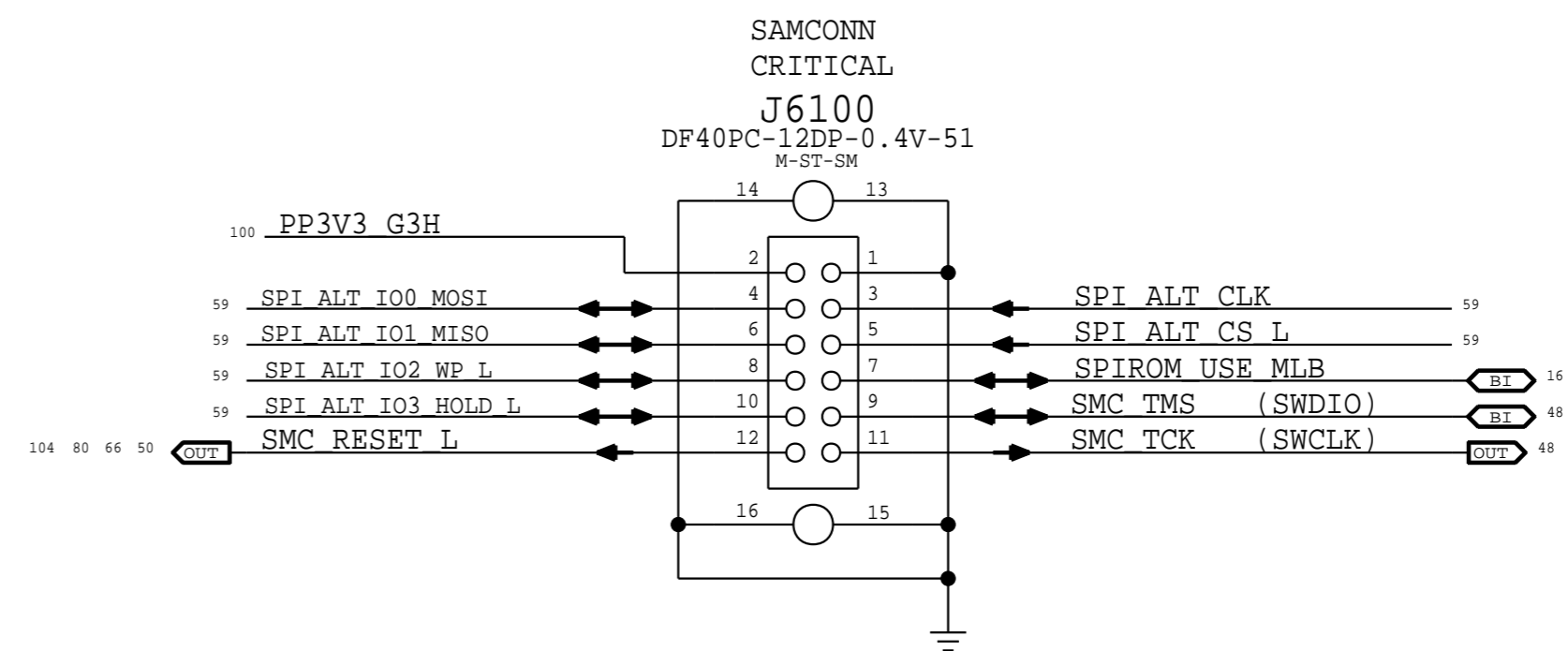
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



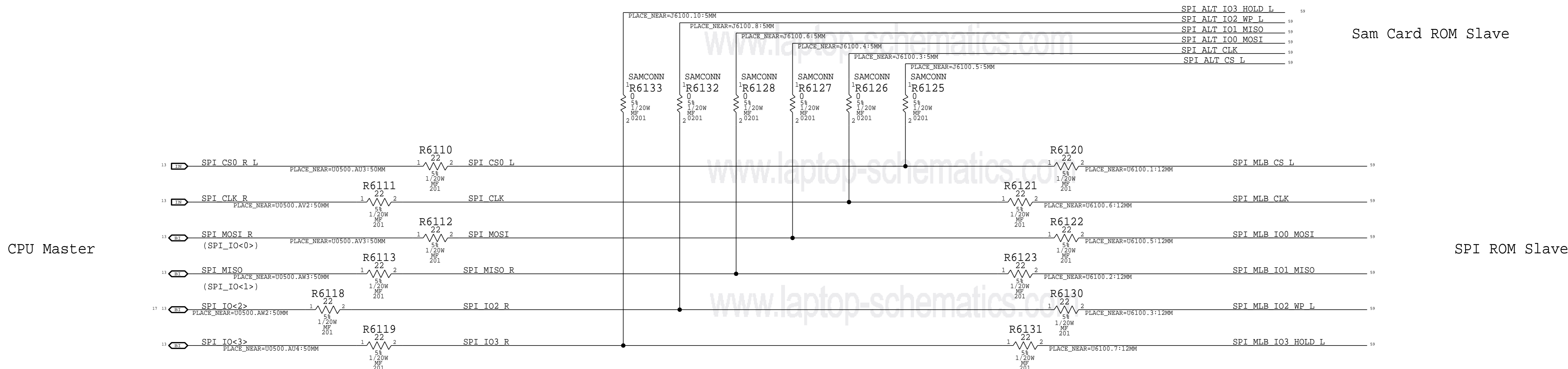
NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE

SPI Debug Connector

| | | | | |
|---|----------------|-----------|-------------|---|
| | DRAWING NUMBER | 051-00777 | STEP | D |
| | REVISION | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED | | PAGE | 61 OF 145 | |
| | | SHEET | 59 OF 119 | |

BOM_COST_GROUP=CPU & CHIPSET

D

D

C

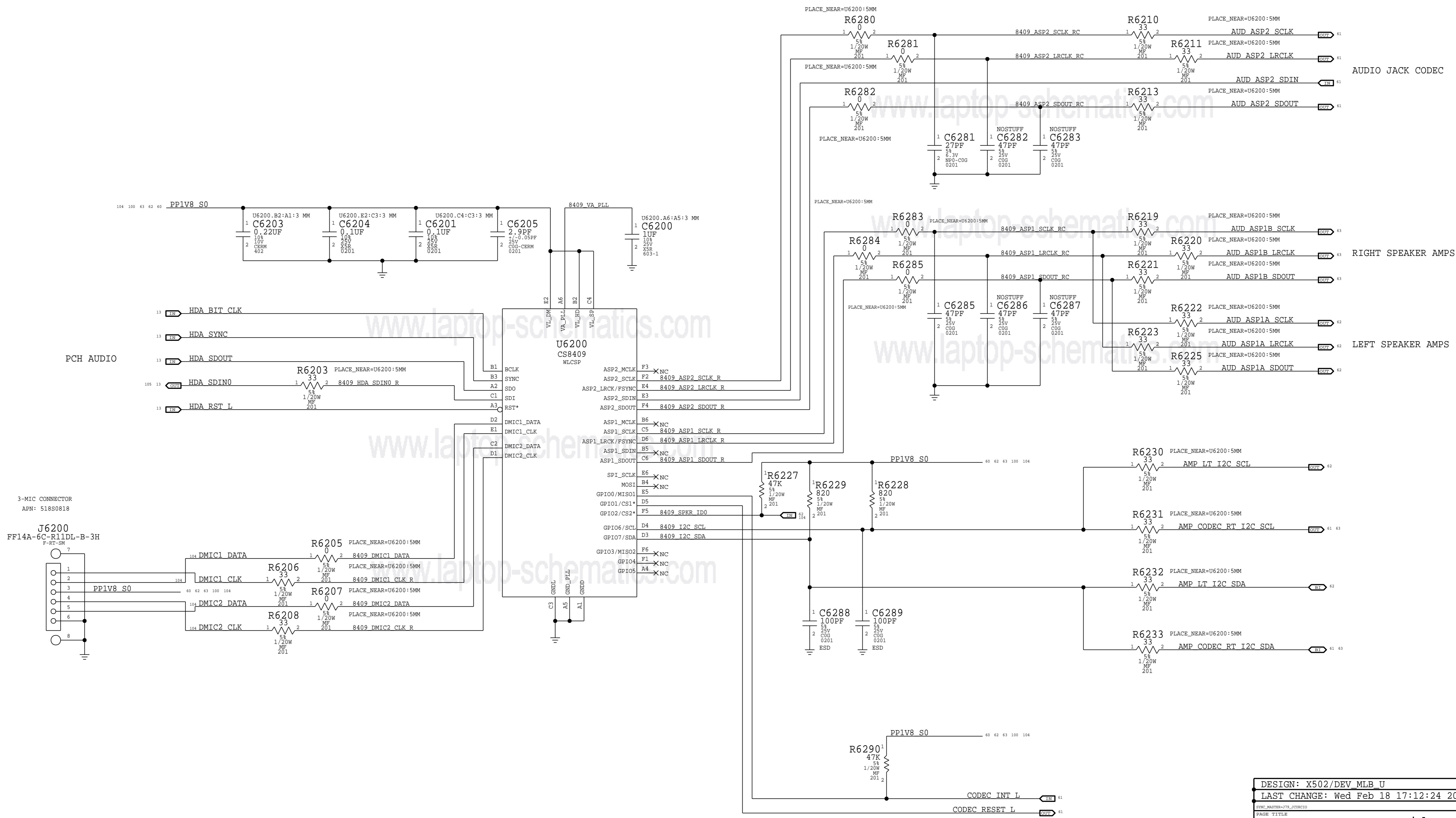
C

B

B

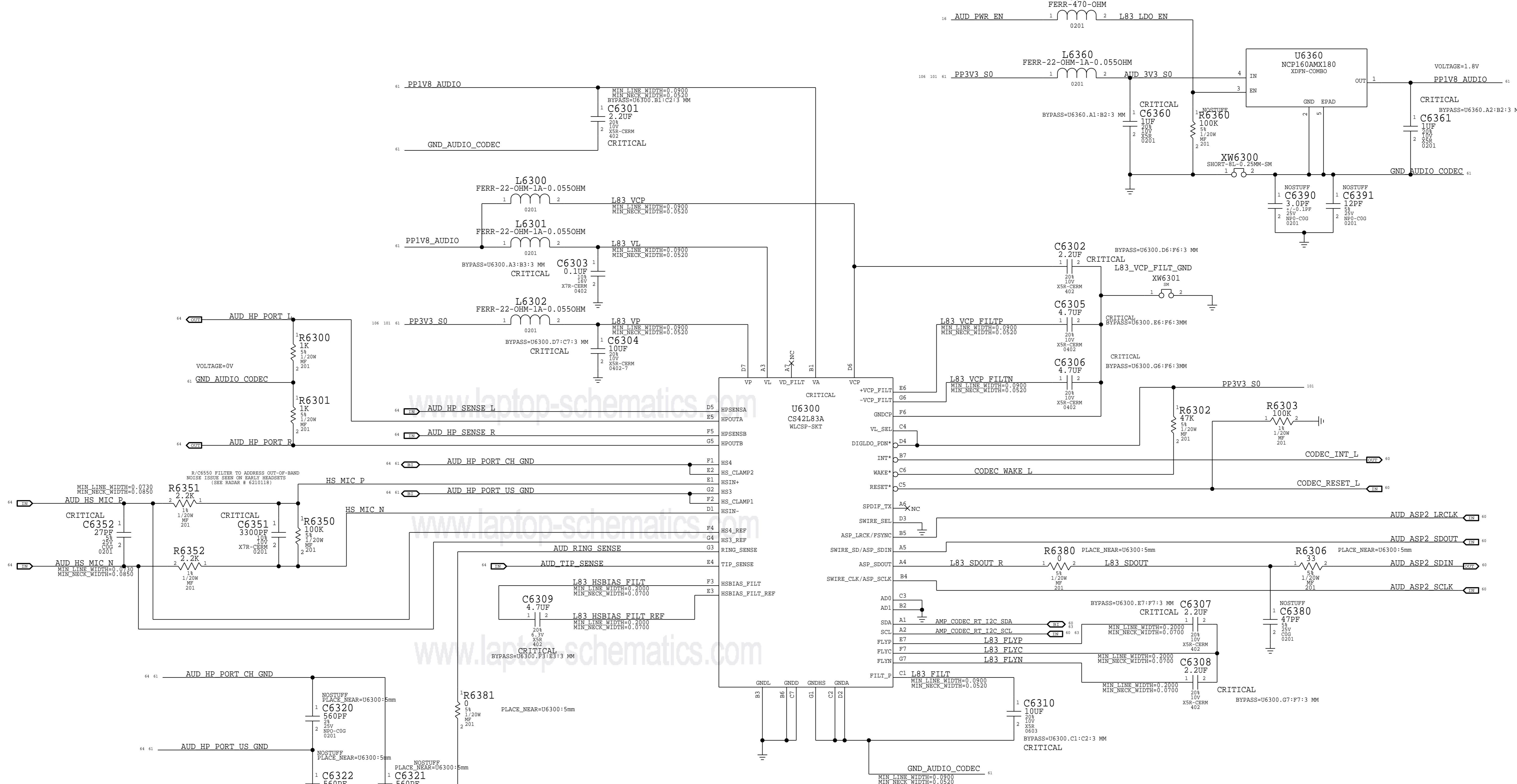
A

A



| | |
|---|-----------------------------|
| DESIGN: X502/DEV_MLB_U | |
| LAST CHANGE: Wed Feb 18 17:12:24 2015 | |
| PAGE TITLE | |
| HDA Bridge | |
| | DRAWING NUMBER 051-00777 |
| | REVISION 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | |
| BRANCH dvt-fab09-0 | STRT D |
| PAGE 62 OF 145 | SHEET 60 OF 119 |

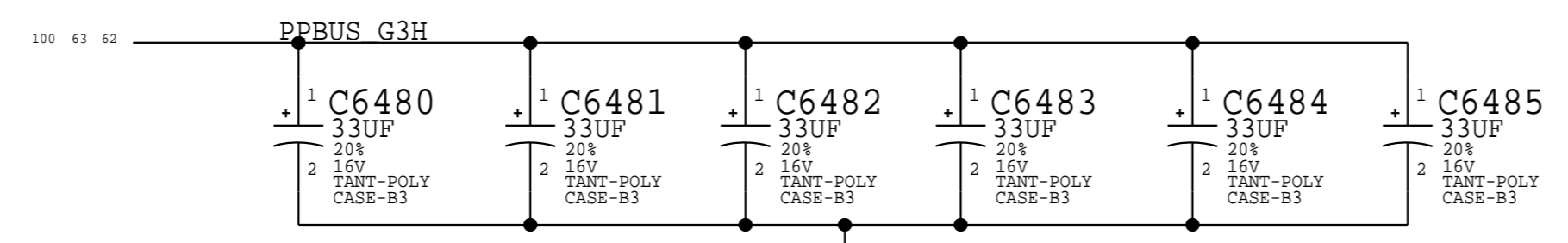
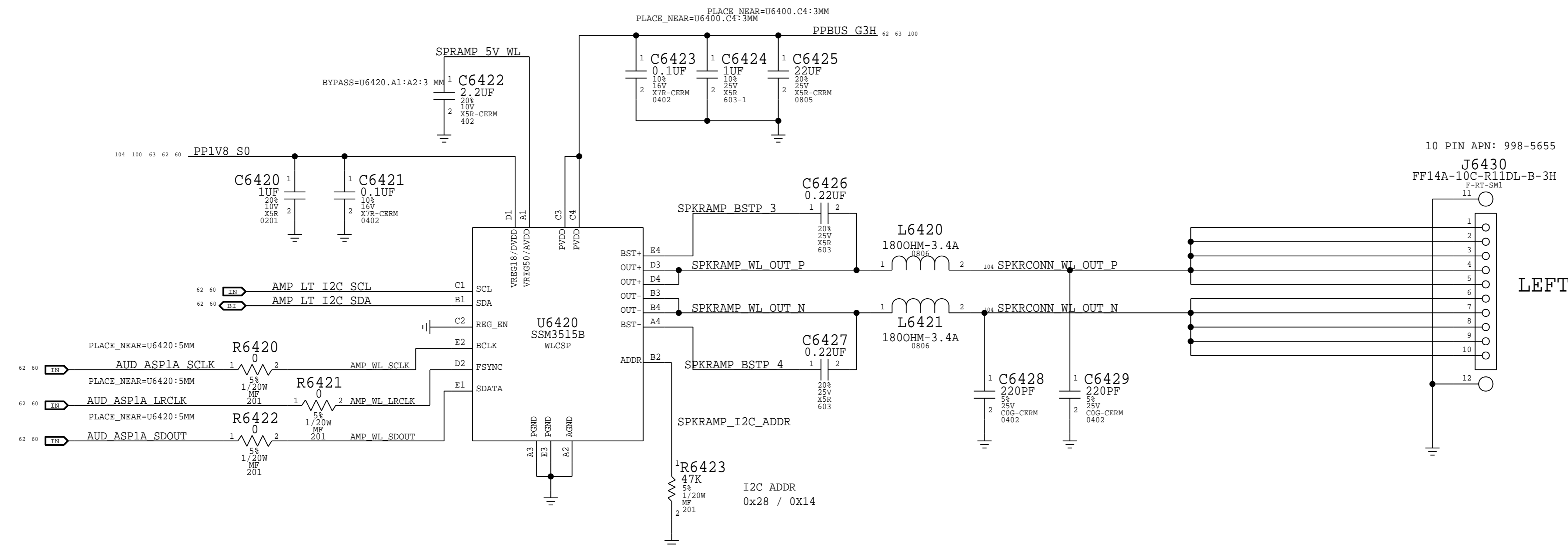
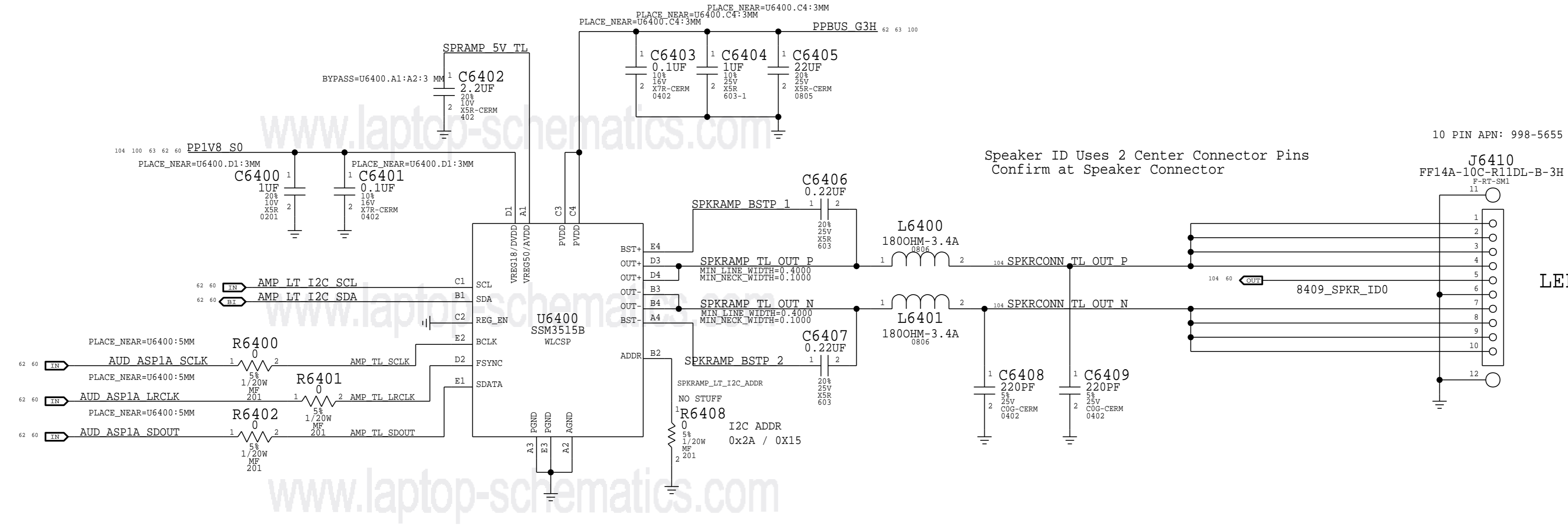
| AUDIO JACK CODEC I2C ADDRESS | | |
|------------------------------|------|----------|
| AD1 | AD0 | ADDRESS |
| GND | GND | 0x90 --- |
| GND | 1.8V | 0x92 |
| 1.8V | GND | 0x94 |
| 1.8V | 1.8V | 0x96 |



| | | | |
|---|--|---------------------------------------|-------------|
| DESIGN: X502/DEV_MLB_U | | LAST CHANGE: Wed Feb 18 17:31:01 2015 | |
| PAGE TITLE | | | |
| AUDIO JACK CODEC | | | |
| | | DRAWING NUMBER | 51-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 63 OF 145 |
| | | SHEET | 61 OF 119 |

BOM_COST_GROUP=AUDIO

2X MONO SPEAKER AMPLIFIERS
APN: 35394074
GAIN = TBD



| | | |
|---|----------------|-------------|
| DESIGN: X502/DEV_MLB_U | | |
| LAST CHANGE: Wed Feb 18 17:12:24 2015 | | |
| PAGE TITLE | | |
| Left Speaker Amps & Conn | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I11 NOT TO REPRODUCE OR COPY IT I12 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I14 ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 64 OF 145 |
| | SHEET | 62 OF 119 |

2X MONO SPEAKER AMPLIFIERS
APN: 35384073
GAIN = TBD

8

7

6

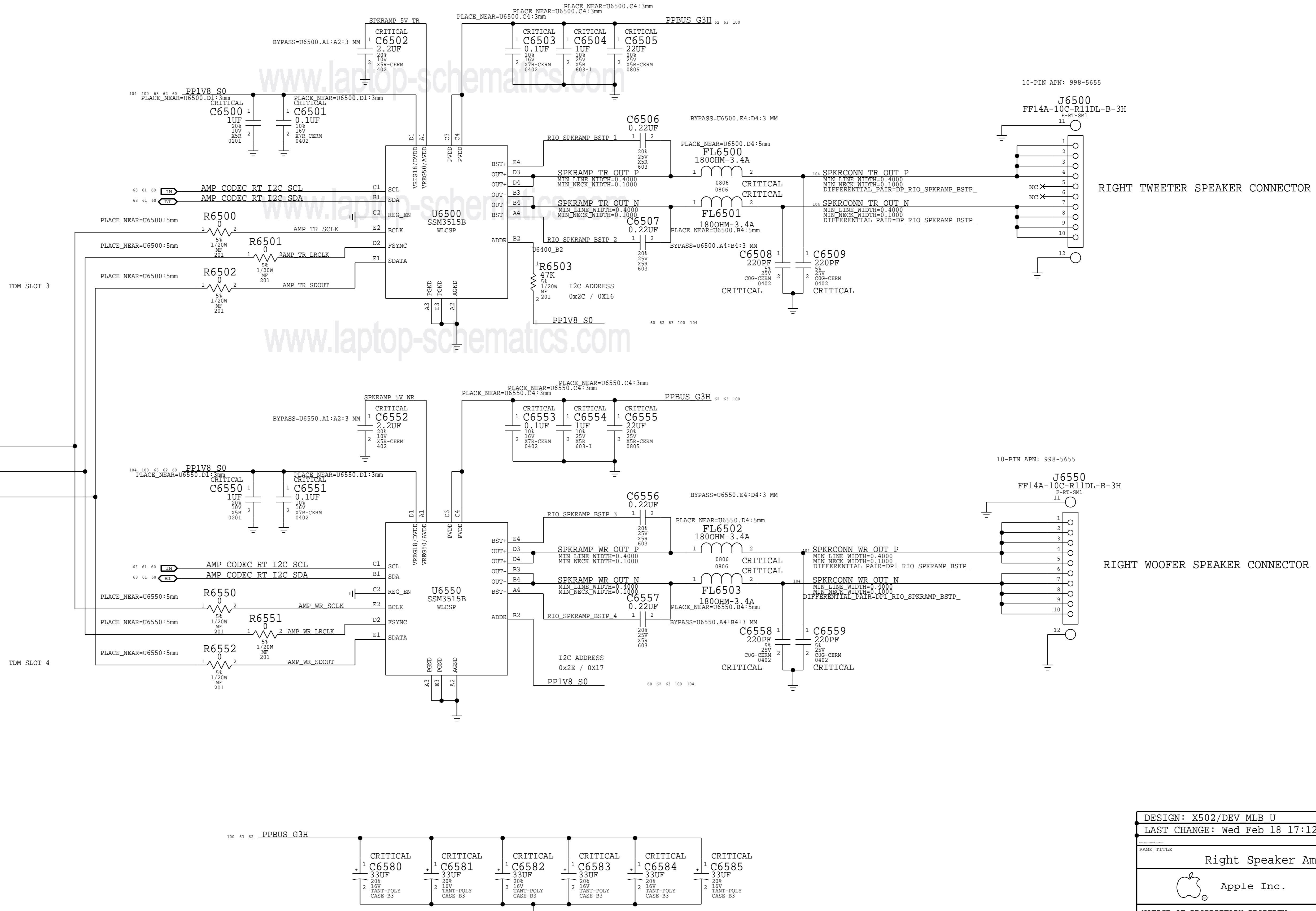
5

4

3

2

1

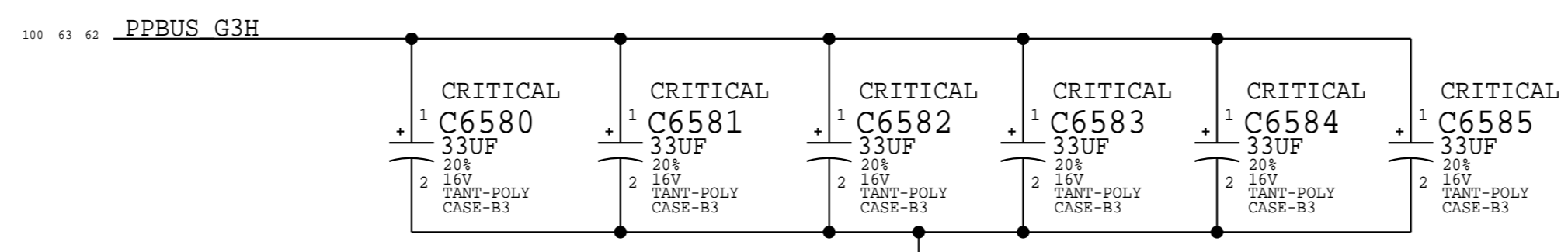


10-PIN APN: 998-5655

RIGHT TWEETER SPEAKER CONNECTOR

10-PIN APN: 998-5655

RIGHT WOOFER SPEAKER CONNECTOR



BOM_COST_GROUP=AUDIO

| | |
|---|--|
| DESIGN: X502/DEV_MLB_U | |
| LAST CHANGE: Wed Feb 18 17:12:24 2015 | |
| PAGE TITLE | |
| Right Speaker Amps & Conn | |
| Apple Inc. | DRAWING NUMBER: 051-00777 |
| | REVISION: 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | BRANCH: dvt-fab09-0 PAGE: 65 OF 145 SHEET: 63 OF 119 |

8

7

6

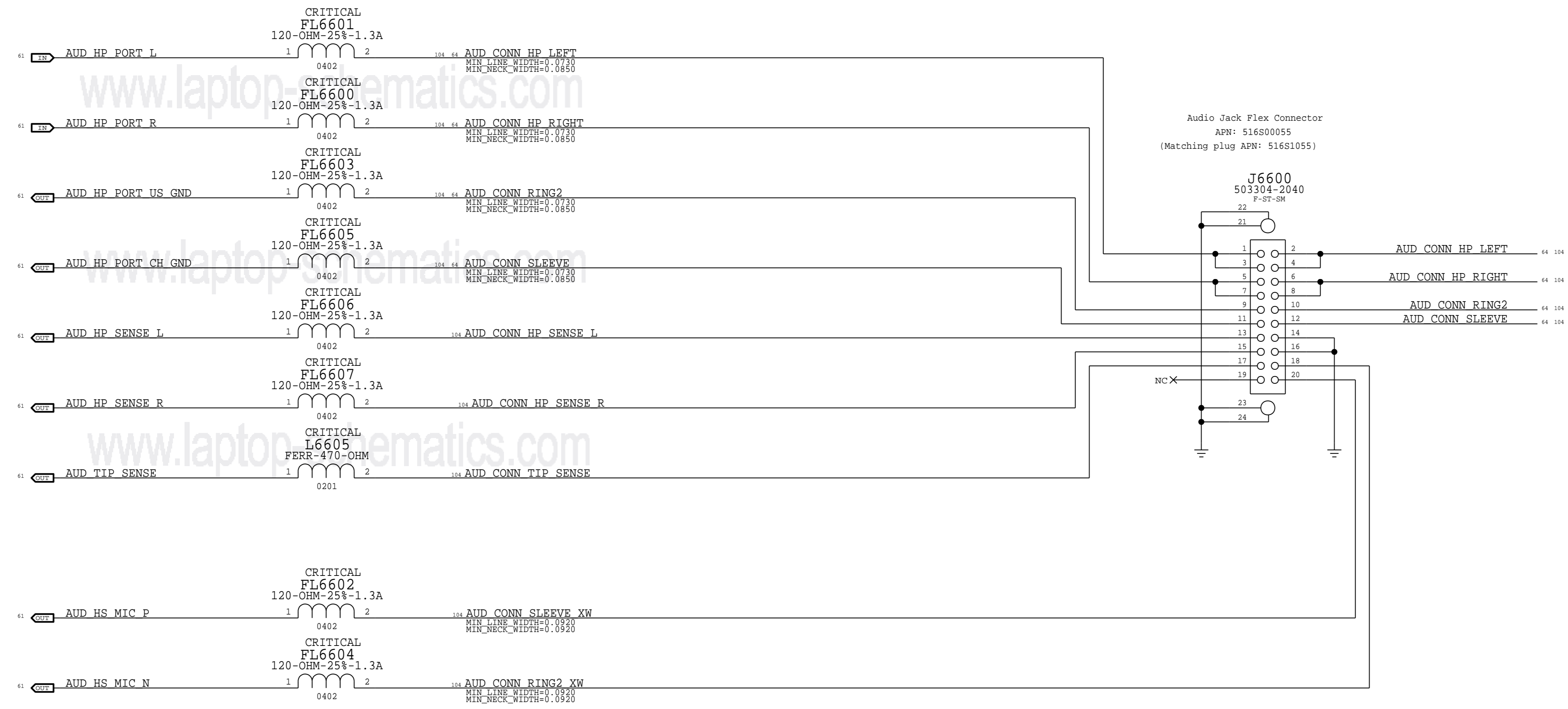
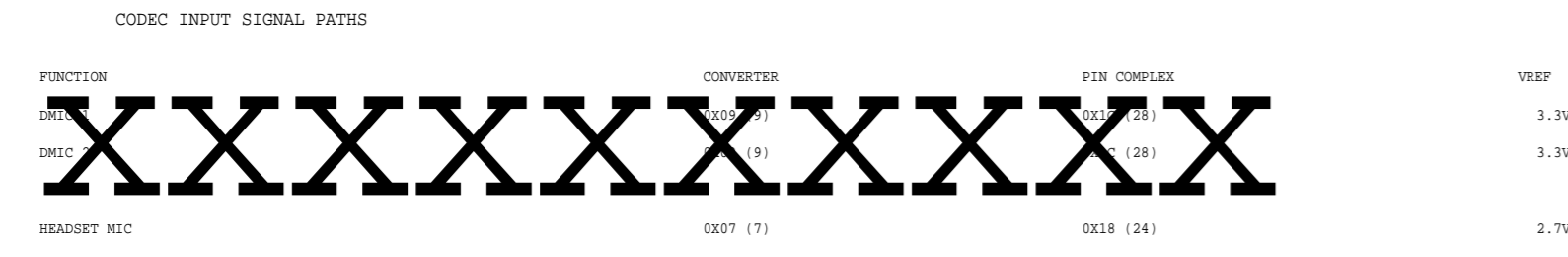
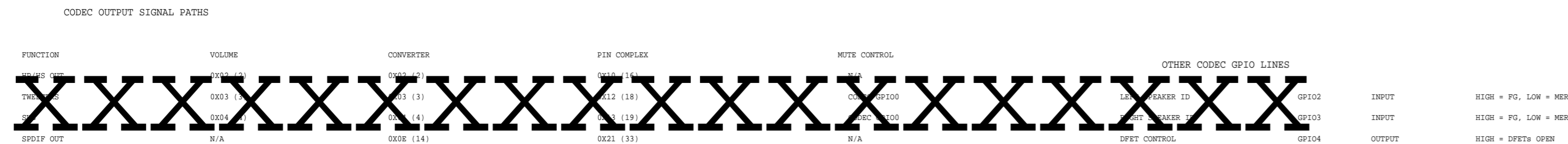
5

4

3

2

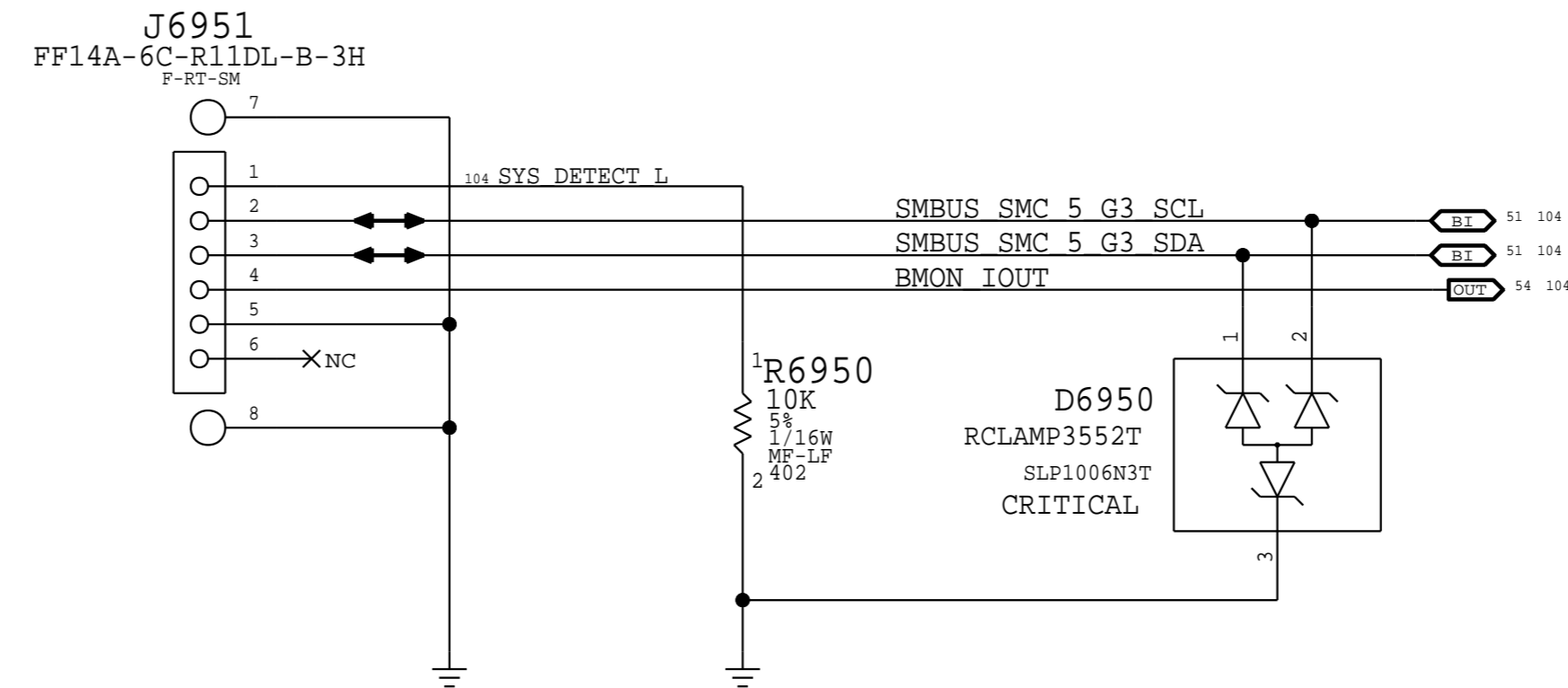
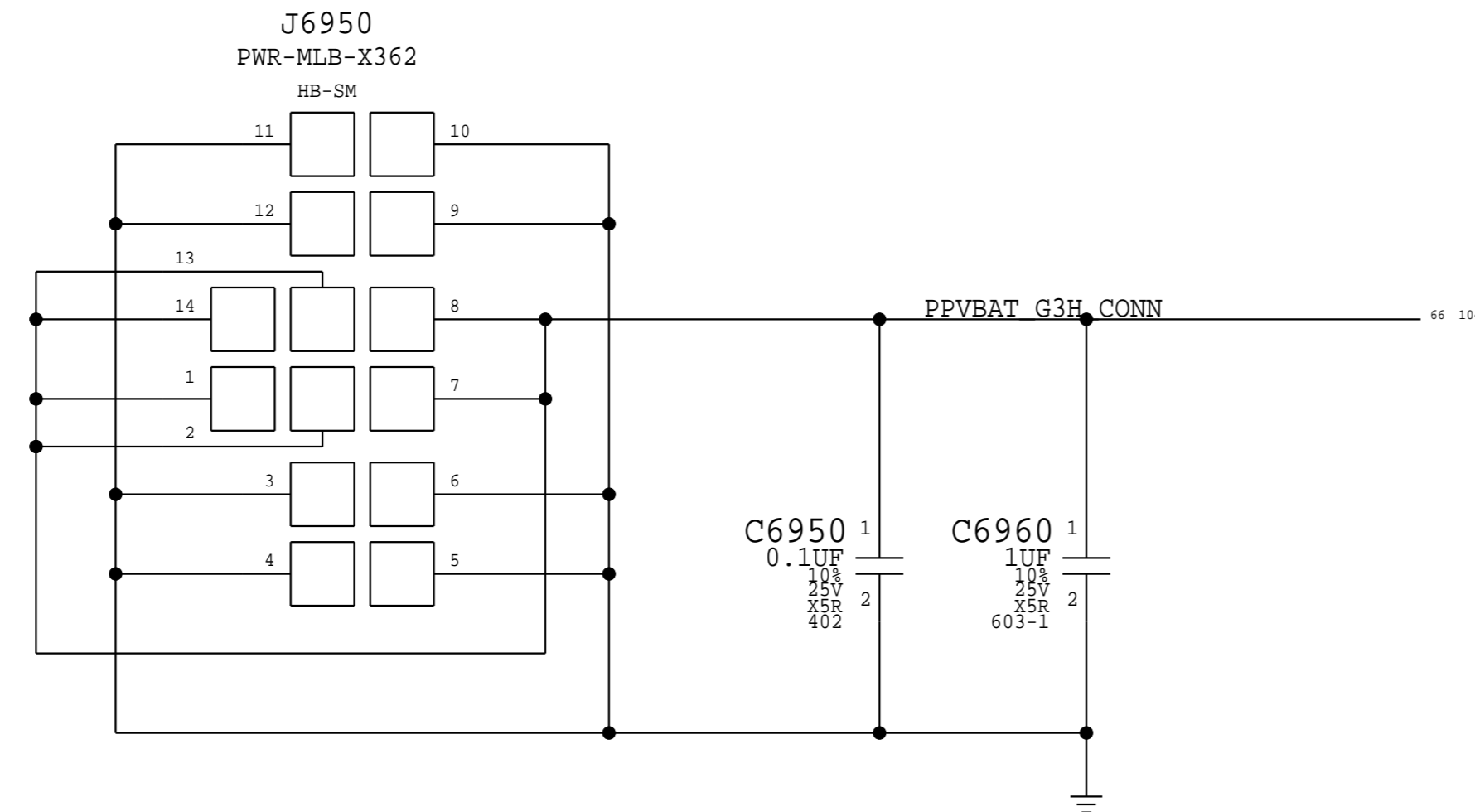
1



| | | |
|---|----------------|-------------|
| DESIGN: X502/DEV_MLB_U | | |
| LAST CHANGE: Wed Feb 18 17:12:24 2015 | | |
| PAGE TITLE | | |
| AUDIO JACK CONNECTOR | | |
| | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 66 OF 145 |
| | SHEET | 64 OF 119 |

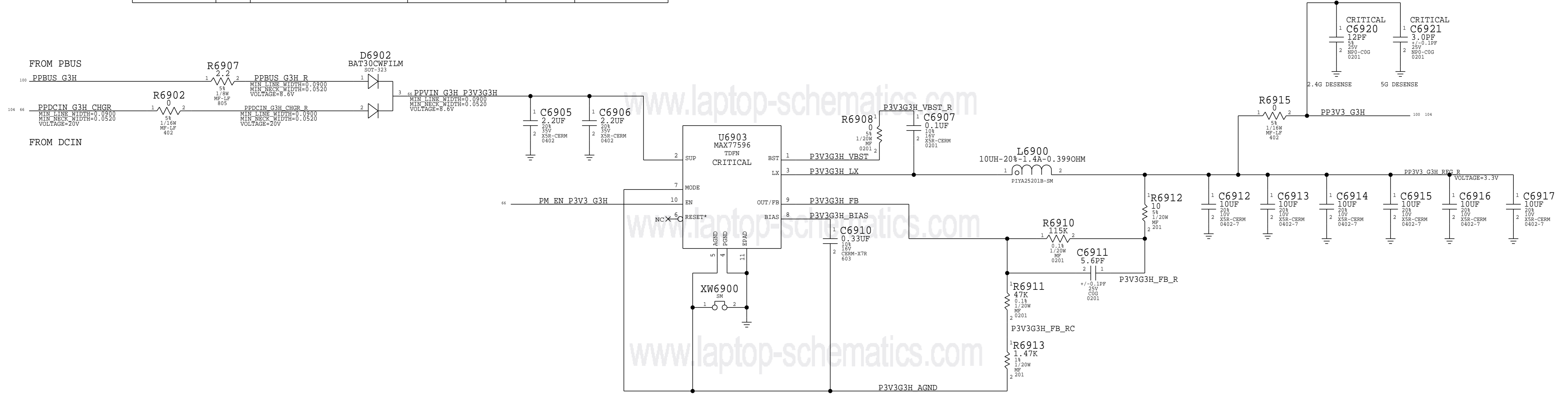
BOM_COST_GROUP=AUDIO

J79 Battery Hotbar Flex Pads

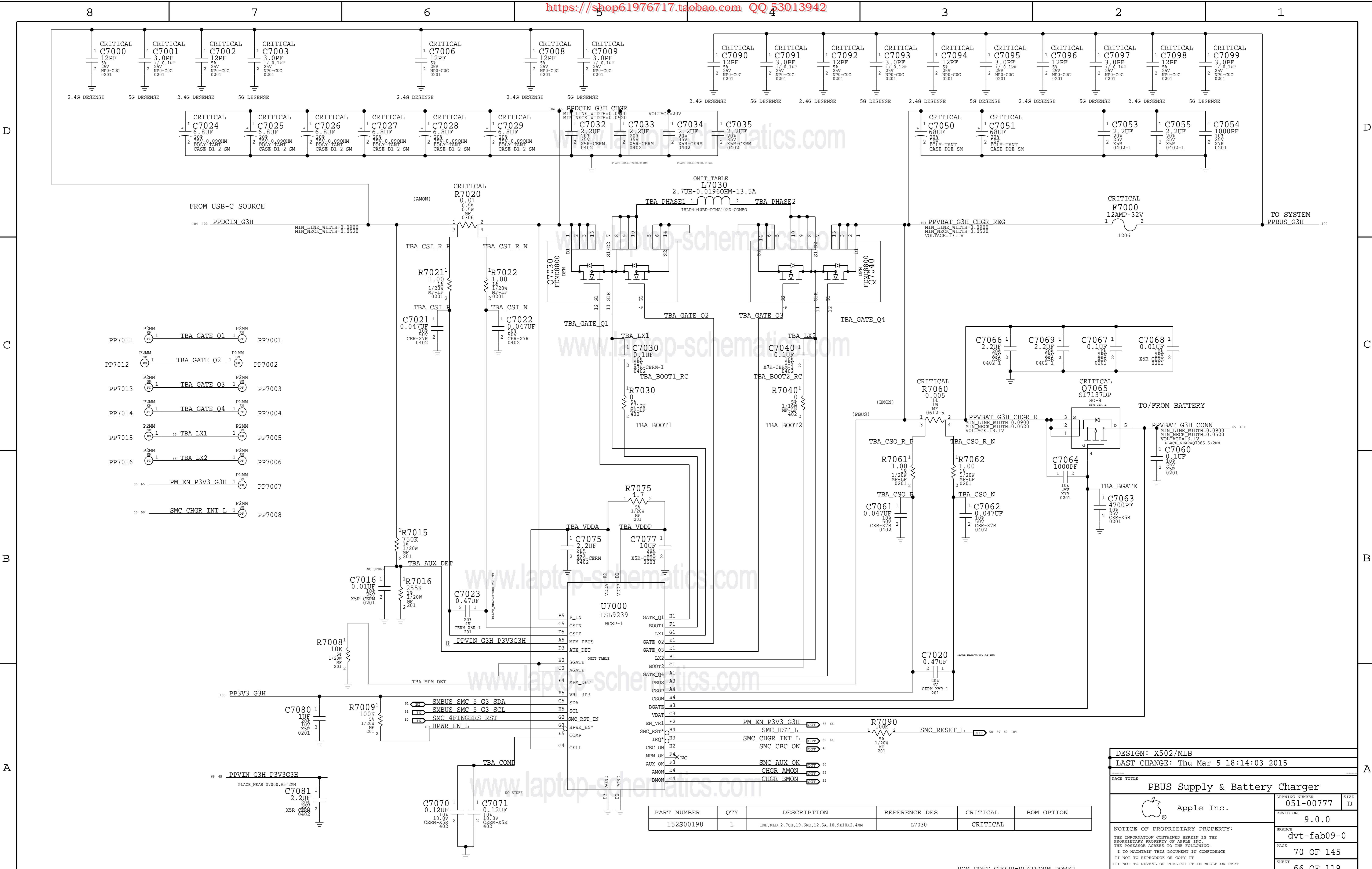


BMU POWER FLEX HOTBAR'd TO THE MLB:

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------------|---------------|----------|------------|
| 632-00566 | 1 | PCBA, FLEX, BMU PWR, X362 | J6950 | CRITICAL | |



| | | |
|--|----------------|-------------|
| PAGE TITLE | | |
| DC-In & Battery Connectors | | |
| | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 69 OF 145 |
| | SHEET | 65 OF 119 |



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--|---------------|----------|------------|
| 152S00198 | 1 | IND.MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM | L7030 | CRITICAL | |

DESIGN: X502/MLB
 LAST CHANGE: Thu Mar 5 18:14:03 2015

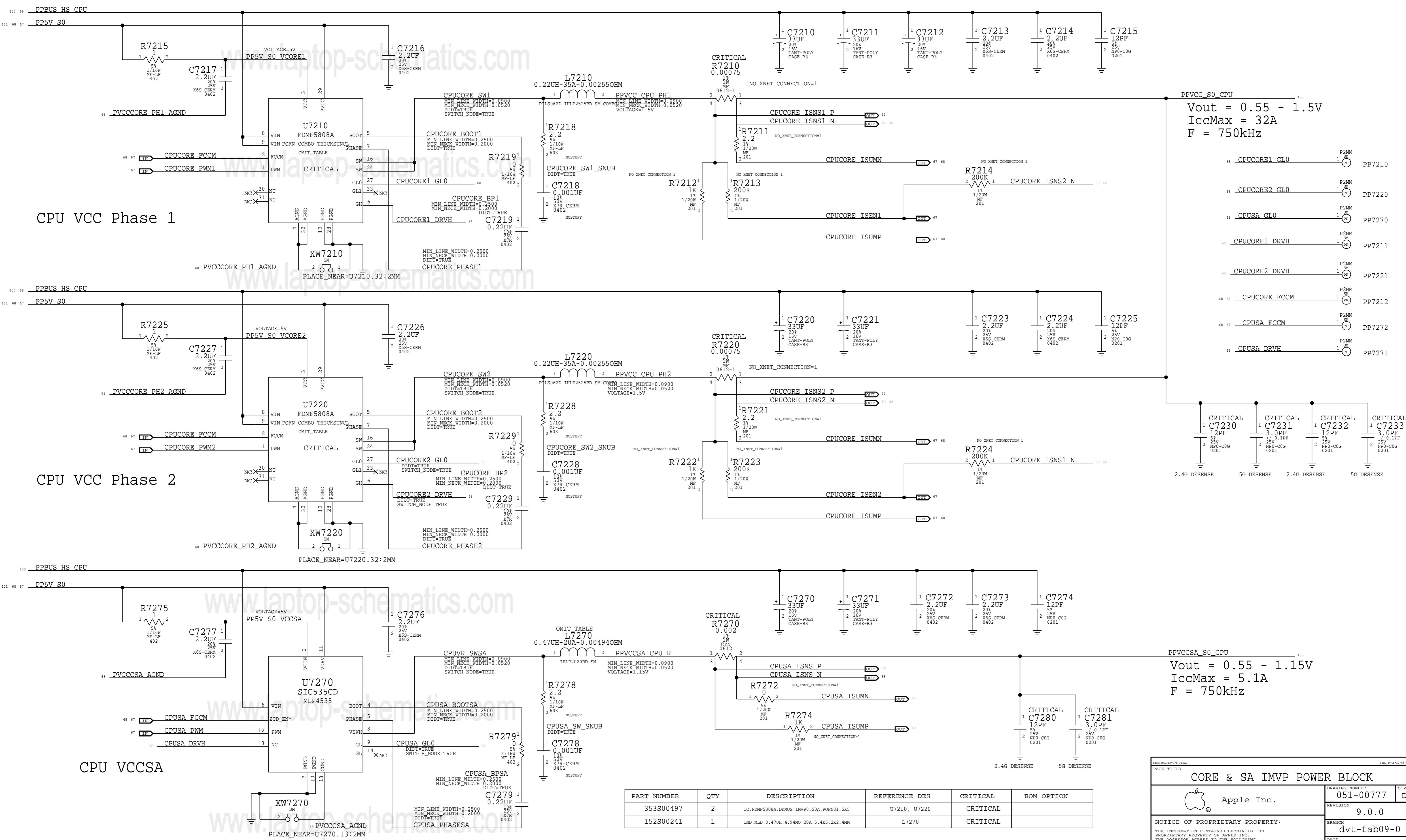
PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

| | | | |
|----------------|-------------|-----|---|
| DRAWING NUMBER | 051-00777 | STR | D |
| REVISION | 9.0.0 | | |
| BRANCH | dvt-fab09-0 | | |
| PAGE | 70 OF 145 | | |
| SHEET | 66 OF 119 | | |

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 11V ALL RIGHTS RESERVED

BOM_COST_GROUP=PLATFORM POWER



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---|---------------|----------|------------|
| 353S00497 | 2 | IC,FDMF5808A,DRMOS,IMVP8.50A,PQFN31.5X5 | U7210,U7220 | CRITICAL | |
| 152S00241 | 1 | IND,MLD,0.47UH,4.94MO,20A,5.4X5.2X2.4MM | L7270 | CRITICAL | |

Apple Inc. CORE & SA IMVP POWER BLOCK

051-00777
 9.0.0
 dvt-fab09-0
 72 OF 145
 68 OF 119

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 11V ALL RIGHTS RESERVED

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6


5

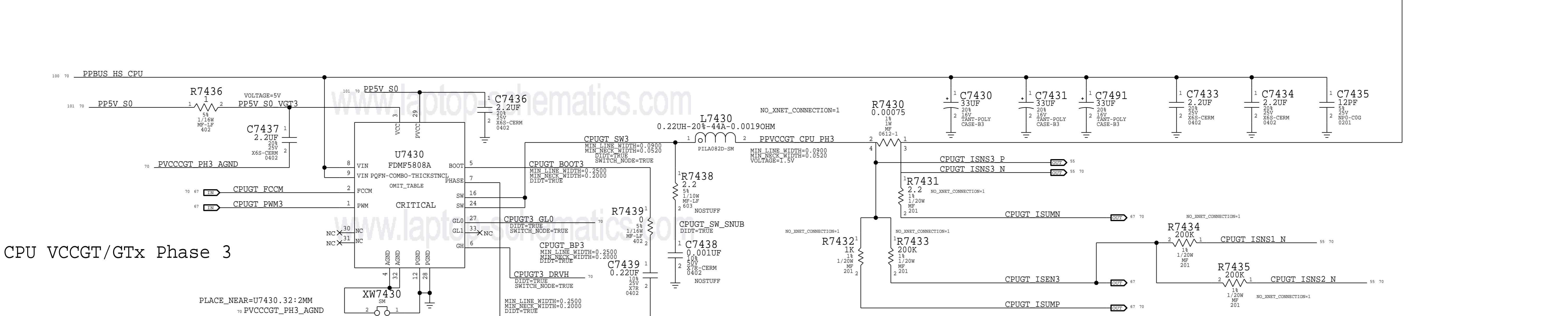
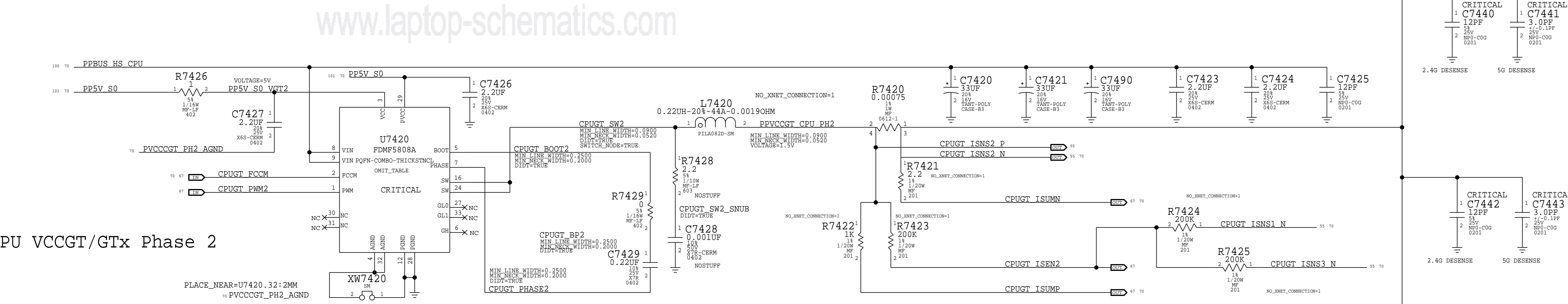
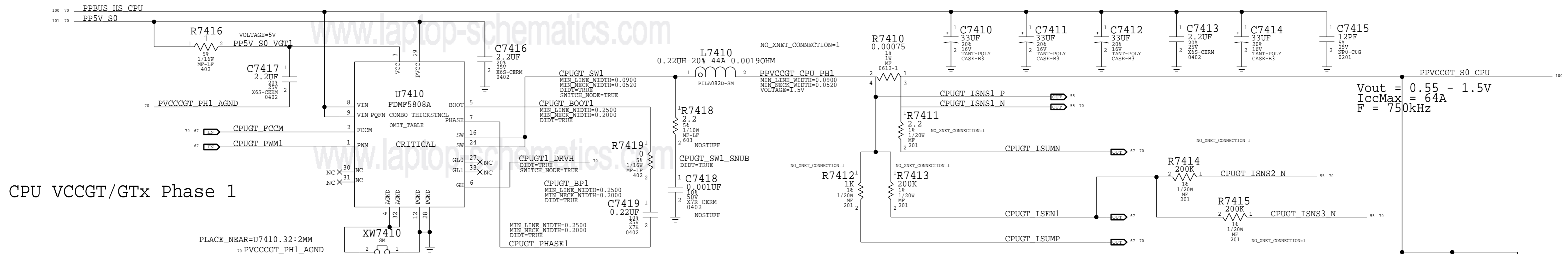
4

3

2

1

| | | | |
|---|----------------|----------------------|------|
| SYNC_MASTER=J79_SILUCHEN | | SYNC_DATE=04/02/2015 | |
| PAGE TITLE | | | |
| Empty | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 73 OF 145 | |
| | SHEET | 69 OF 119 | |



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--|---------------------|----------|------------|
| 353500497 | 3 | IC,FDMF5808A,DRMOS,1.1MPH,50A,PQFN31,5X5 | U7410, U7420, U7430 | CRITICAL | |

GT & GTX IMVP POWER BLOCK

Apple Inc.

DRWING NUMBER: 051-00777
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 74 OF 145
SHEET: 70 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1111 ALL RIGHTS RESERVED

8

7

6

5

4

3

2

1

D

D

C


C

B

B

A

A

| | | | |
|---|----------------|----------------------|------|
| SYNC_MASTER=J79_SILUCHEN | | SYNC_DATE=03/27/2015 | |
| PAGE TITLE | | | |
| Empty | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 75 OF 145 | |
| | SHEET | 71 OF 119 | |

8

7

6

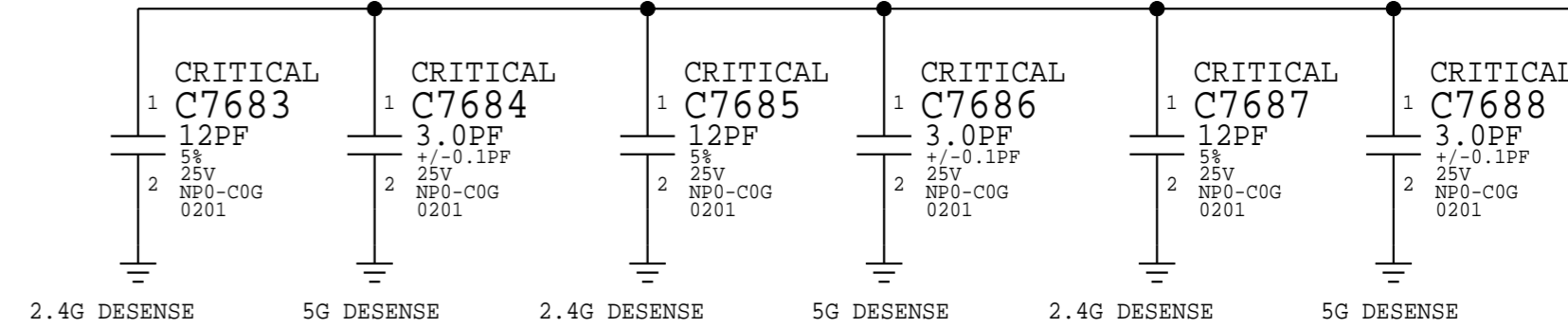
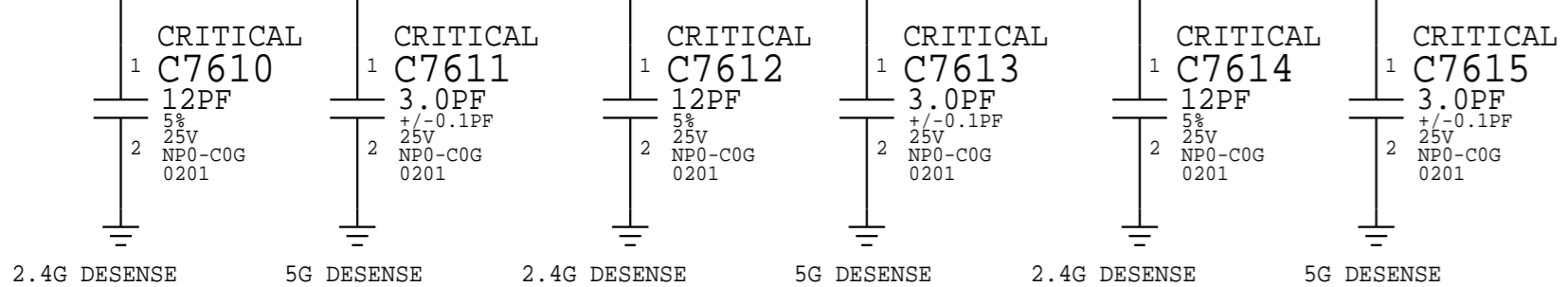
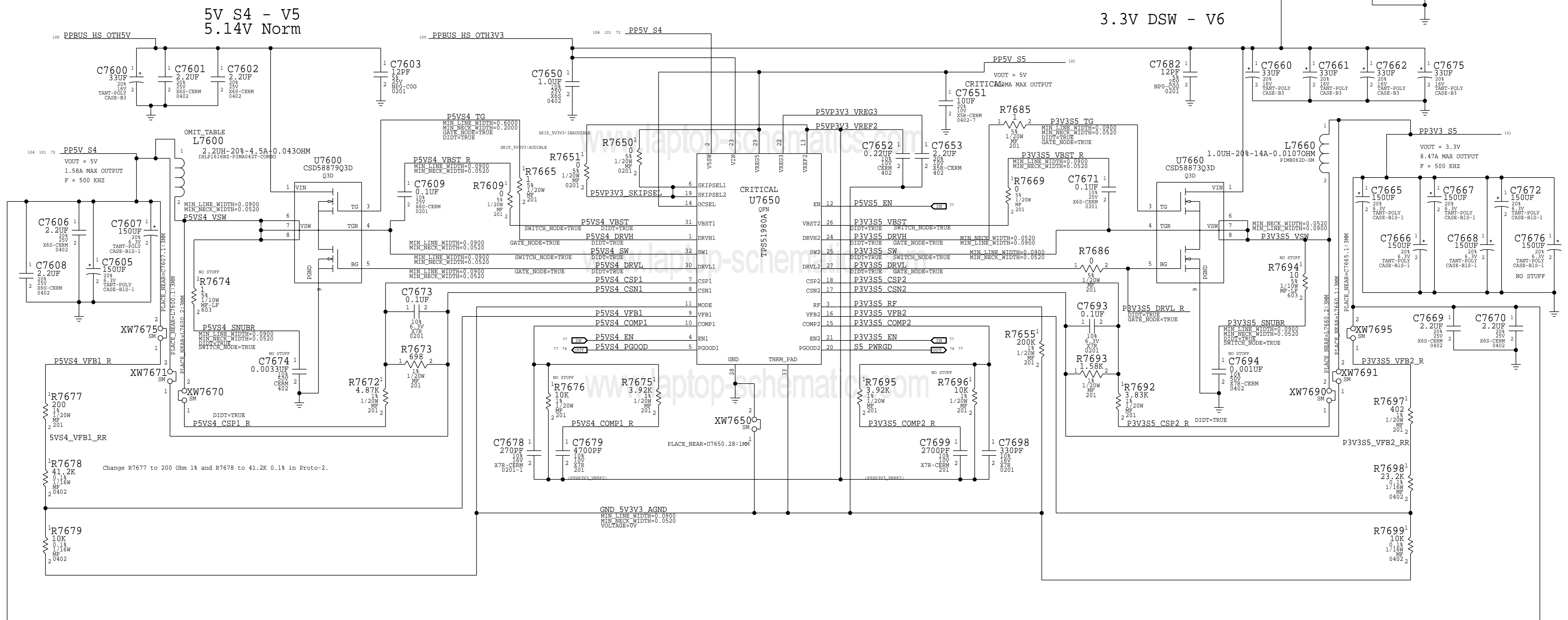
5

4

3

2

1



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---|---------------|----------|------------|
| 152S00182 | 1 | IND, PWR, 2.2UH, 20%, 4.5A, 43MOHM, 4X4MM | L7600 | CRITICAL | |

PAGE TITLE: Power - 5V 3.3V Supply

Apple Inc.

BRANCHING NUMBER: 051-00777

REVISION: 9.0.0

BRANCH: dvt-fab09-0

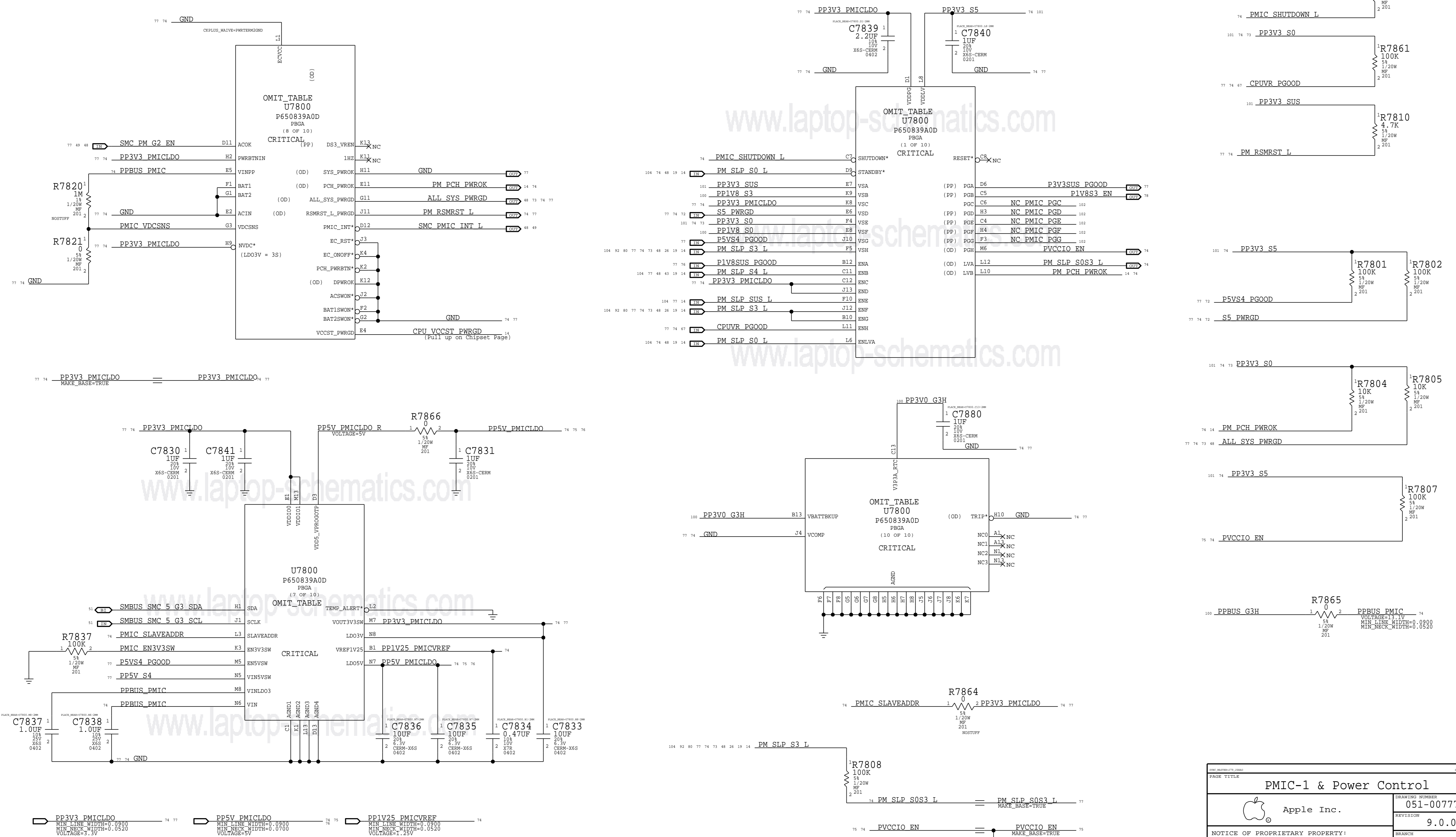
PAGE: 76 OF 145

SHEET: 72 OF 119

NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED

BOM_COST_GROUP=PLATFORM POWER

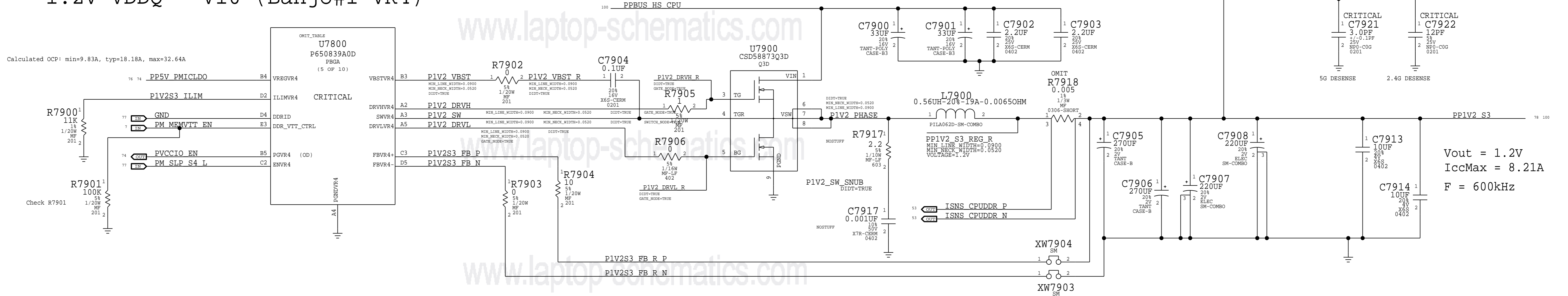
BANJO - PMIC Control



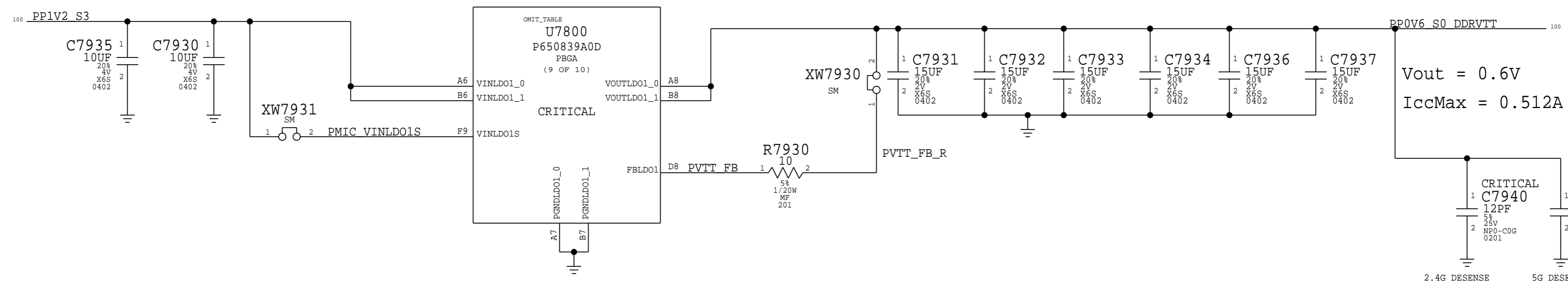
| | | |
|------------------------------------|--|------------------------------|
| DRAWING NUMBER 051-00777 | | STEP D |
| REVISION 9.0.0 | | BRANCH dvt-fab09-0 |
| PAGE 78 OF 145 | | SHEET 74 OF 119 |

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
1111 ALL RIGHTS RESERVED

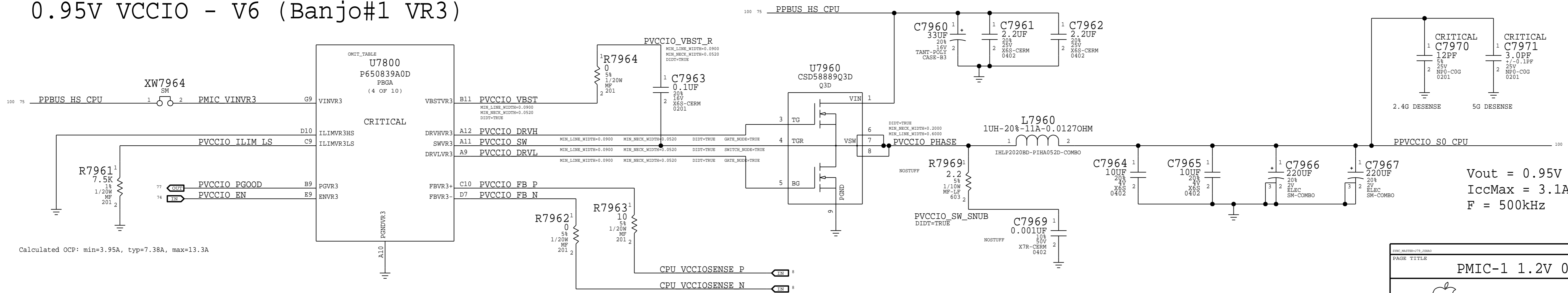
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LD01)

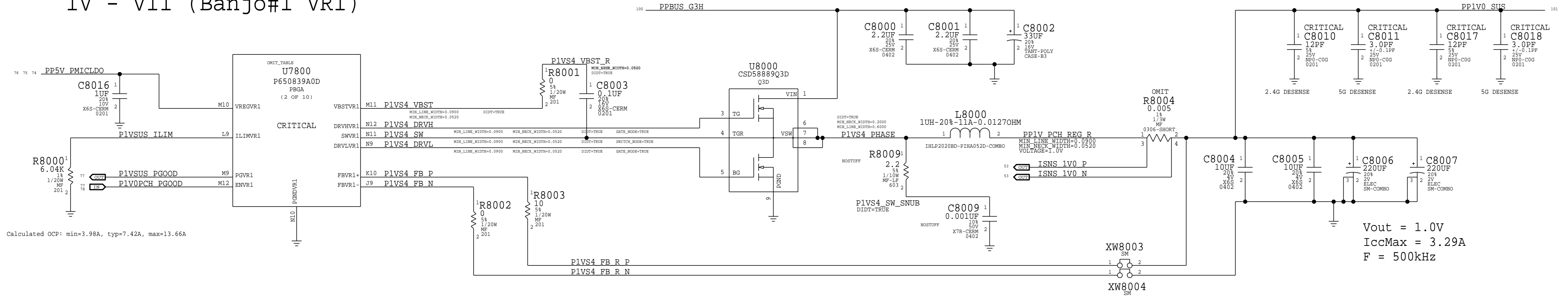


0.95V VCCIO - V6 (Banjo#1 VR3)

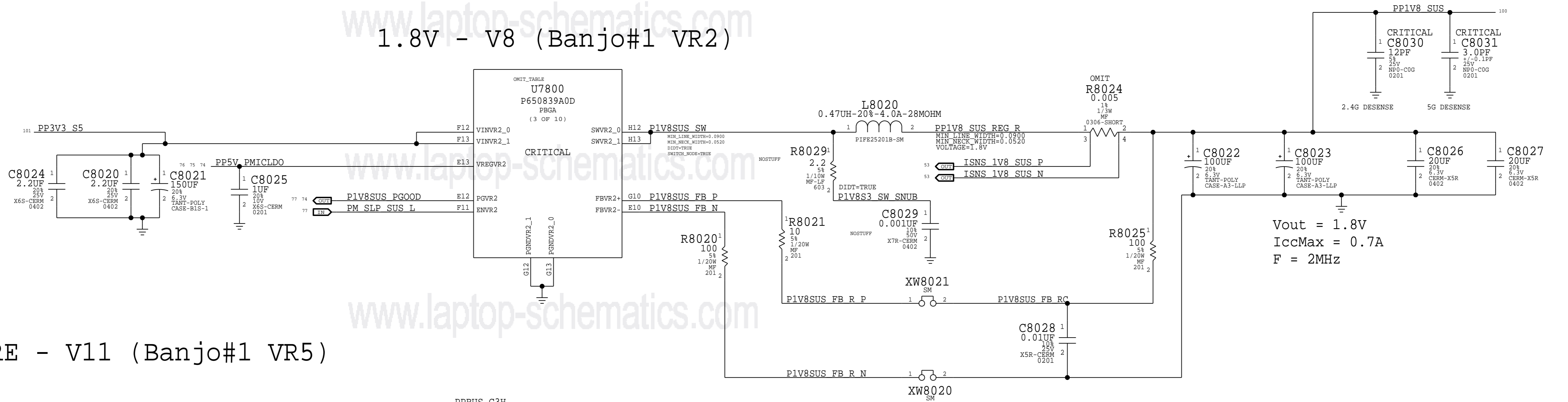


| | | | | |
|----------------|--|-------------|------|---|
| DRAWING NUMBER | | 051-00777 | STEP | D |
| REVISION | | 9.0.0 | | |
| BRANCH | | dvt-fab09-0 | | |
| PAGE | | 79 OF 145 | | |
| SHEET | | 75 OF 119 | | |

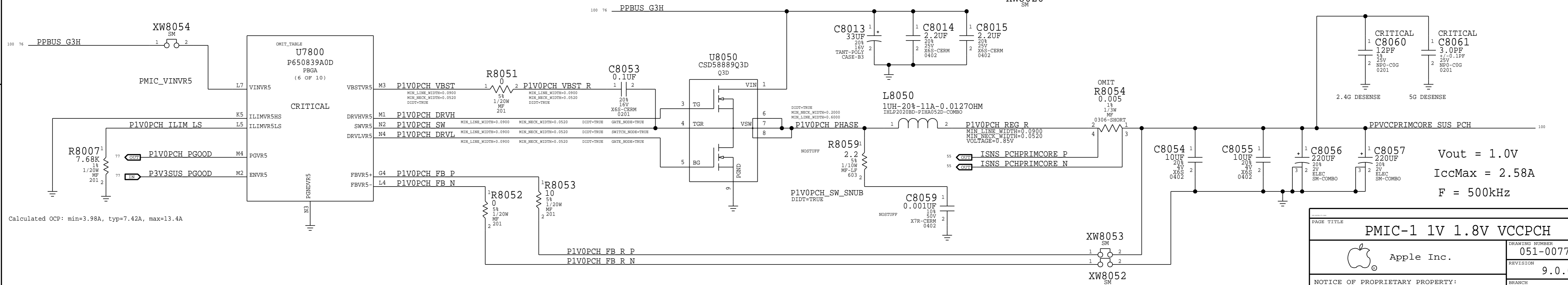
1V - V11 (Banjo#1 VR1)



1.8V - V8 (Banjo#1 VR2)

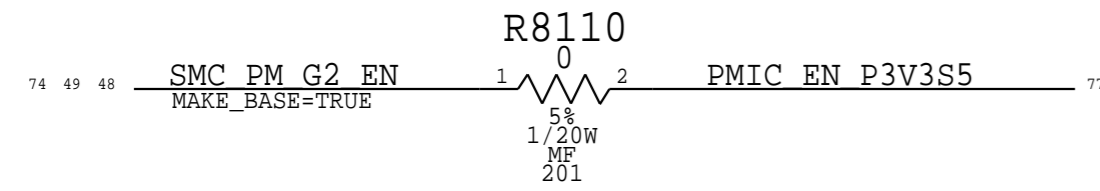


1.0V PCH CORE - V11 (Banjo#1 VR5) 0.7V LPM

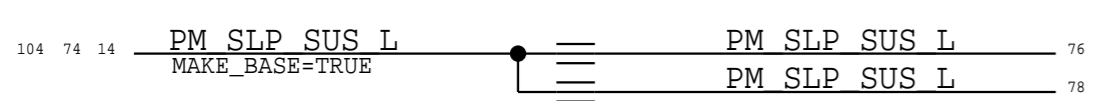


| | | | | |
|---|--|----------------|--|------|
| PAGE TITLE | | DRAWING NUMBER | | STAR |
| PMIC-1 1V 1.8V VCCPCH | | 051-00777 | | D |
| Apple Inc. | | REVISION | | |
| | | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | dvt-fab09-0 | | |
| 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | PAGE | | |
| 11 NOT TO REPRODUCE OR COPY IT | | 80 OF 145 | | |
| 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | SHEET | | |
| 112 ALL RIGHTS RESERVED | | 76 OF 119 | | |

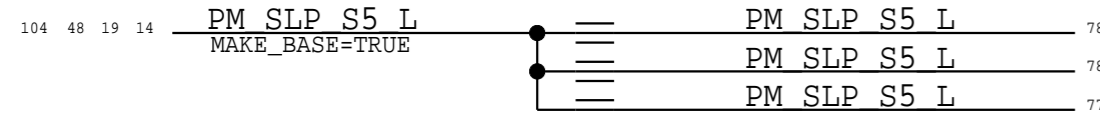
S5 Enables



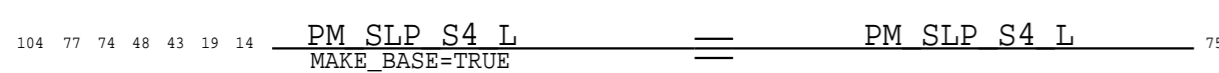
SUS Enables



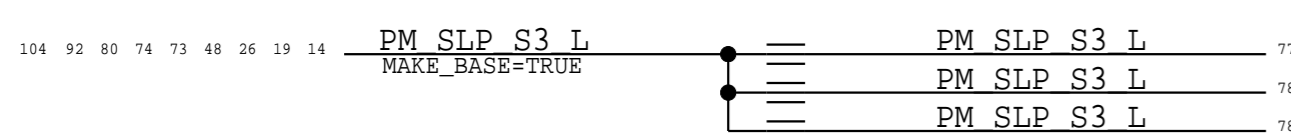
S4 Enables



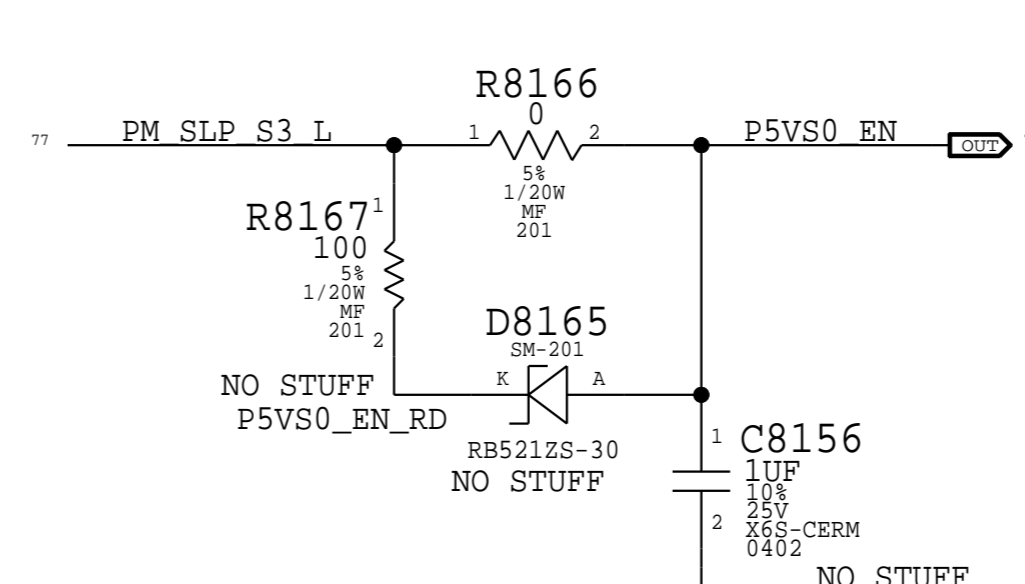
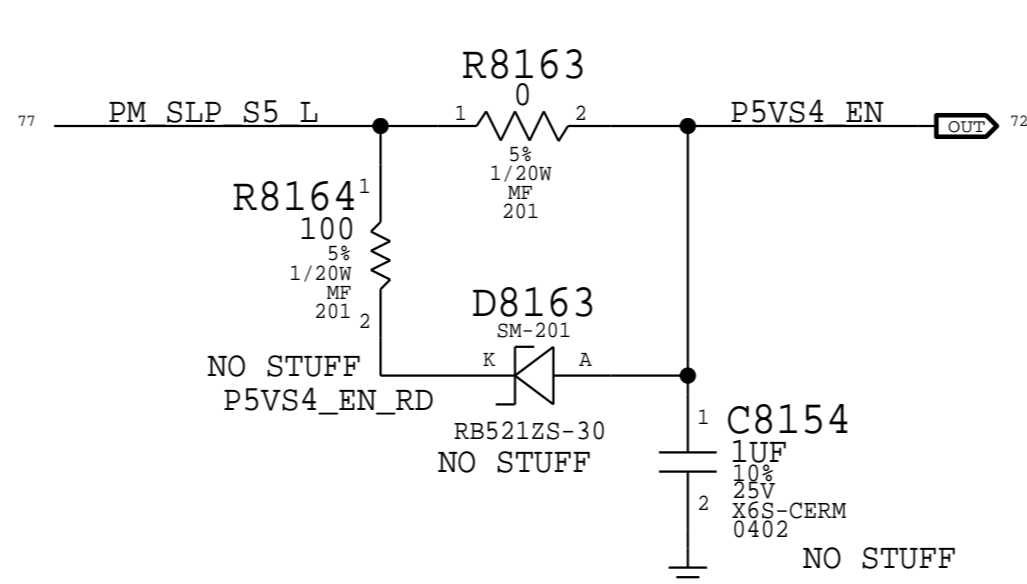
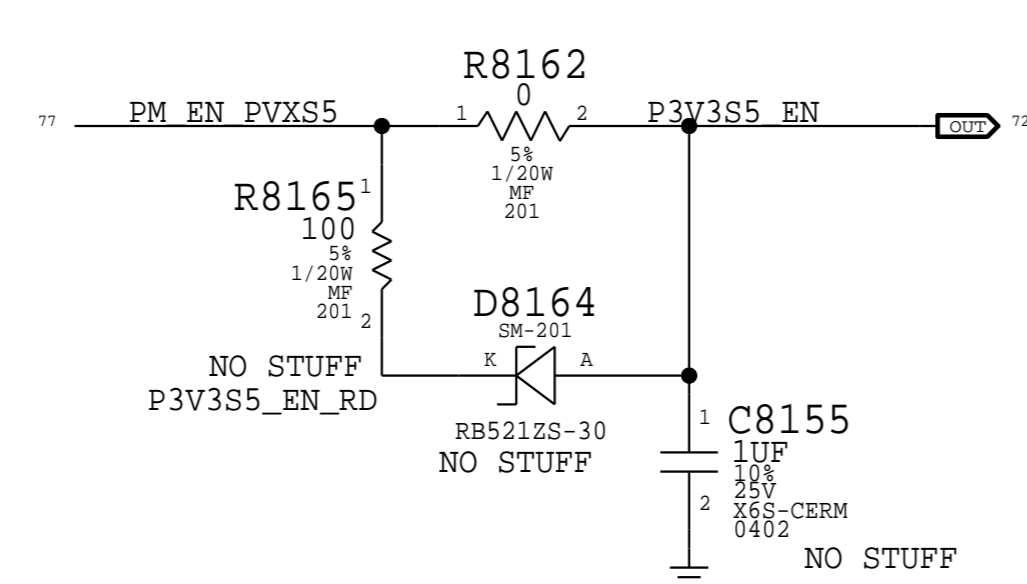
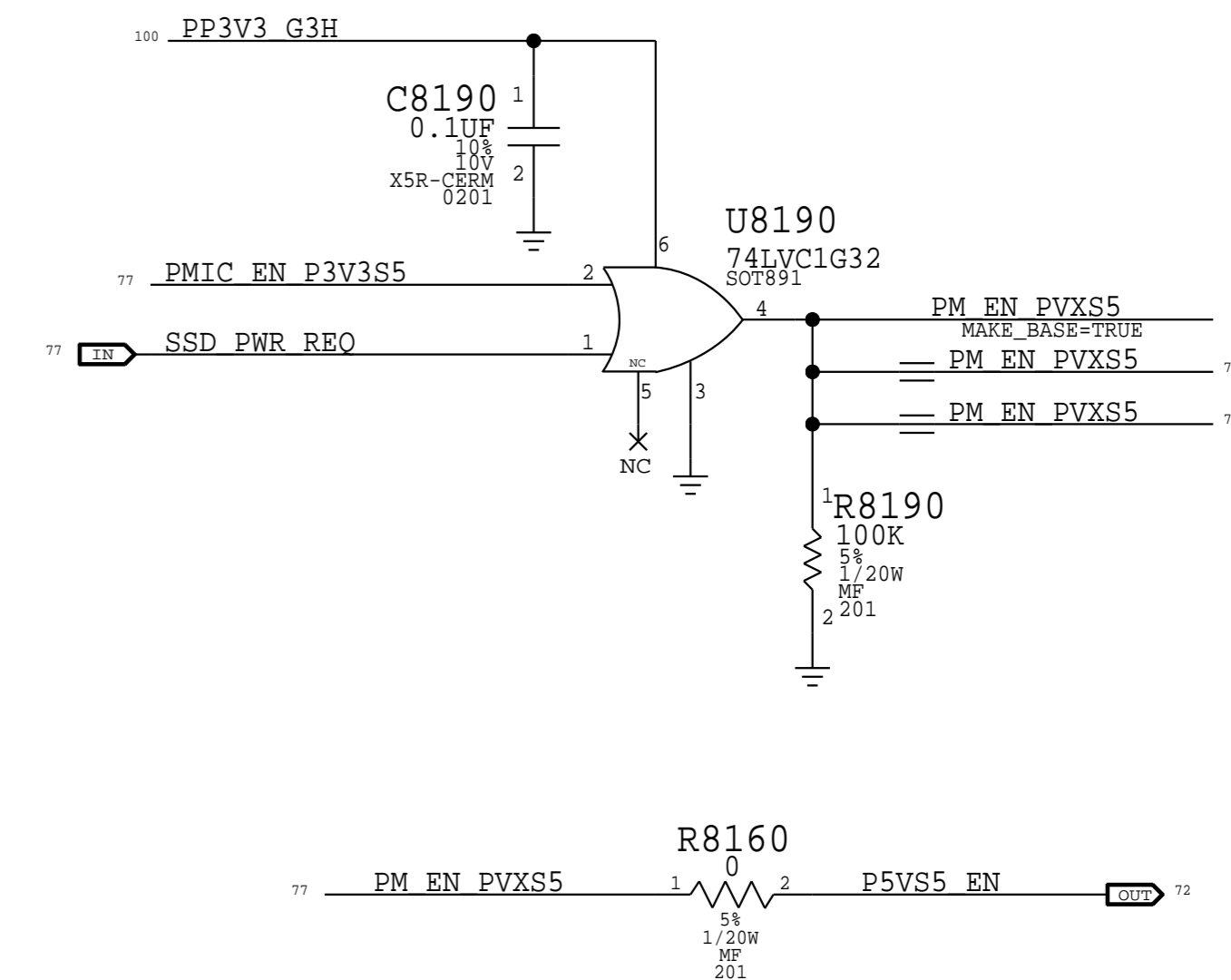
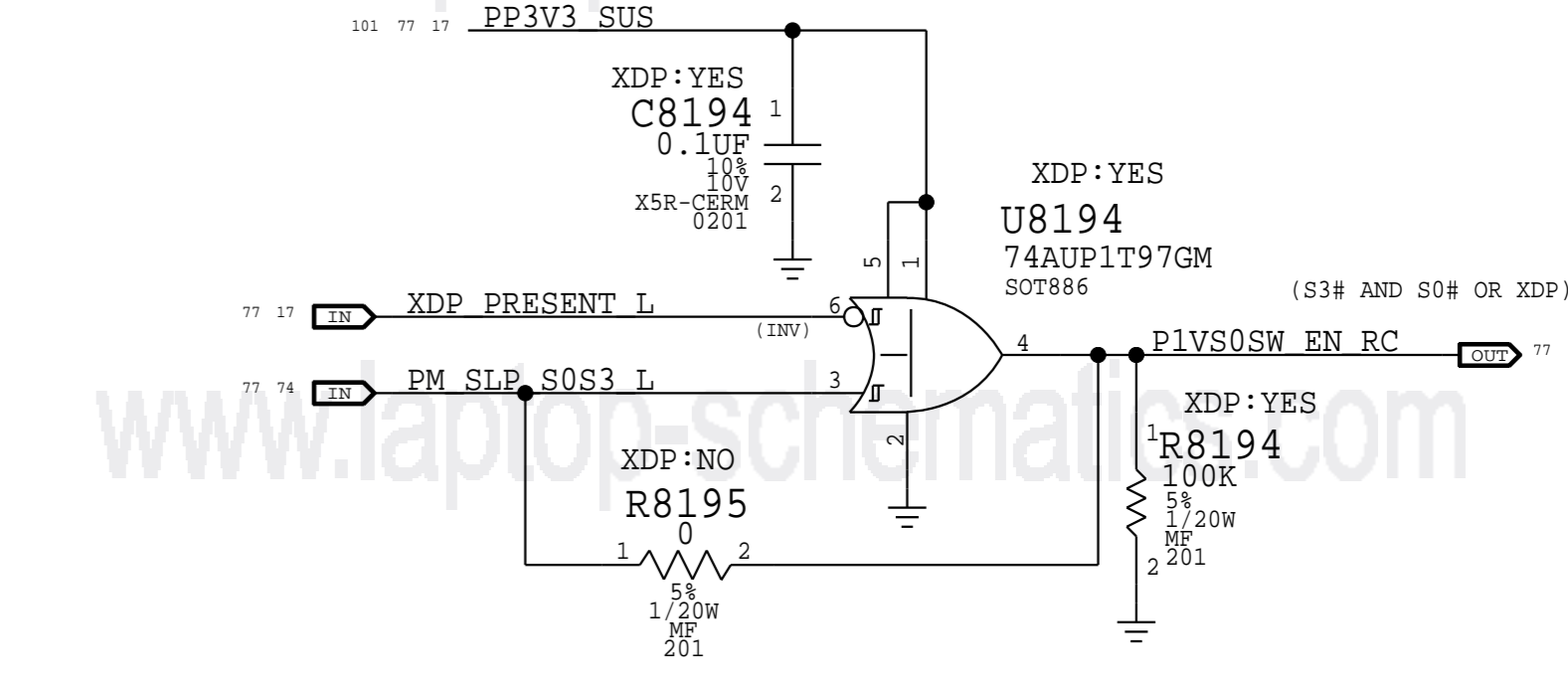
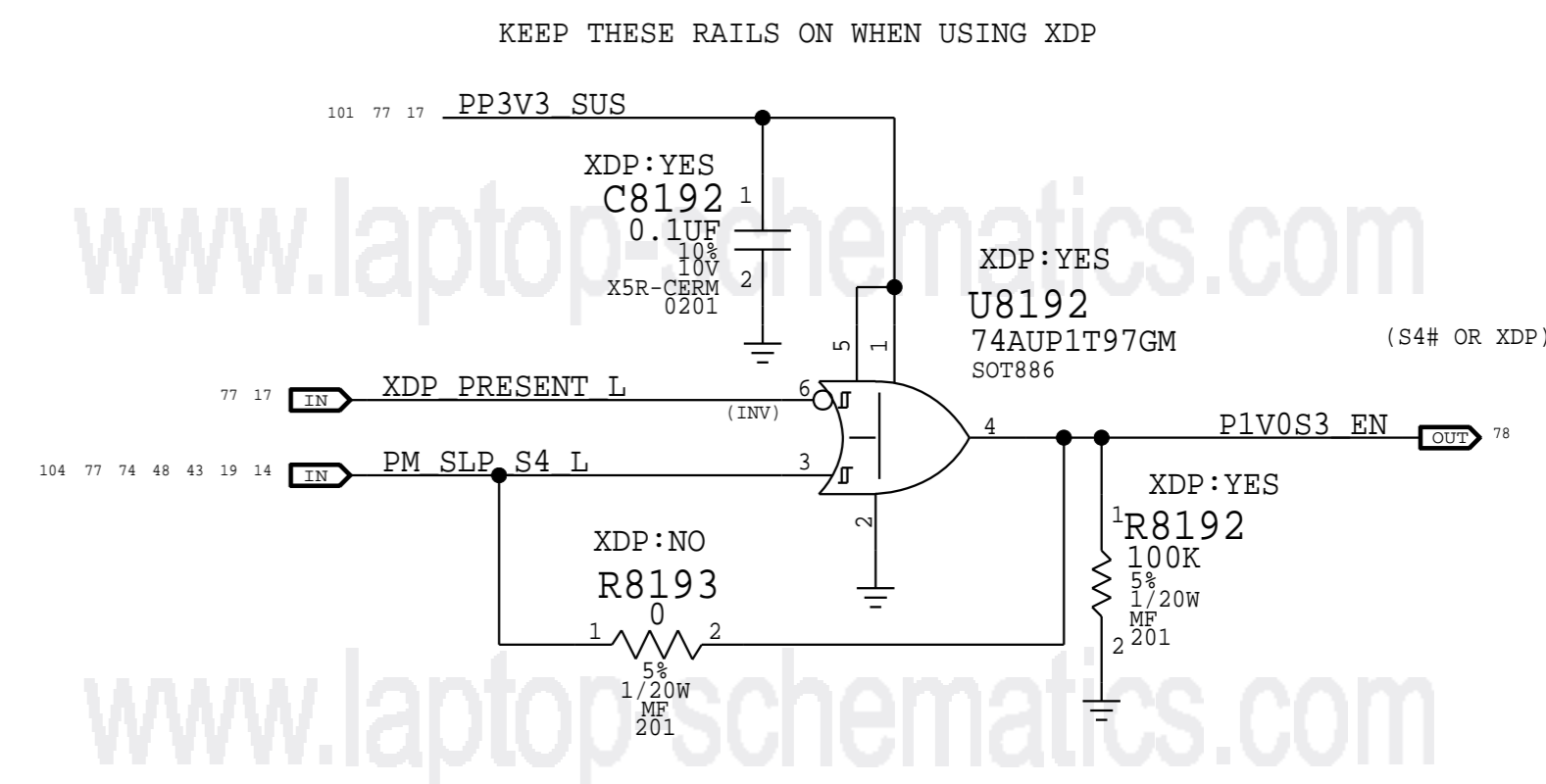
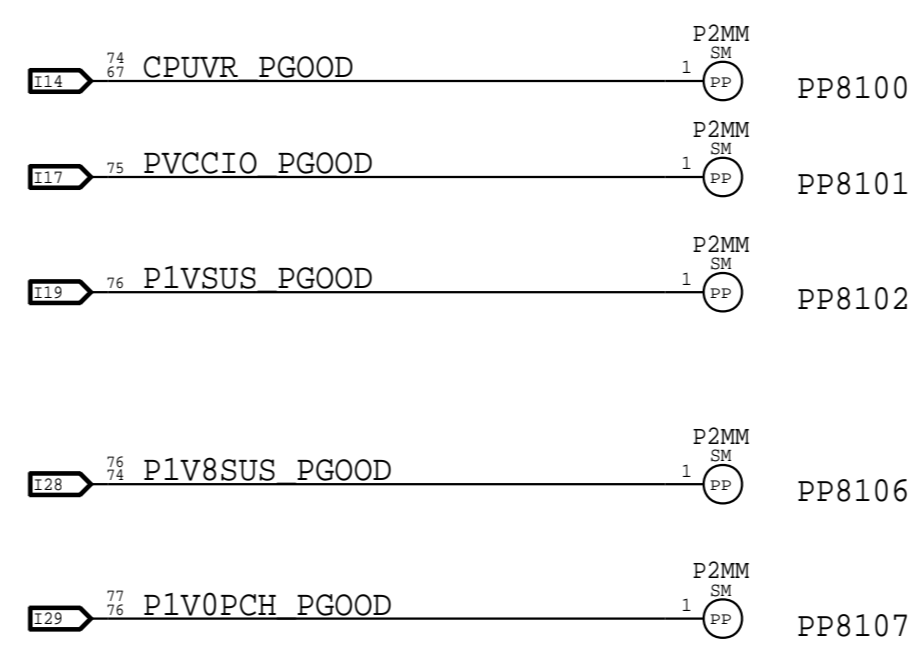
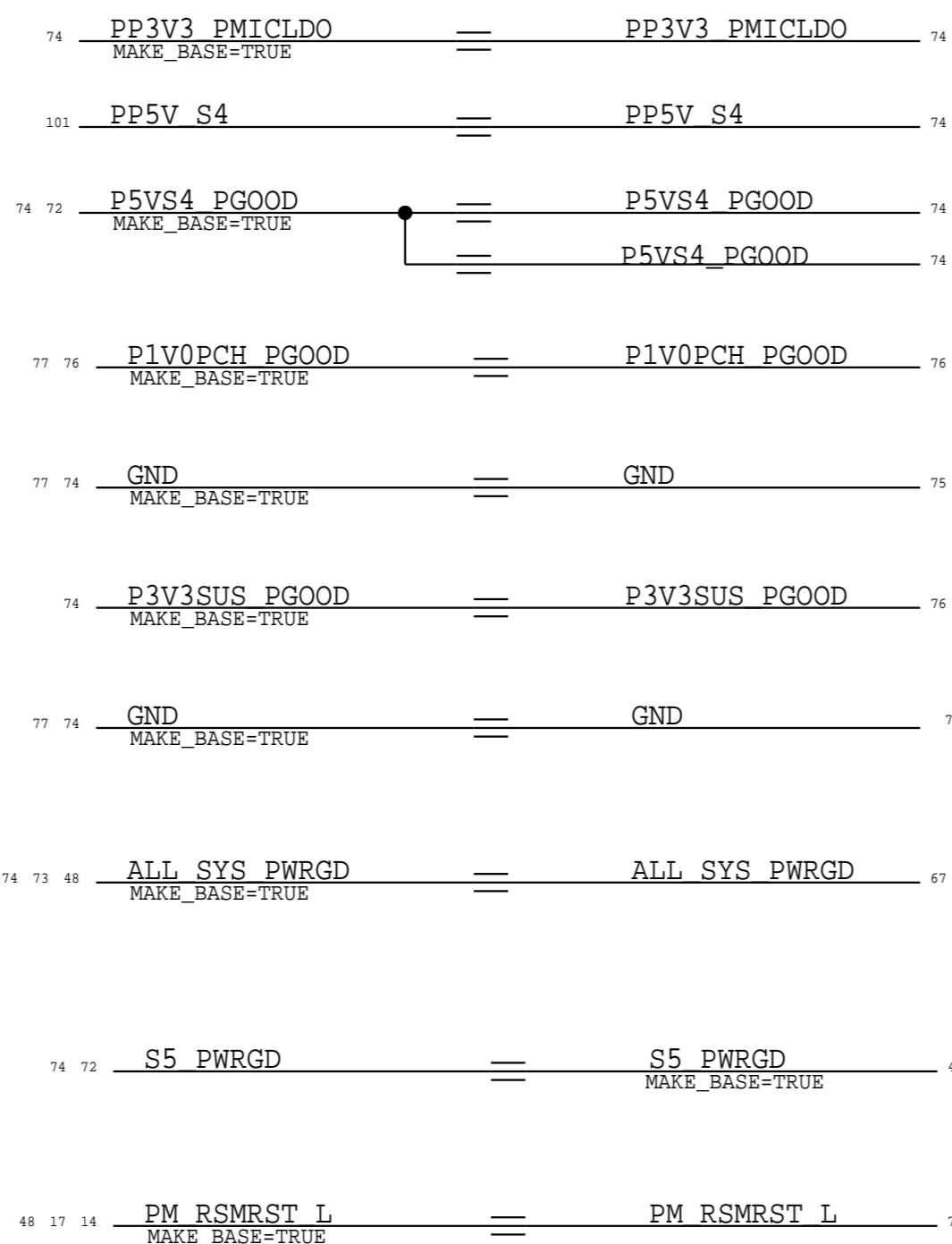
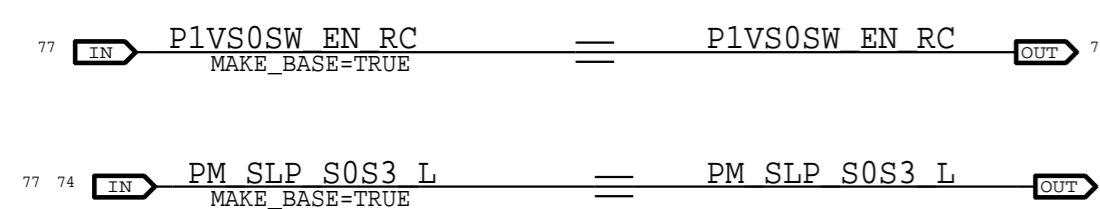
S3 Enables



S0 Enables

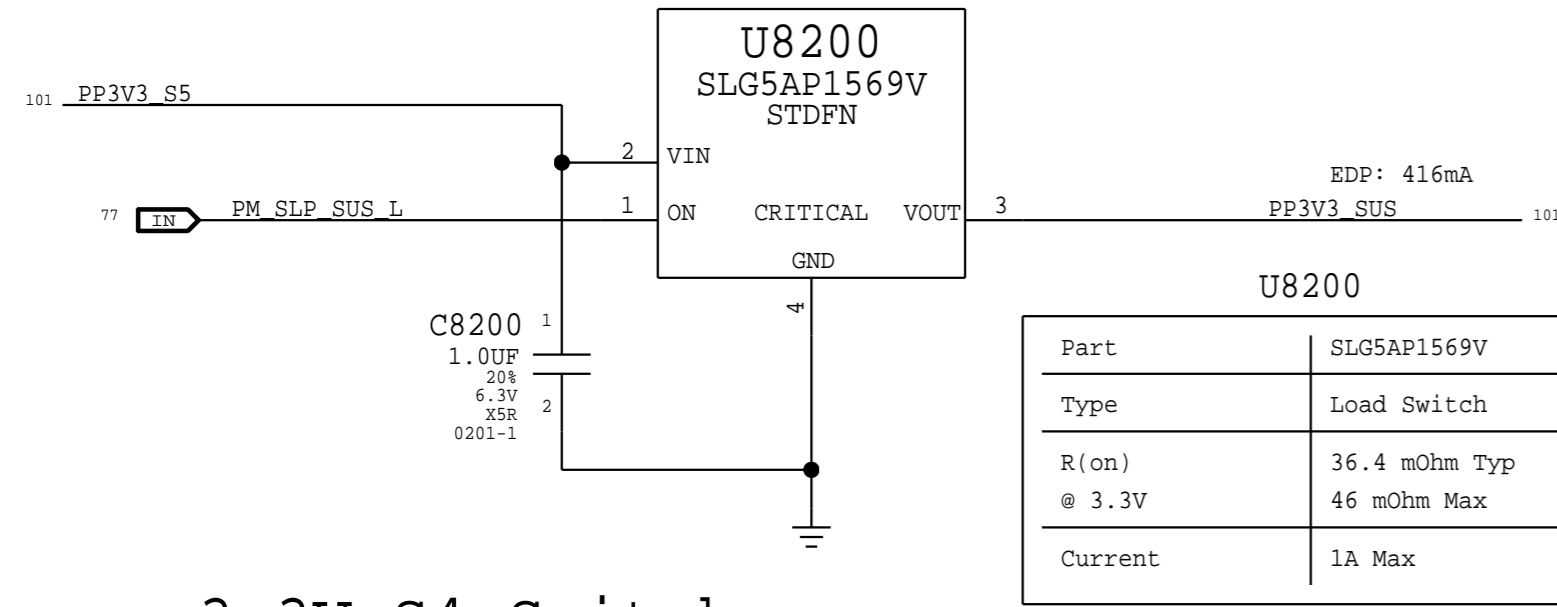


S0i Enables

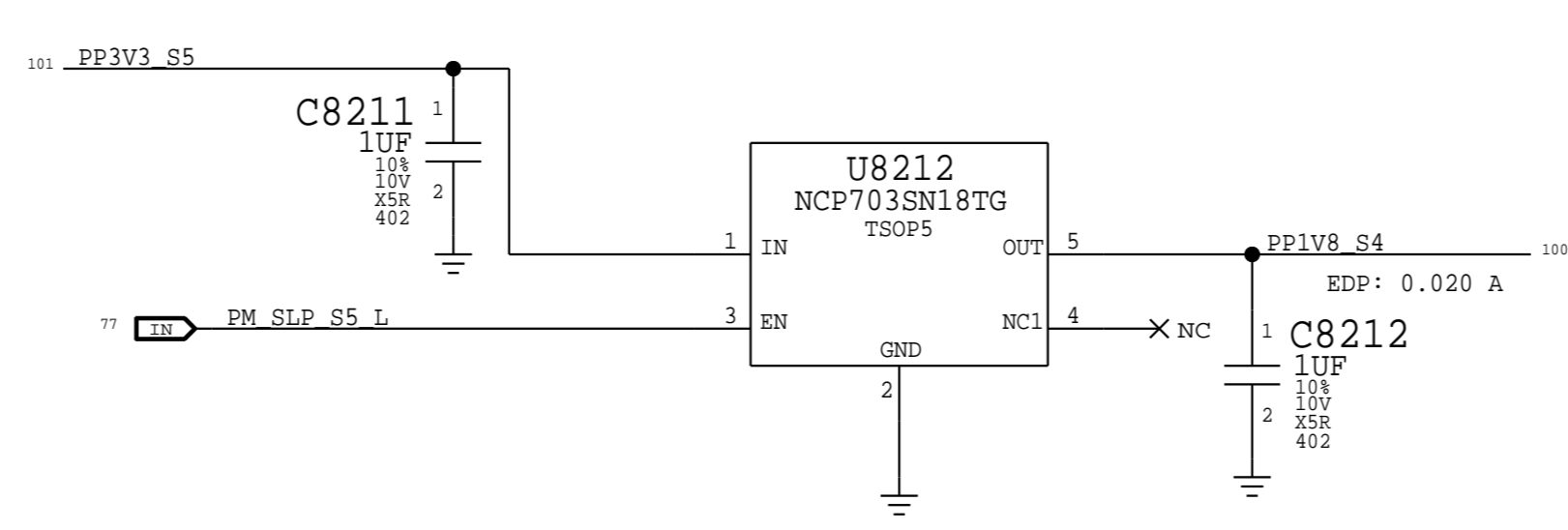


| | | |
|---|----------------|-------------|
| PAGE TITLE PMIC-1 Aliases & TPS | | |
| Apple Inc. | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 11 ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 81 OF 145 |
| | SHEET | 77 OF 119 |

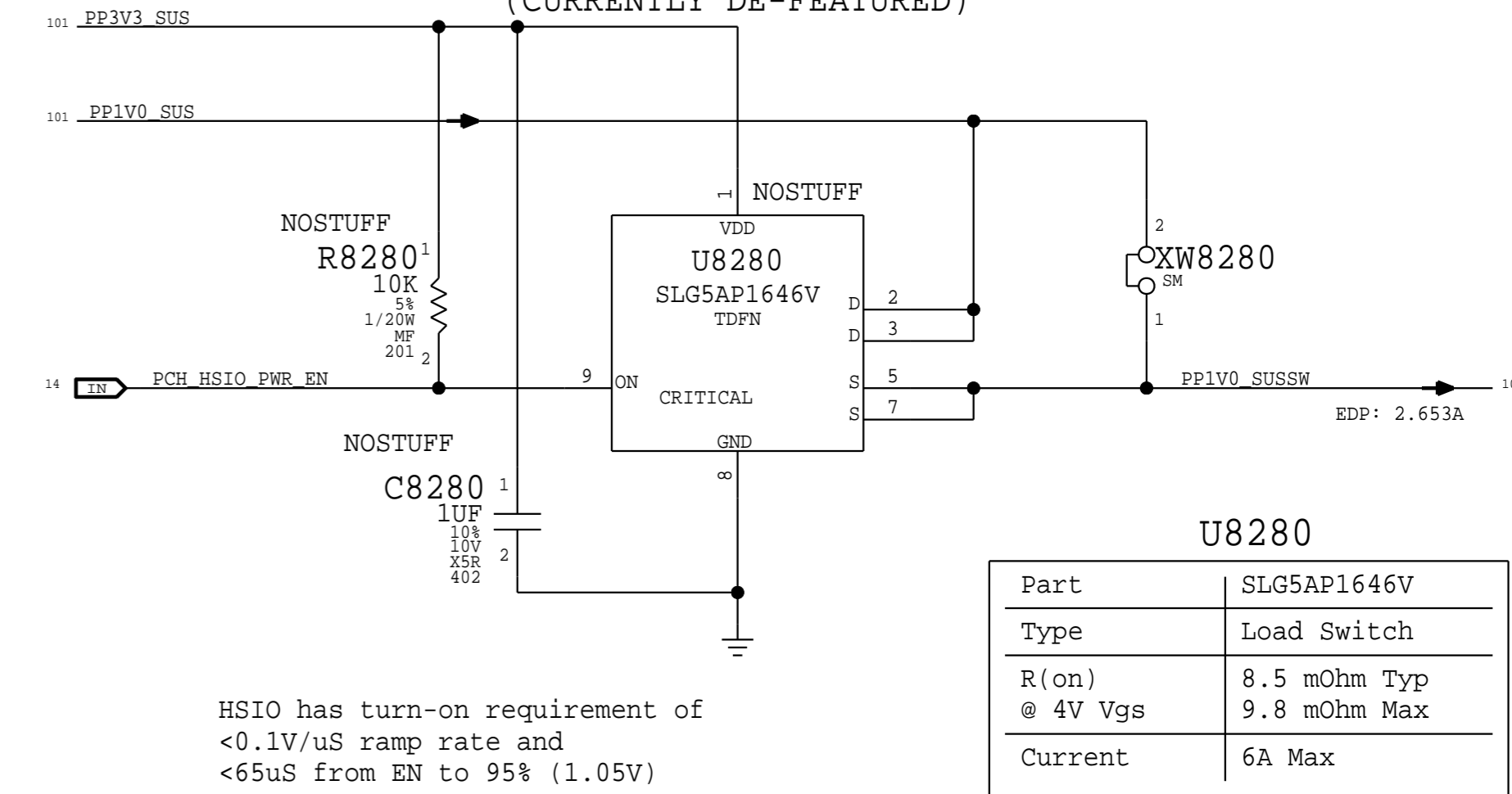
3.3V SUS Switch



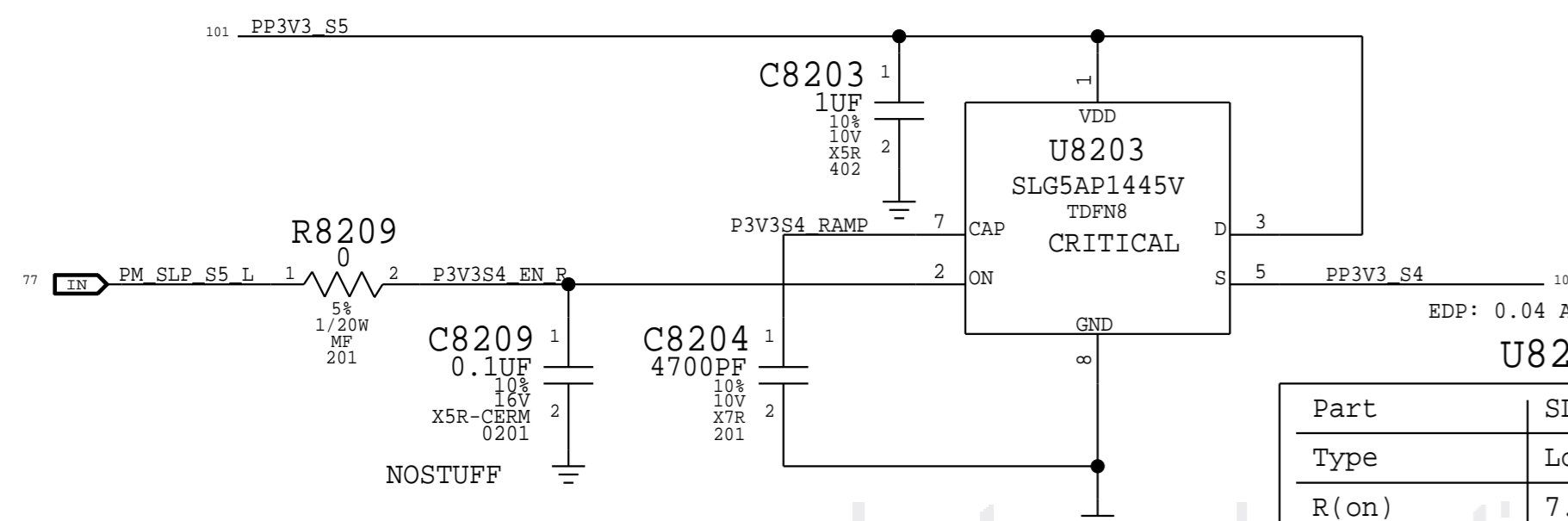
1.8V S4 LDO



1.0V SUS SW Switch (CURRENTLY DE-FEATURED)



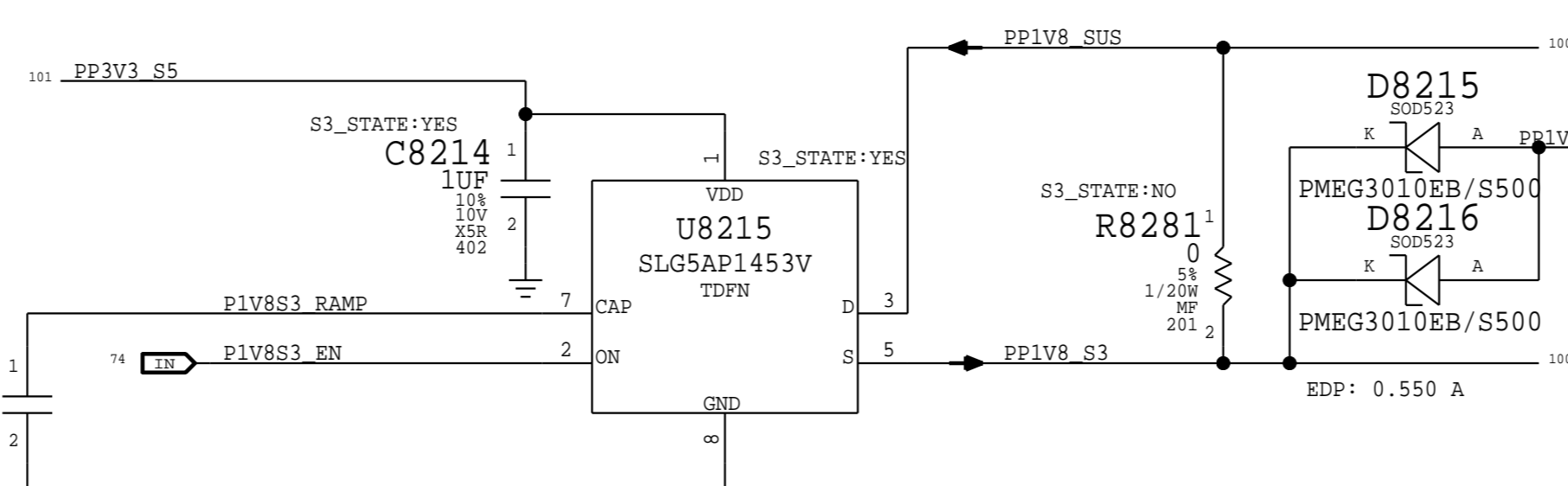
3.3V S4 Switch



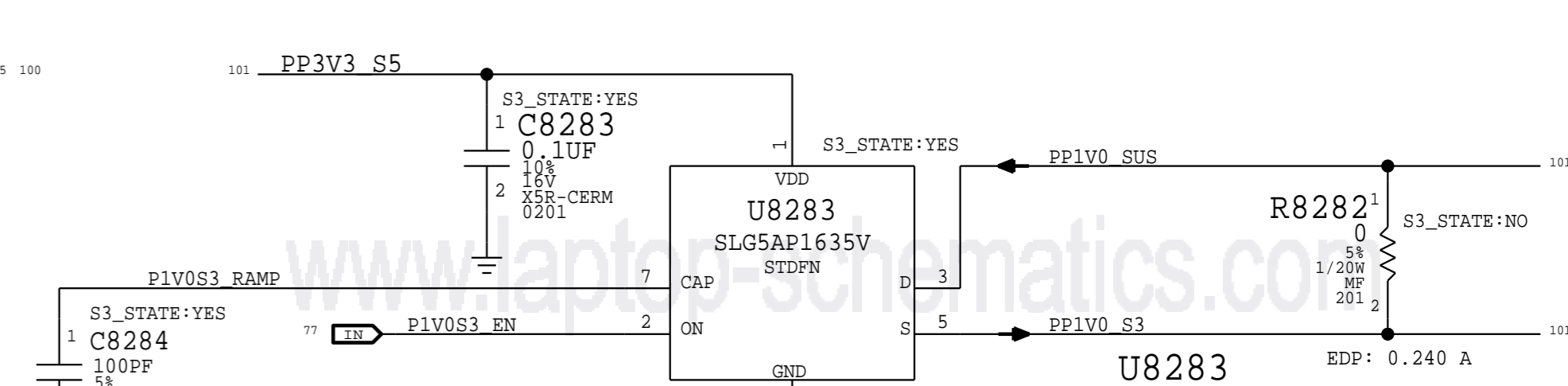
U8215

| Part | SLG5AP1453V |
|--------------|------------------------------|
| Type | Load Switch |
| R(on) @ 5.3A | 7.8 mOhm Typ 9.6 mOhm Max |
| Current | 5.3A Max |

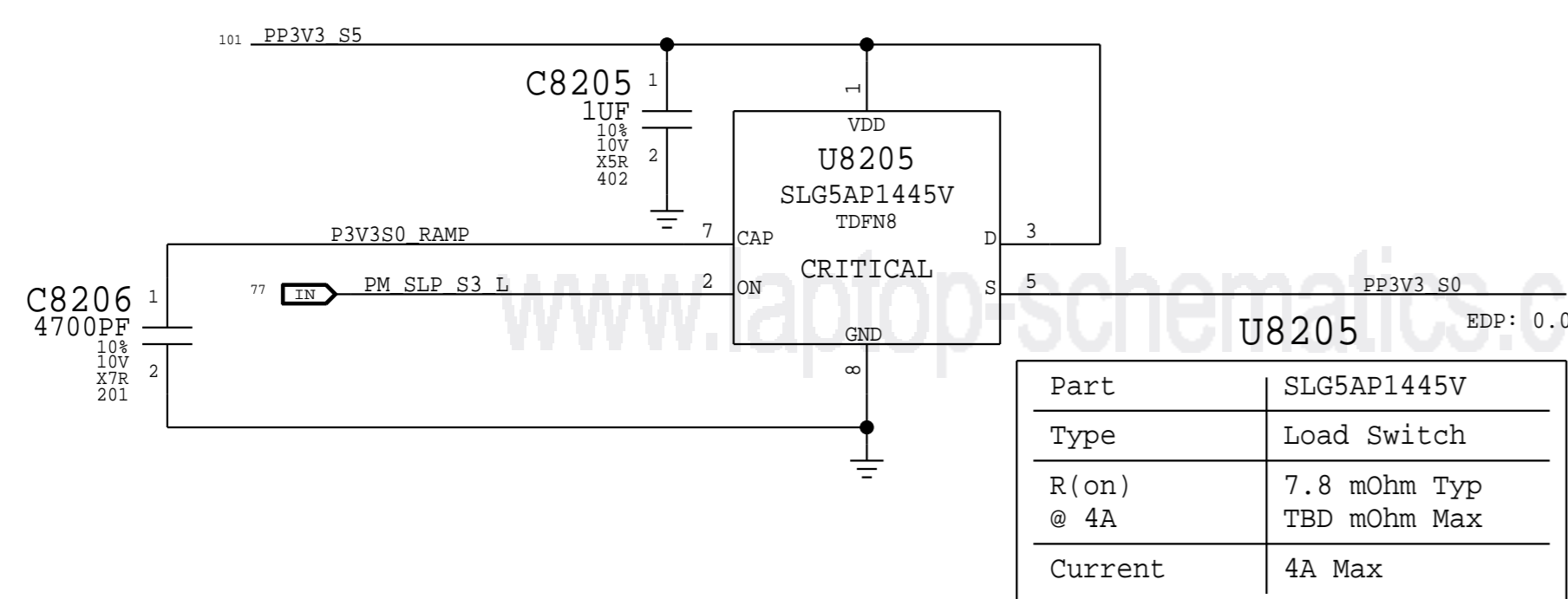
1.8V S3 Switch



1.0V S3 Switch



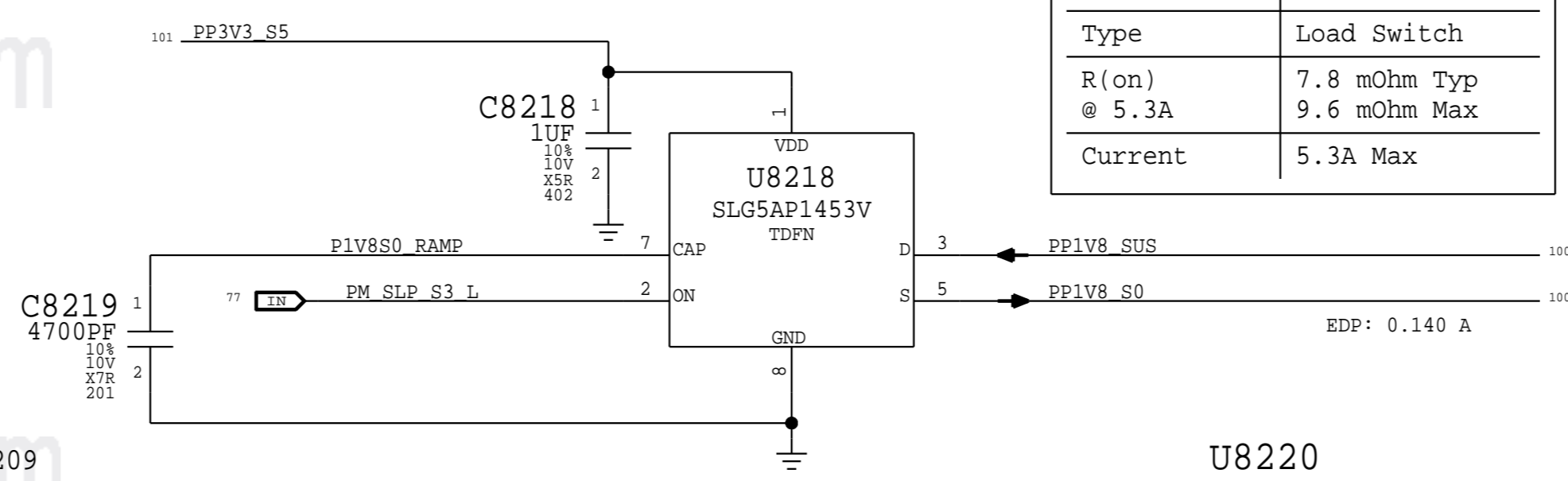
3.3V S0 Switch



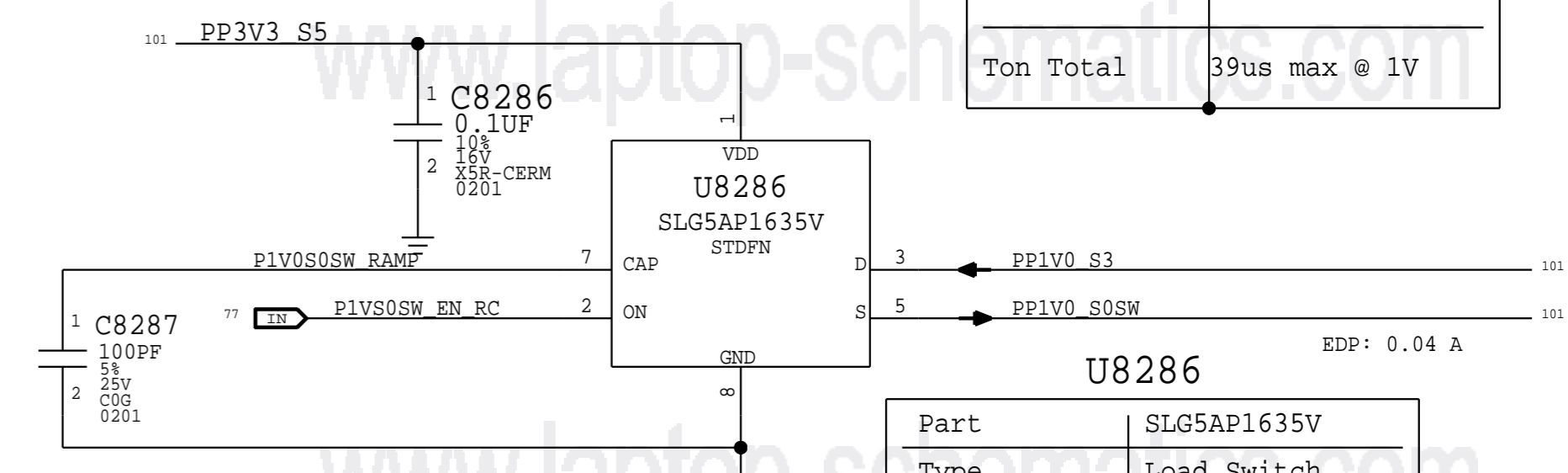
U8218

| Part | SLG5AP1453V |
|--------------|------------------------------|
| Type | Load Switch |
| R(on) @ 5.3A | 7.8 mOhm Typ 9.6 mOhm Max |
| Current | 5.3A Max |

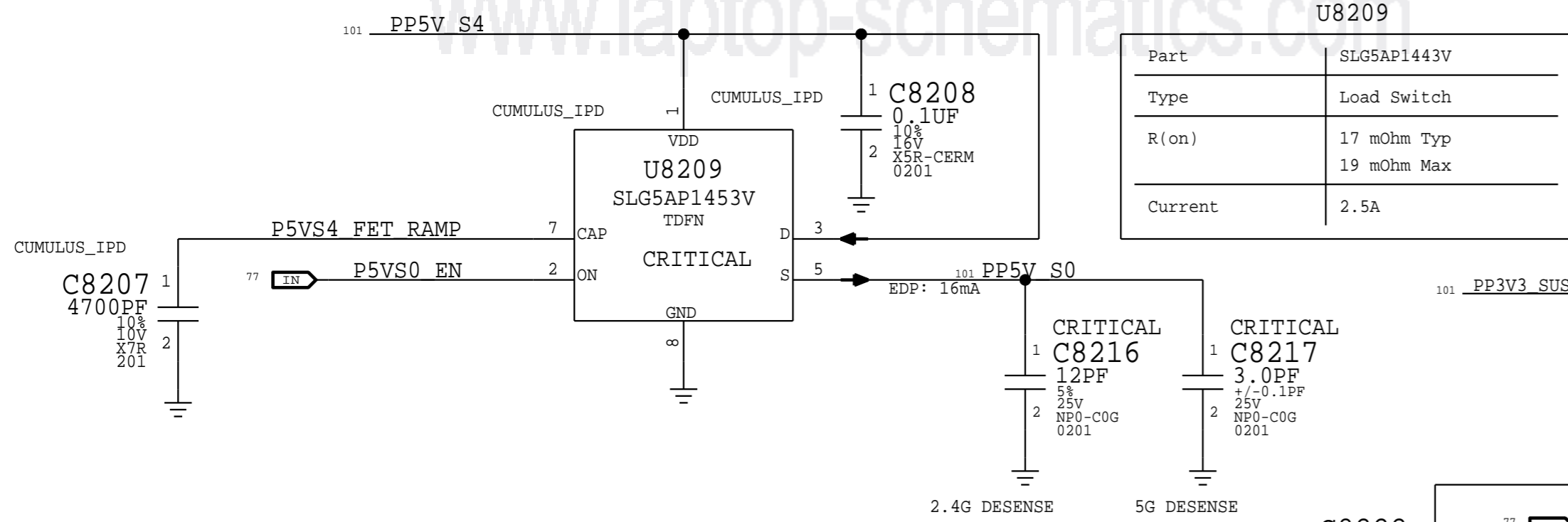
1.8V S0 Switch



1.0V S0 SW Switch



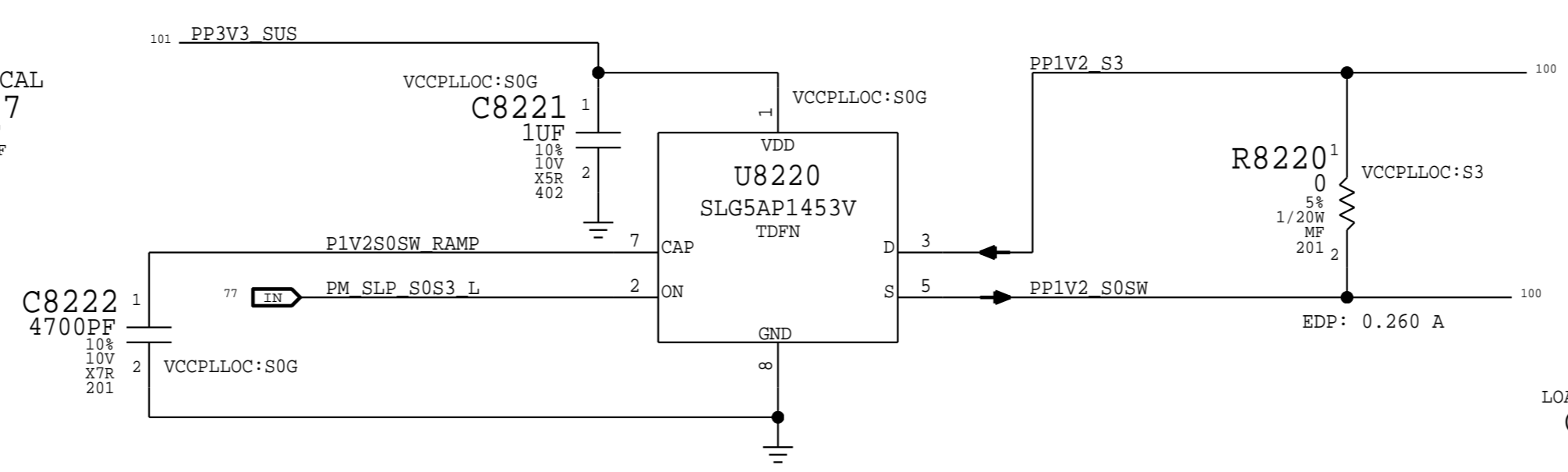
5V S0 Switch (Cumulus vs Kona)



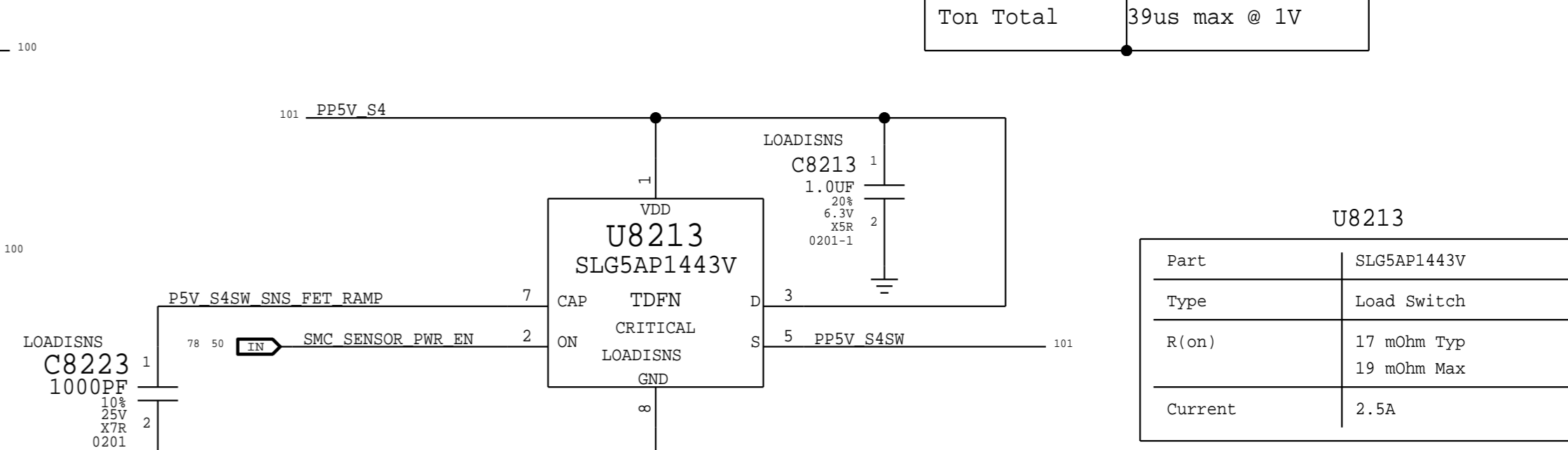
U8220

| Part | SLG5AP1453V |
|--------------|------------------------------|
| Type | Load Switch |
| R(on) @ 5.3A | 7.8 mOhm Typ 9.6 mOhm Max |
| Current | 5.3A Max |

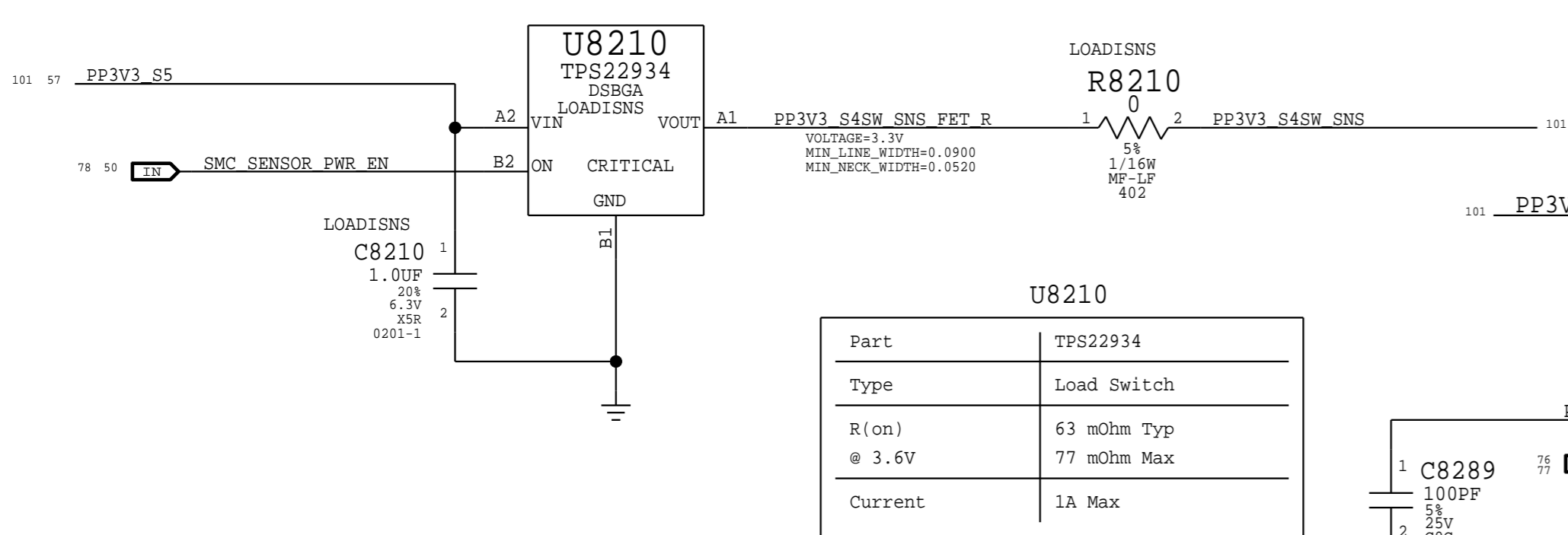
1.2V S0 SW Switch



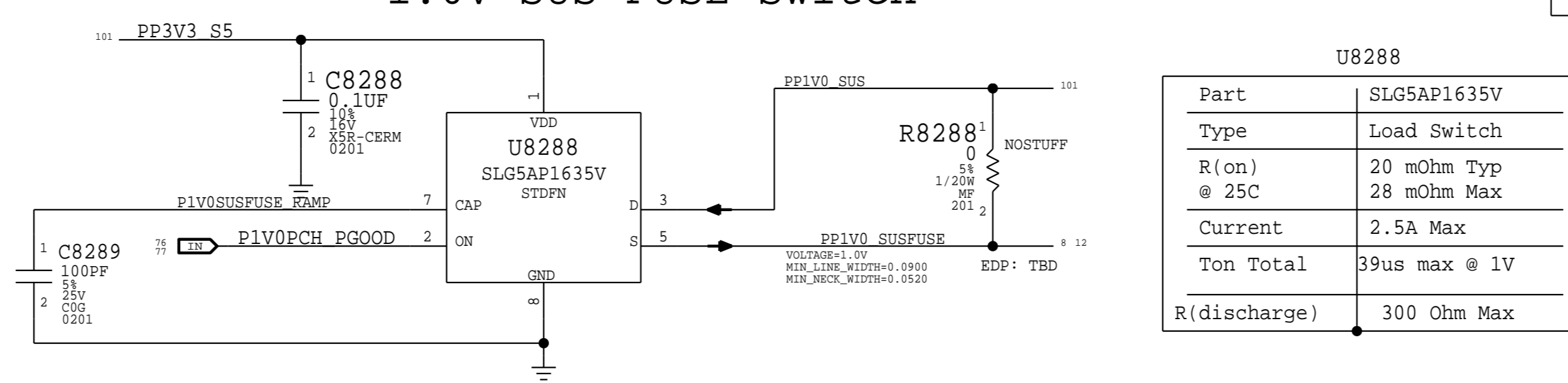
5V Sensor Switch



3.3V Sensor Switch



1.0V SUS FUSE Switch

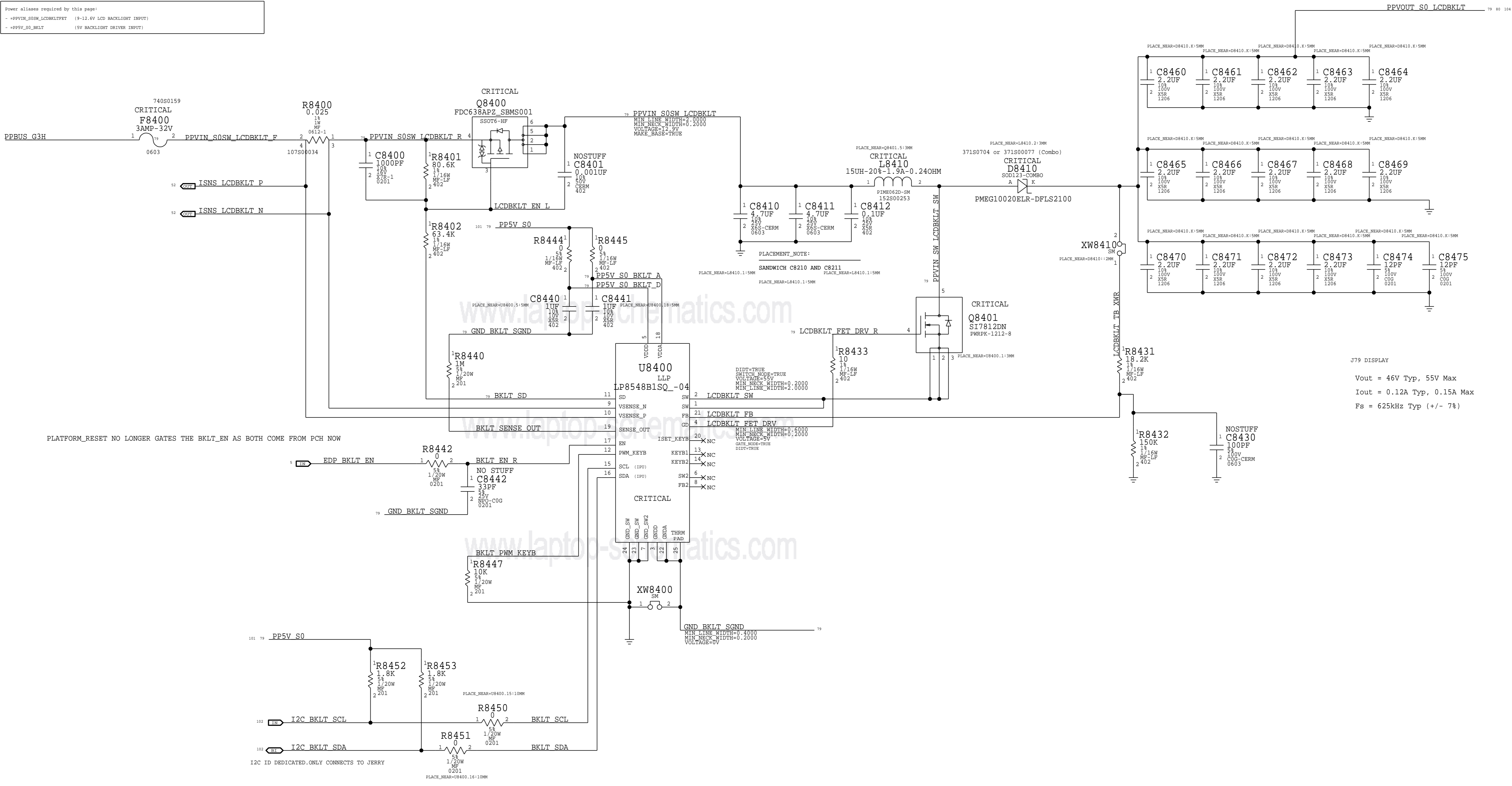


BOM_COST_GROUP=PLATFORM POWER

| Power FETs | | DRAWING NUMBER | STEP |
|--|--|----------------|-------|
| Apple Inc. | | 051-00777 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 114 ALL RIGHTS RESERVED | | REVISION | SHEET |
| | | 9.0.0 | |
| | | branch | |
| | | dvt-fab09-0 | |
| | | PAGE | |
| | | 82 OF 145 | |
| | | SHEET | |
| | | 78 OF 119 | |

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLT_FET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

LINE WIDTHS

- PP5V_S0_BKLT_A: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- PP5V_S0_BKLT_D: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
- BKLT_SD: MIN_LINE_WIDTH=0.2500, MIN_NECK_WIDTH=0.2000

PBUS LINE WIDTHS

- PPVIN_S0SW_LCDBKLT_F: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT_R: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
- PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V

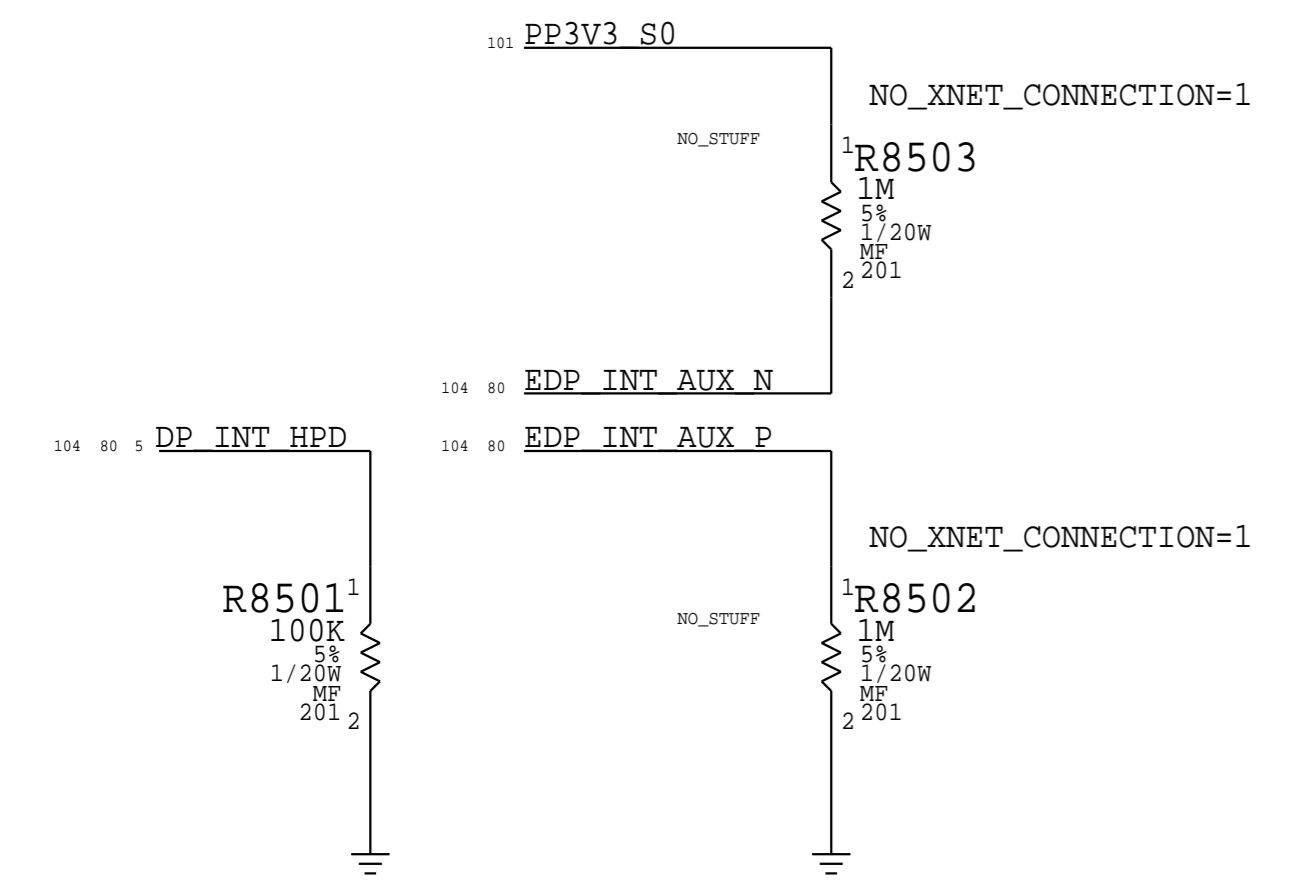
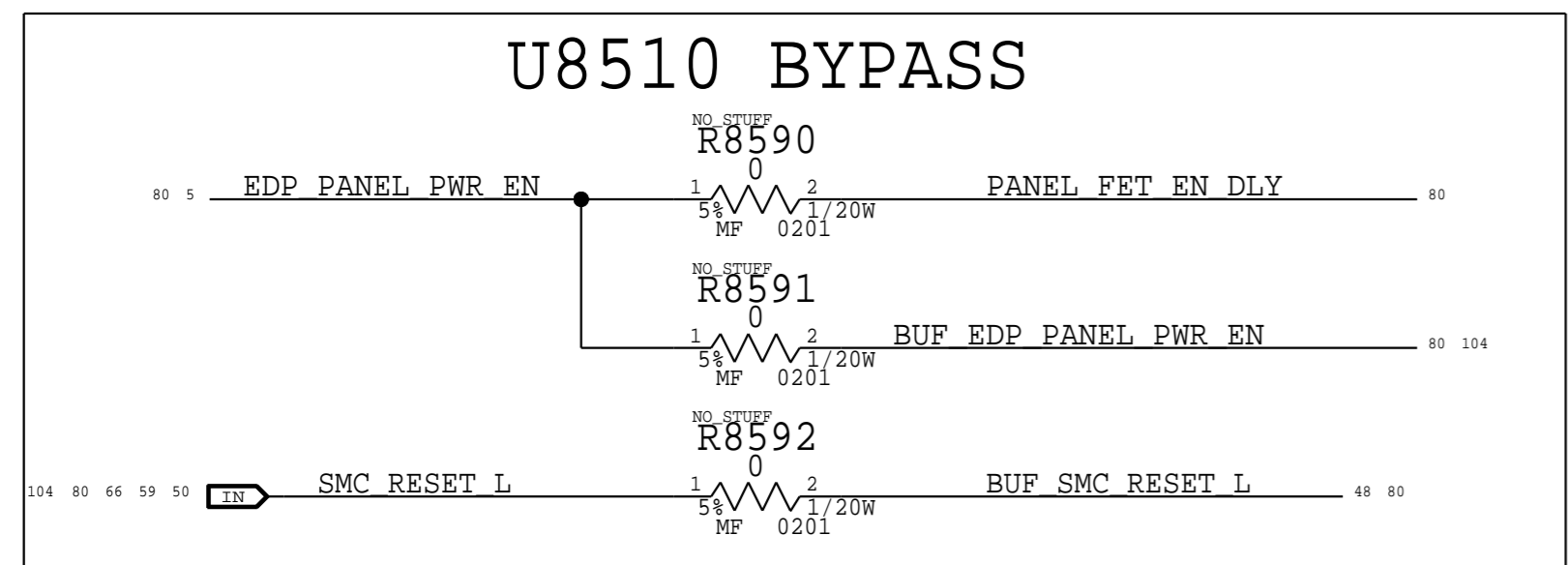
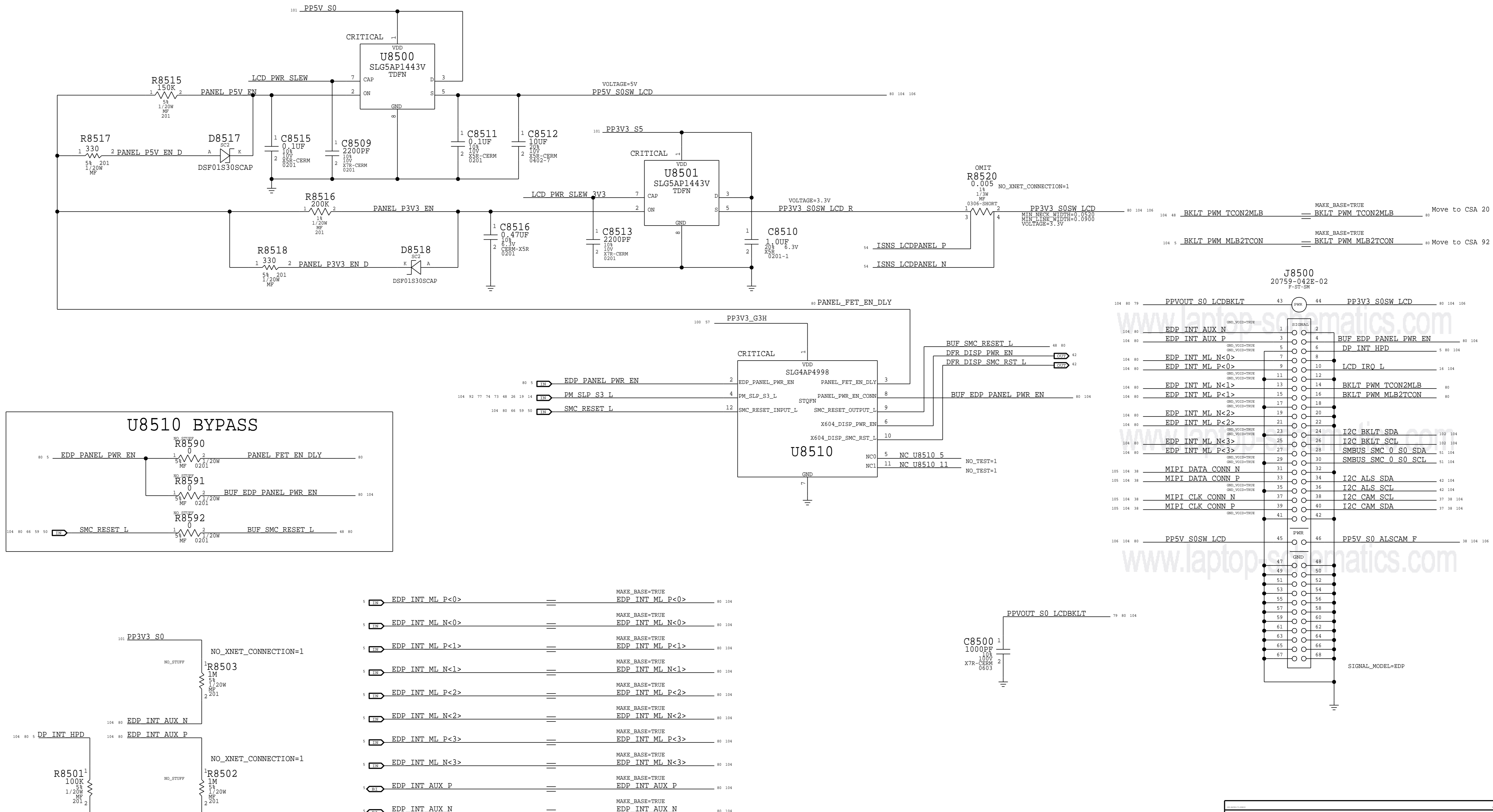
LCD BKLT LINE WIDTHS

- LCDBKLT_FET_DRV_R: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
- PPVIN_SW_LCDBKLT_SW: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V, SWITCH_NODE=TRUE, DIDT=TRUE
- PPVOUT_S0_LCDBKLT: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1500, VOLTAGE=5V

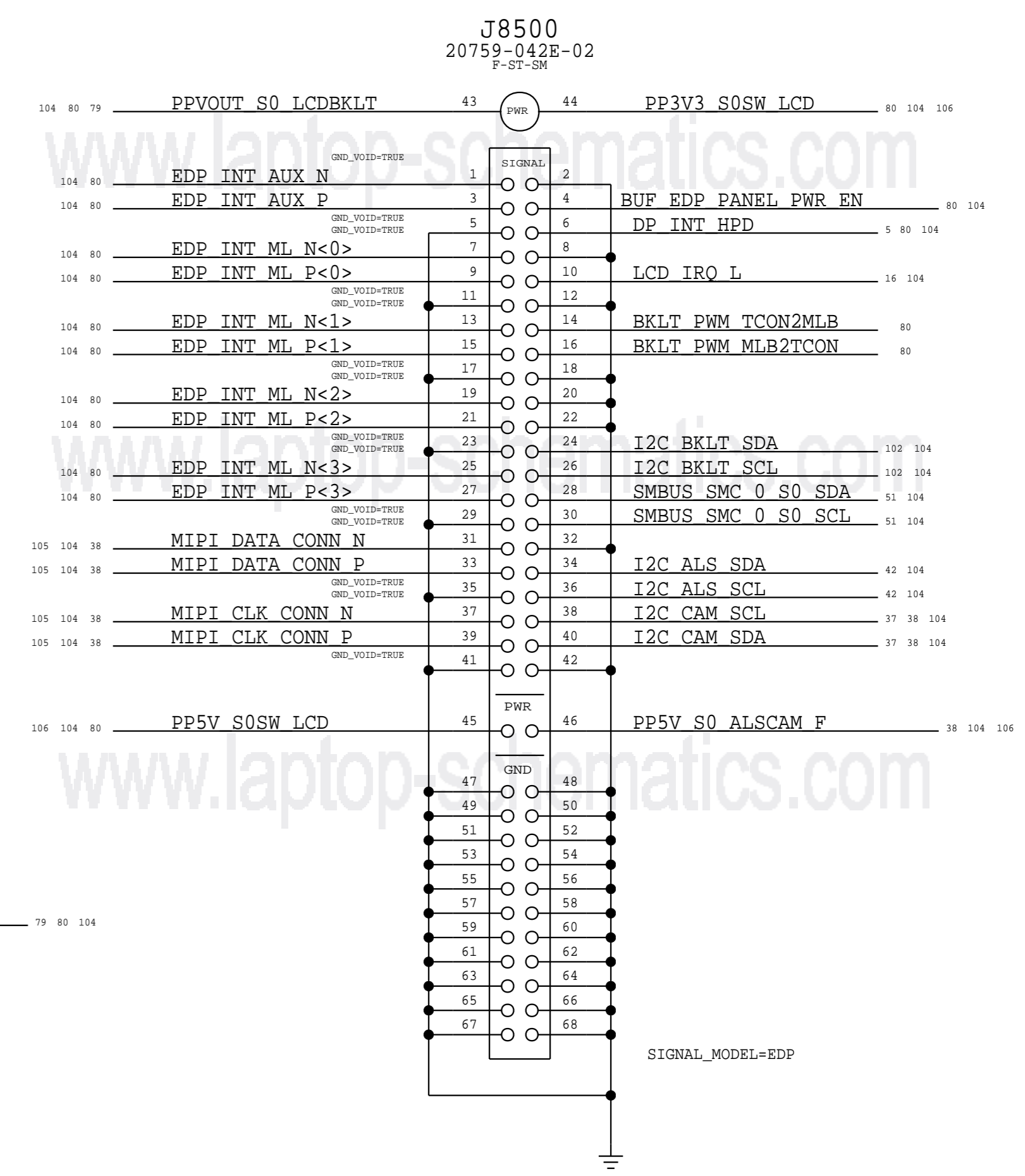
J79 DISPLAY
Vout = 46V Typ, 55V Max
Iout = 0.12A Typ, 0.15A Max
Fs = 625kHz Typ (+/- 7%)

| | |
|---|--|
| LCD Backlight Driver | |
| Apple Inc. | DRWGNG NUMBER: 051-00777 |
| | REVISION: 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | BRANCH: dvt-fab09-0 PAGE: 84 OF 145 SHEET: 79 OF 119 |

LCD PANEL INTERFACE (eDP) + Camera (MIPI)



| | | | | | |
|---|----|-----------------|----|-----------------------------------|--------|
| 5 | IN | EDP INT ML P<0> | == | MAKE_BASE=TRUE EDP INT ML P<0> | 80 104 |
| 5 | IN | EDP INT ML N<0> | == | MAKE_BASE=TRUE EDP INT ML N<0> | 80 104 |
| 5 | IN | EDP INT ML P<1> | == | MAKE_BASE=TRUE EDP INT ML P<1> | 80 104 |
| 5 | IN | EDP INT ML N<1> | == | MAKE_BASE=TRUE EDP INT ML N<1> | 80 104 |
| 5 | IN | EDP INT ML P<2> | == | MAKE_BASE=TRUE EDP INT ML P<2> | 80 104 |
| 5 | IN | EDP INT ML N<2> | == | MAKE_BASE=TRUE EDP INT ML N<2> | 80 104 |
| 5 | IN | EDP INT ML P<3> | == | MAKE_BASE=TRUE EDP INT ML P<3> | 80 104 |
| 5 | IN | EDP INT ML N<3> | == | MAKE_BASE=TRUE EDP INT ML N<3> | 80 104 |
| 5 | IN | EDP INT AUX P | == | MAKE_BASE=TRUE EDP INT AUX P | 80 104 |
| 5 | IN | EDP INT AUX N | == | MAKE_BASE=TRUE EDP INT AUX N | 80 104 |



| | | | |
|----------------|--|------------------------------|------|
| PAGE TITLE | | eDP Display Connector | |
| DRAWING NUMBER | | 051-00777 | STEP |
| REVISION | | 9.0.0 | D |
| BRANCH | | dvt-fab09-0 | |
| PAGE | | 85 OF 145 | |
| SHEET | | 80 OF 119 | |

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
11V ALL RIGHTS RESERVED

NAND LANDINGS

| CONFIG | LANDING1 R8601 | LANDING0 R8660 |
|---------------|-------------------|-------------------|
| 00 - 2 | NOSTUFF | NOSTUFF |
| 01 - 4 | NOSTUFF | ASSEMBLE |
| 10 - 8 | ASSEMBLE | NOSTUFF |
| 11 - RESERVED | ASSEMBLE | ASSEMBLE |

NAND CONFIGURATION

| CONFIG | ROMBOOT2 R8617 | ROMBOOT1 R8618 | ROMBOOT0 R8616 |
|---|-------------------|-------------------|-------------------|
| 000 - MLC SD/TOS 1Y/1Z (W/ HARD RESET) | NOSTUFF | NOSTUFF | NOSTUFF |
| 001 - MLC SD/TOS 1Y/1Z (W/O HARD RESET) | NOSTUFF | NOSTUFF | ASSEMBLE |
| 010 - RESERVED | NOSTUFF | ASSEMBLE | NOSTUFF |
| 011 - MLC HYNIX 3D-V2 | NOSTUFF | ASSEMBLE | ASSEMBLE |
| 100 - RESERVED | NOSTUFF | NOSTUFF | NOSTUFF |
| 101 - RESERVED | ASSEMBLE | NOSTUFF | ASSEMBLE |
| 110 - RESERVED | ASSEMBLE | ASSEMBLE | NOSTUFF |
| 111 - RESERVED | ASSEMBLE | ASSEMBLE | ASSEMBLE |

OPERATION MODE (ODT, CLK FREQ, ETC)

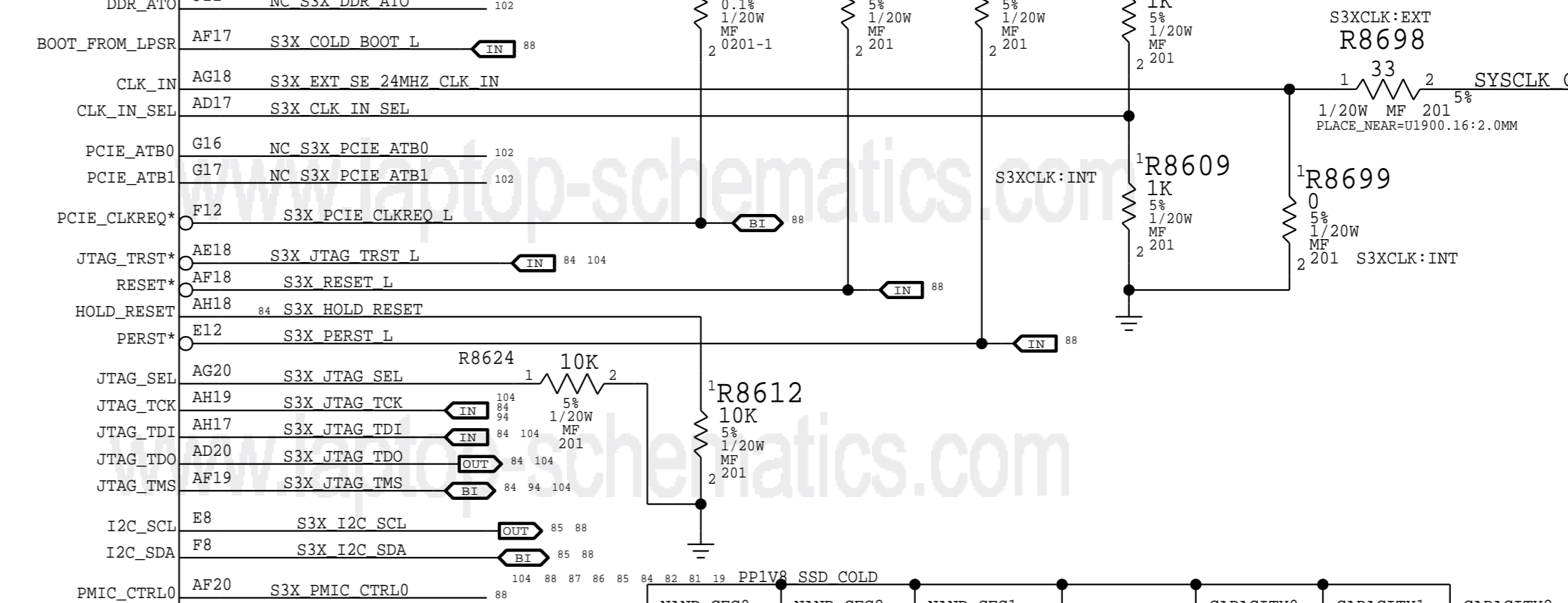
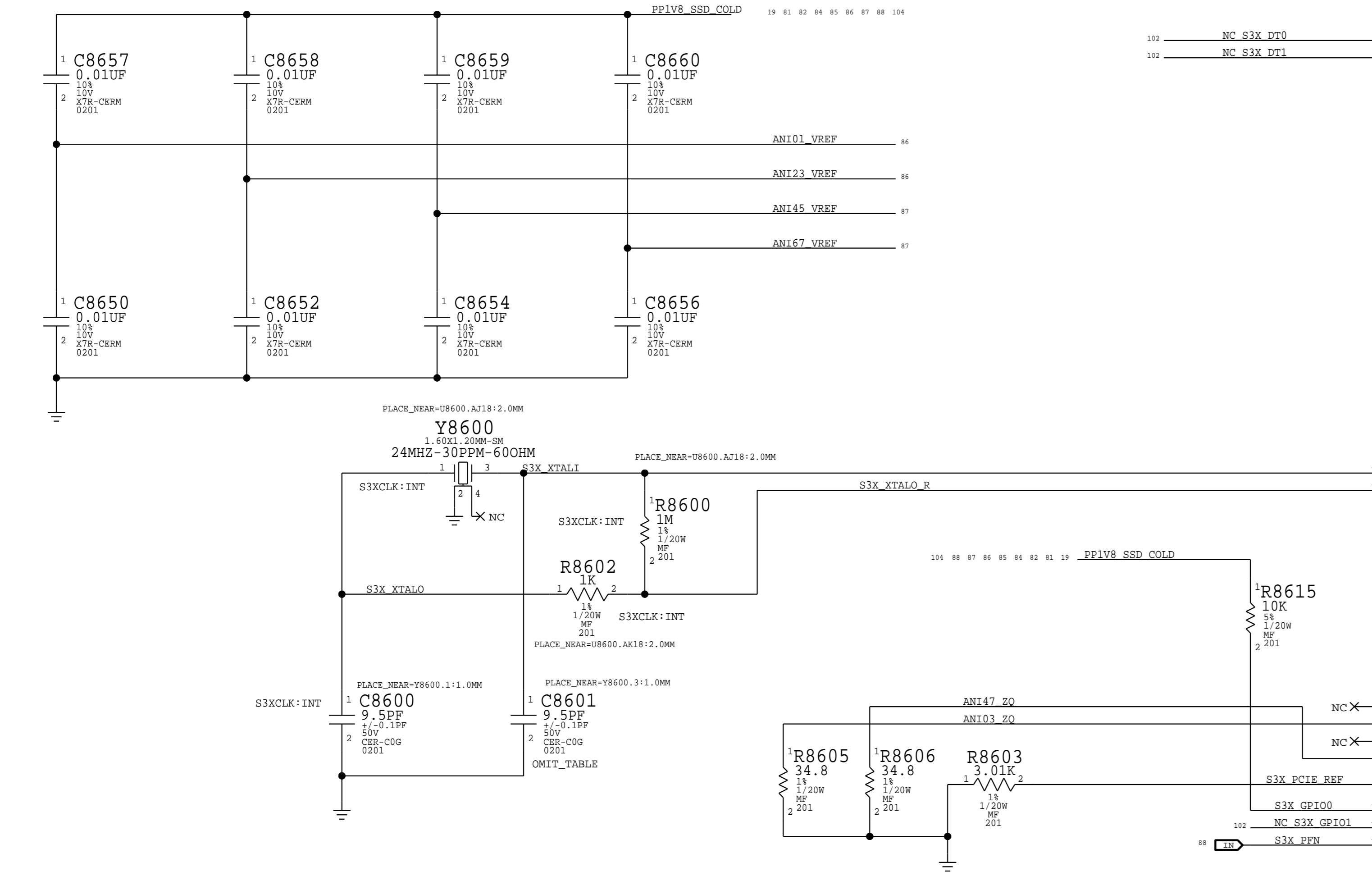
| CONFIG | OP_MODE2 R8614 | OP_MODE1 R8615 | OP_MODE0 R8660 |
|----------------|-------------------|-------------------|-------------------|
| 000 - TEABERRY | NOSTUFF | NOSTUFF | NOSTUFF |
| 001 - XB58 GS | NOSTUFF | NOSTUFF | ASSEMBLE |
| 010 - RESERVED | NOSTUFF | ASSEMBLE | NOSTUFF |
| 011 - RESERVED | NOSTUFF | ASSEMBLE | ASSEMBLE |
| 100 - RESERVED | ASSEMBLE | NOSTUFF | NOSTUFF |
| 101 - RESERVED | ASSEMBLE | NOSTUFF | ASSEMBLE |
| 110 - RESERVED | ASSEMBLE | ASSEMBLE | NOSTUFF |
| 111 - RESERVED | ASSEMBLE | ASSEMBLE | ASSEMBLE |

PRODUCT CAPACITY

| CONFIG | CAPACITY2 R8664 | CAPACITY1 R8663 | CAPACITY0 R8662 |
|----------------|--------------------|--------------------|--------------------|
| 000 - 32GB | NOSTUFF | NOSTUFF | NOSTUFF |
| 001 - 64GB | NOSTUFF | NOSTUFF | ASSEMBLE |
| 010 - 128GB | NOSTUFF | ASSEMBLE | NOSTUFF |
| 011 - 256GB | NOSTUFF | ASSEMBLE | ASSEMBLE |
| 100 - 512GB | ASSEMBLE | NOSTUFF | NOSTUFF |
| 101 - 1024GB | ASSEMBLE | NOSTUFF | ASSEMBLE |
| 110 - 2048GB | ASSEMBLE | ASSEMBLE | NOSTUFF |
| 111 - RESERVED | ASSEMBLE | ASSEMBLE | ASSEMBLE |

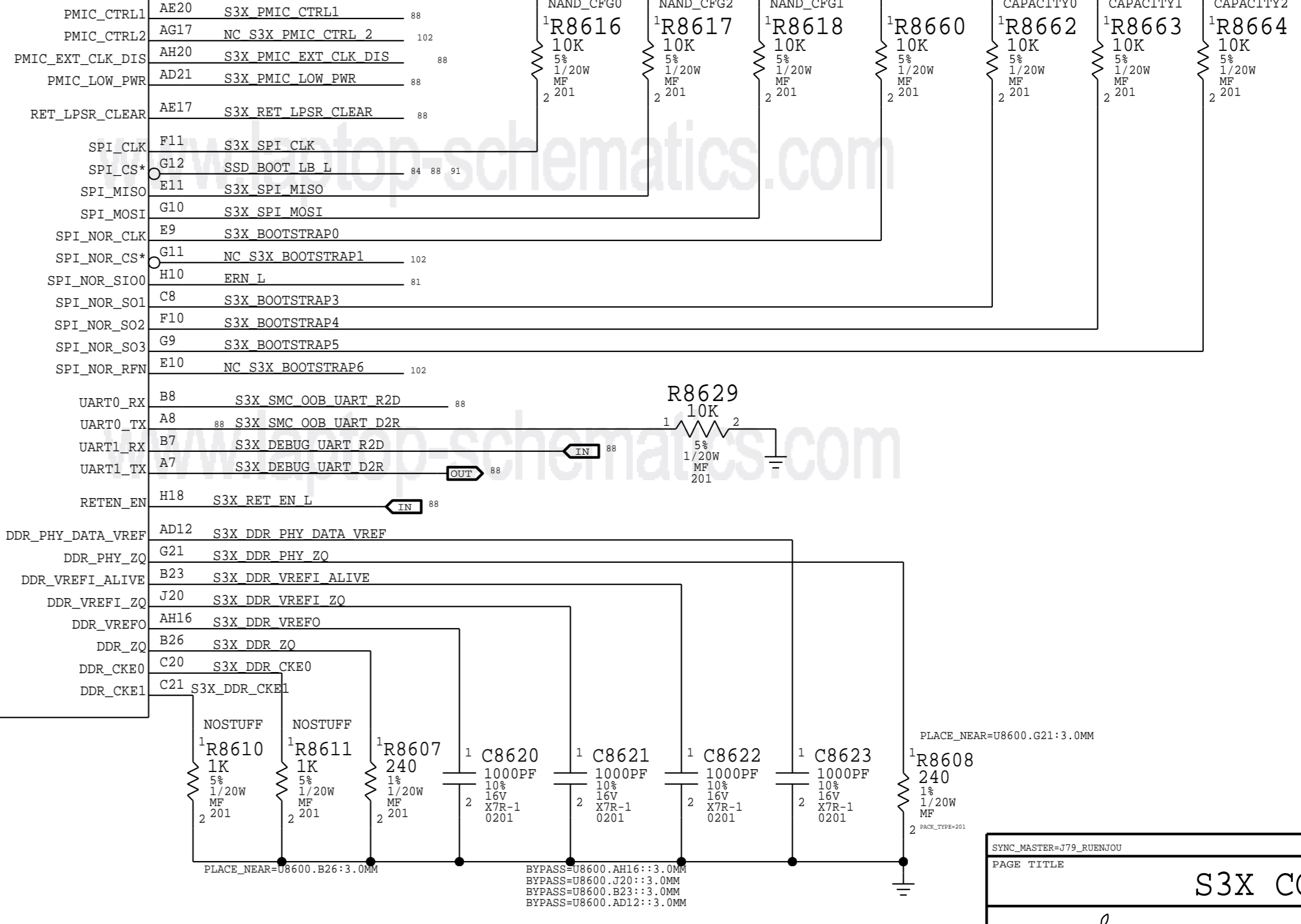
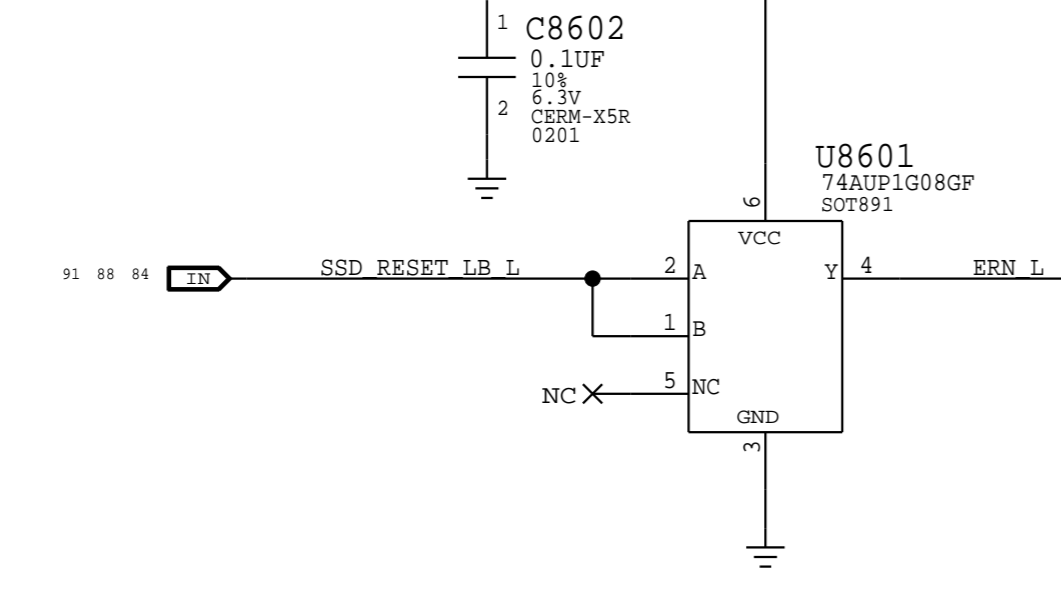
OMIT_TABLE
U8600
S3X
BGA-H1P35
SYM 3 OF 7

| REF | VALUE | REF | VALUE | REF | VALUE | REF | VALUE |
|-----|-----------------------|-----|-------|-----|-------|-----|-------|
| A19 | PCIE_CLK100M SSD LB P | 91 | 105 | 91 | 105 | 91 | 105 |
| A18 | PCIE_CLK100M SSD LB N | 91 | 105 | 91 | 105 | 91 | 105 |
| A17 | PCIE_SSD_D2R_C P<0> | 81 | | 81 | | 81 | |
| A16 | PCIE_SSD_D2R_C N<0> | 81 | | 81 | | 81 | |
| A15 | PCIE_SSD_D2R_C P<1> | 81 | | 81 | | 81 | |
| A14 | PCIE_SSD_D2R_C N<1> | 81 | | 81 | | 81 | |
| A13 | PCIE_SSD_D2R_C P<2> | 81 | | 81 | | 81 | |
| A12 | PCIE_SSD_D2R_C N<2> | 81 | | 81 | | 81 | |
| A11 | PCIE_SSD_D2R_C P<3> | 81 | | 81 | | 81 | |
| A10 | PCIE_SSD_D2R_C N<3> | 81 | | 81 | | 81 | |
| C17 | PCIE_SSD_R2D LB P<0> | 84 | | 84 | | 84 | |
| C16 | PCIE_SSD_R2D LB N<0> | 84 | | 84 | | 84 | |
| C15 | PCIE_SSD_R2D P<1> | 84 | | 84 | | 84 | |
| C14 | PCIE_SSD_R2D N<1> | 84 | | 84 | | 84 | |
| C13 | PCIE_SSD_R2D P<2> | 84 | | 84 | | 84 | |
| C12 | PCIE_SSD_R2D N<2> | 84 | | 84 | | 84 | |
| C11 | PCIE_SSD_R2D P<3> | 84 | | 84 | | 84 | |
| C10 | PCIE_SSD_R2D N<3> | 84 | | 84 | | 84 | |



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-----------------------------|---------------|----------|------------|
| 131S00077 | 1 | CAP, 9.5PF, 50V, 0201 | C8601 | CRITICAL | S3XCLK:INT |
| 117S0002 | 1 | RES, MF, 0 OHM, 1/20W, 0201 | C8601 | CRITICAL | S3XCLK:EXT |

Buffered SSD_RESET L to Mitigate EPO Issue



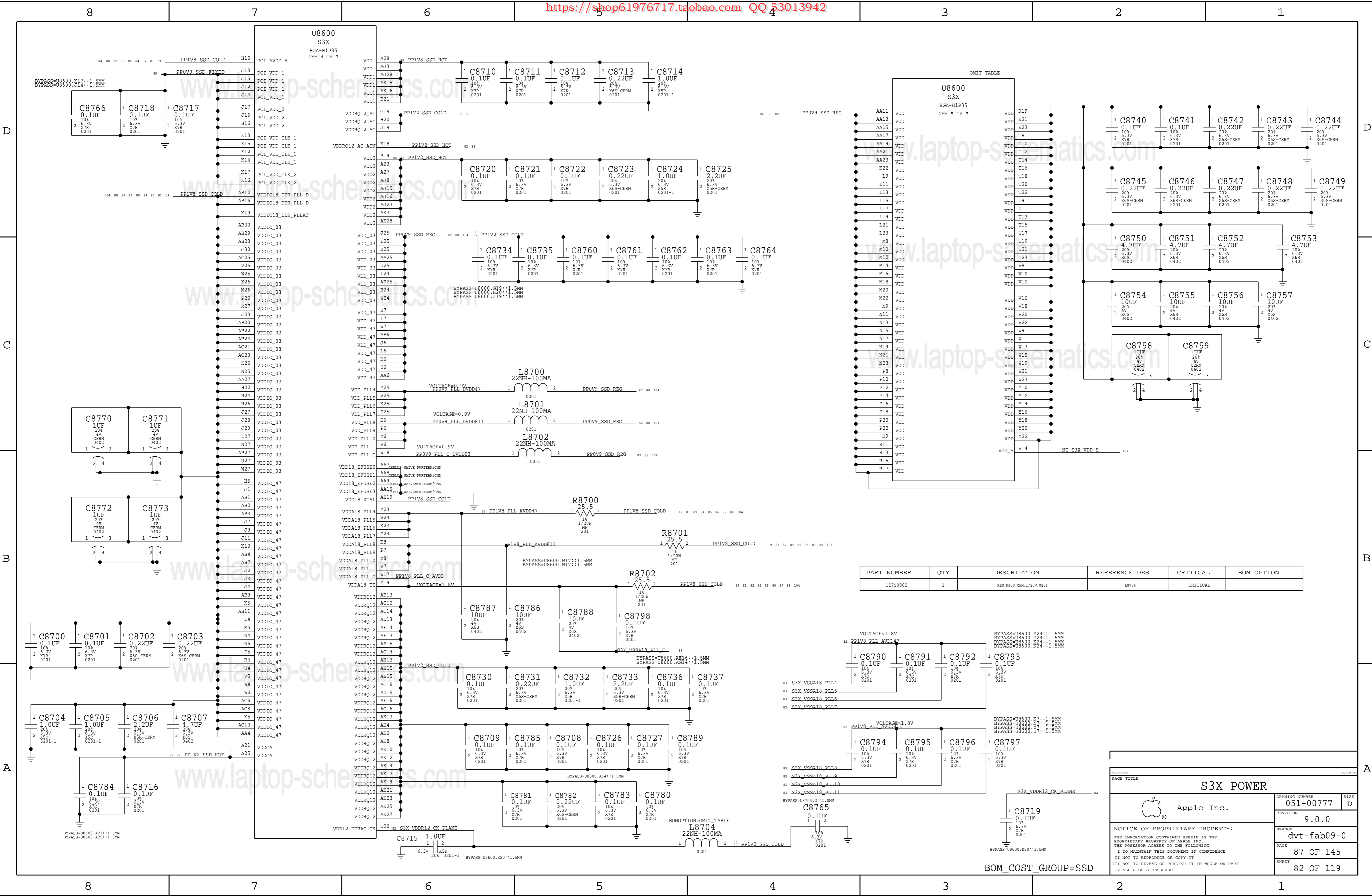
S3X CORE PCIE

Apple Inc.

DRWING NUMBER: 051-00777
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 86 OF 145
SHEET: 81 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
I NOT TO REPRODUCE OR COPY IT
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART


BOM_COST_GROUP=SSD



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-----------------------------|---------------|----------|------------|
| 11750002 | 1 | RES, MF, 0 OHM, 1/20W, 0201 | L8704 | CRITICAL | |

PAGE TITLE

S3X POWER



Apple Inc.

DRAWING NUMBER
051-00777

REVISION
9.0.0

BRANCH
dvt-fab09-0

PAGE
87 OF 145

SHEET
82 OF 119

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
11 NOT TO REPRODUCE OR COPY IT
111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
114 ALL RIGHTS RESERVED

BOM_COST_GROUP=S3D

OMIT_TABLE

OMIT_TABLE

#2 S3X_VSSA18_P1L4 Y24 VSS_P1L4
 #2 S3X_VSSA18_P1L5 U24 VSS_P1L5
 #2 S3X_VSSA18_P1L6 K24 VSS_P1L6
 #2 S3X_VSSA18_P1L7 N24 VSS_P1L7
 #2 S3X_VSSA18_P1L8 K7 VSS_P1L8
 #2 S3X_VSSA18_P1L9 N7 VSS_P1L9
 #2 S3X_VSSA18_P1L10 Y7 VSS_P1L10
 #2 S3X_VSSA18_P1L11 U7 VSS_P1L11
 #2 S3X_VSSA18_P1L_C V17 VSS_P1L_C

U8600
S3X
 BGA-HIP35
 SYM 6 OF 7

VSS AG19
 VSS AG21
 VSS AG23
 VSS AG25
 VSS AG27
 VSS AG28
 VSS AH4
 VSS AH14
 VSS AH27
 VSS AH7
 VSS AJ1
 VSS AJ2
 VSS AJ4
 VSS AJ6
 VSS AJ10
 VSS AJ12
 VSS AJ13
 VSS AJ14
 VSS AJ17
 VSS AJ19
 VSS AJ21
 VSS AJ25
 VSS AJ27
 VSS AJ29
 VSS AJ30
 VSS J18
 VSS J22
 VSS J24
 VSS J26
 VSS AK30
 VSS B1
 VSS B2
 VSS B9
 VSS B10
 VSS B11
 VSS B12
 VSS B13
 VSS B14
 VSS B15
 VSS B16
 VSS B17
 VSS B18
 VSS B27
 VSS B28
 VSS B29
 VSS B30
 VSS C5
 VSS C7
 VSS C9
 VSS C18
 VSS C22
 VSS C23
 VSS C24
 VSS C25
 VSS C26
 VSS C27
 VSS D3
 VSS D9
 VSS D10
 VSS D11
 VSS D12
 VSS D13
 VSS D14
 VSS D15
 VSS D16
 VSS D17
 VSS D18
 VSS D27
 VSS D28
 VSS E3
 VSS E13
 VSS E14
 VSS E15
 VSS E16
 VSS E17
 VSS E18
 VSS E27
 VSS E28
 VSS F3
 VSS F5
 VSS F7
 VSS F9
 VSS F13
 VSS F14
 VSS F15
 VSS F16
 VSS F17
 VSS F19
 VSS F20
 VSS F22
 VSS F24
 VSS F25
 VSS F26
 VSS F27
 VSS F28
 VSS G4
 VSS G13
 VSS G14
 VSS G15
 VSS G20
 VSS G22

U8600
S3X
 BGA-HIP35
 SYM 7 OF 7

VSS G23
 VSS G24
 VSS G25
 VSS G26
 VSS G27
 VSS H3
 VSS H4
 VSS H6
 VSS H7
 VSS H8
 VSS H11
 VSS H12
 VSS H13
 VSS H14
 VSS H19
 VSS H21
 VSS H23
 VSS H25
 VSS H27
 VSS H28
 VSS J5
 VSS J8
 VSS J10
 VSS J18
 VSS J22
 VSS J24
 VSS J26
 VSS K4
 VSS K9
 VSS K11
 VSS K21
 VSS K27
 VSS L3
 VSS L5
 VSS L8
 VSS L10
 VSS L12
 VSS L14
 VSS L16
 VSS L18
 VSS L20
 VSS L22
 VSS L26
 VSS L28
 VSS M3
 VSS M4
 VSS M6
 VSS M7
 VSS M9
 VSS M11
 VSS M13
 VSS M15
 VSS M17
 VSS M19
 VSS M21
 VSS M23
 VSS M24
 VSS M25
 VSS M27
 VSS M28
 VSS N3
 VSS N5
 VSS N8
 VSS N10
 VSS N12
 VSS N14
 VSS N16
 VSS N18
 VSS N20
 VSS N22
 VSS N26
 VSS N28
 VSS P4
 VSS P9
 VSS P11

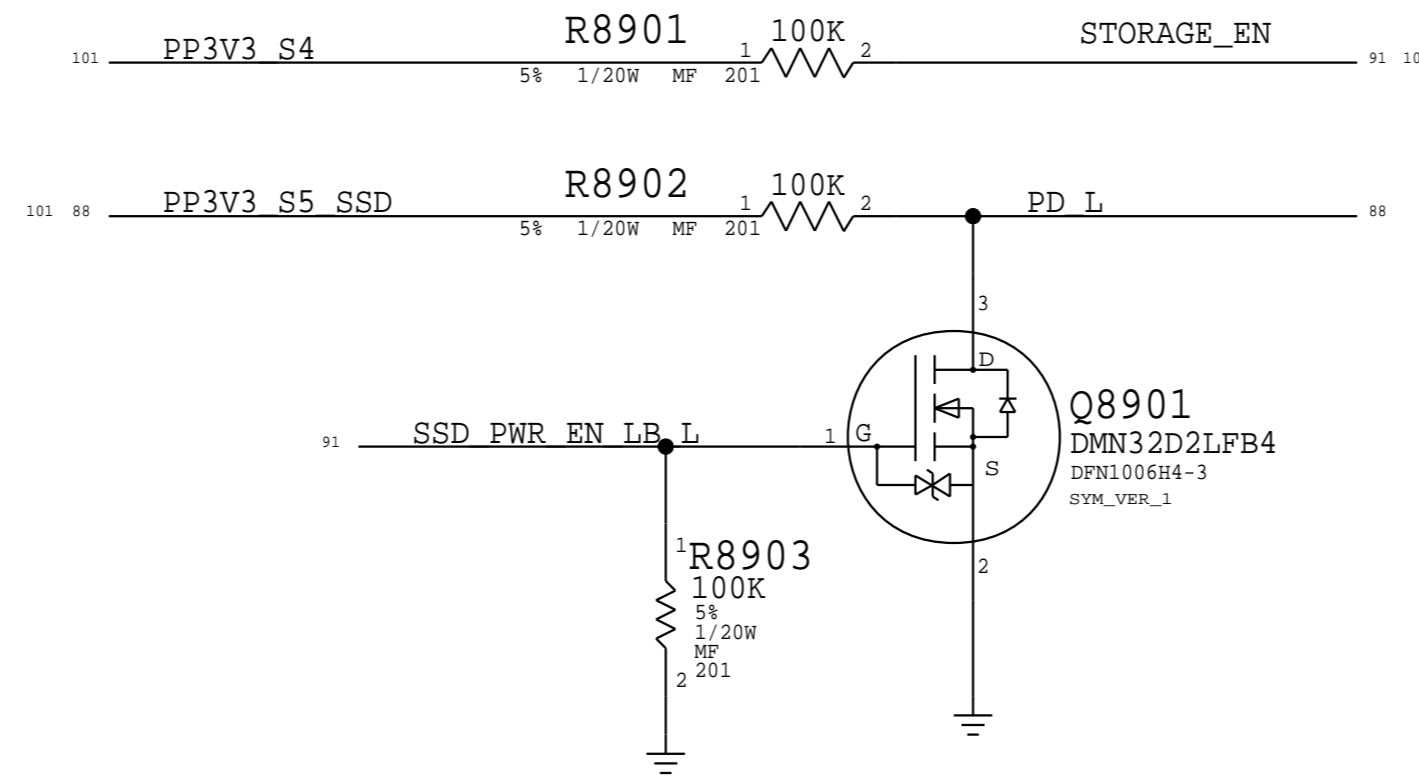
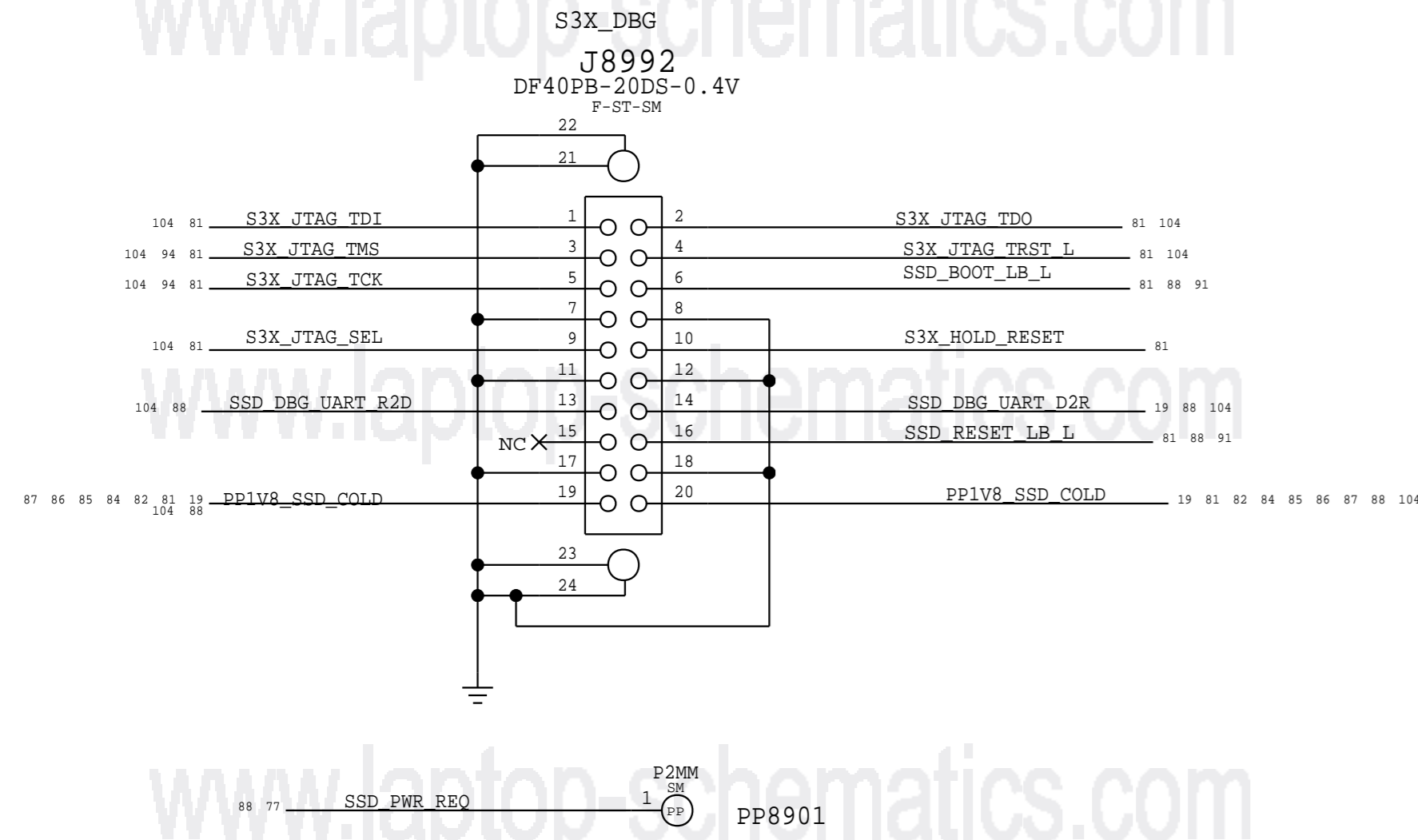
VSS P13
 VSS P15
 VSS P17
 VSS P19
 VSS P21
 VSS P23
 VSS P27
 VSS R3
 VSS R5
 VSS R8
 VSS R10
 VSS R12
 VSS R14
 VSS R16
 VSS R18
 VSS R20
 VSS R22
 VSS R26
 VSS R28
 VSS T3
 VSS T4
 VSS T7
 VSS T9
 VSS T11
 VSS T13
 VSS T15
 VSS T17
 VSS T19
 VSS T21
 VSS T23
 VSS T24
 VSS T27
 VSS T28
 VSS U5
 VSS U8
 VSS U10
 VSS U12
 VSS U14
 VSS U16
 VSS U18
 VSS U20
 VSS U22
 VSS U26
 VSS V3
 VSS V4
 VSS V9
 VSS V11
 VSS V13

NC S3X VSS_S 103

BOM_COST_GROUP=SSD

| | | | | | | | | | | | | | | | |
|---------------------------------|--|---|--|---|--|--------------------------------|--|--|--|-------------------------|--|-----------|--|-----------|--|
| SYNC_MASTER=J79_RIO | | PAGE TITLE | | PAGE_TITLE=S3X_GND | | DRAWING NUMBER | | 051-00777 | | STEP | | D | | | |
| Apple Inc. | | REVISION | | 9.0.0 | | BRANCH | | dvt-fab09-0 | | PAGE | | 88 OF 145 | | | |
| NOTICE OF PROPRIETARY PROPERTY: | | THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | 11 NOT TO REPRODUCE OR COPY IT | | 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | 11V ALL RIGHTS RESERVED | | SHEET | | 83 OF 119 | |

JTAG (DEBUG 1)

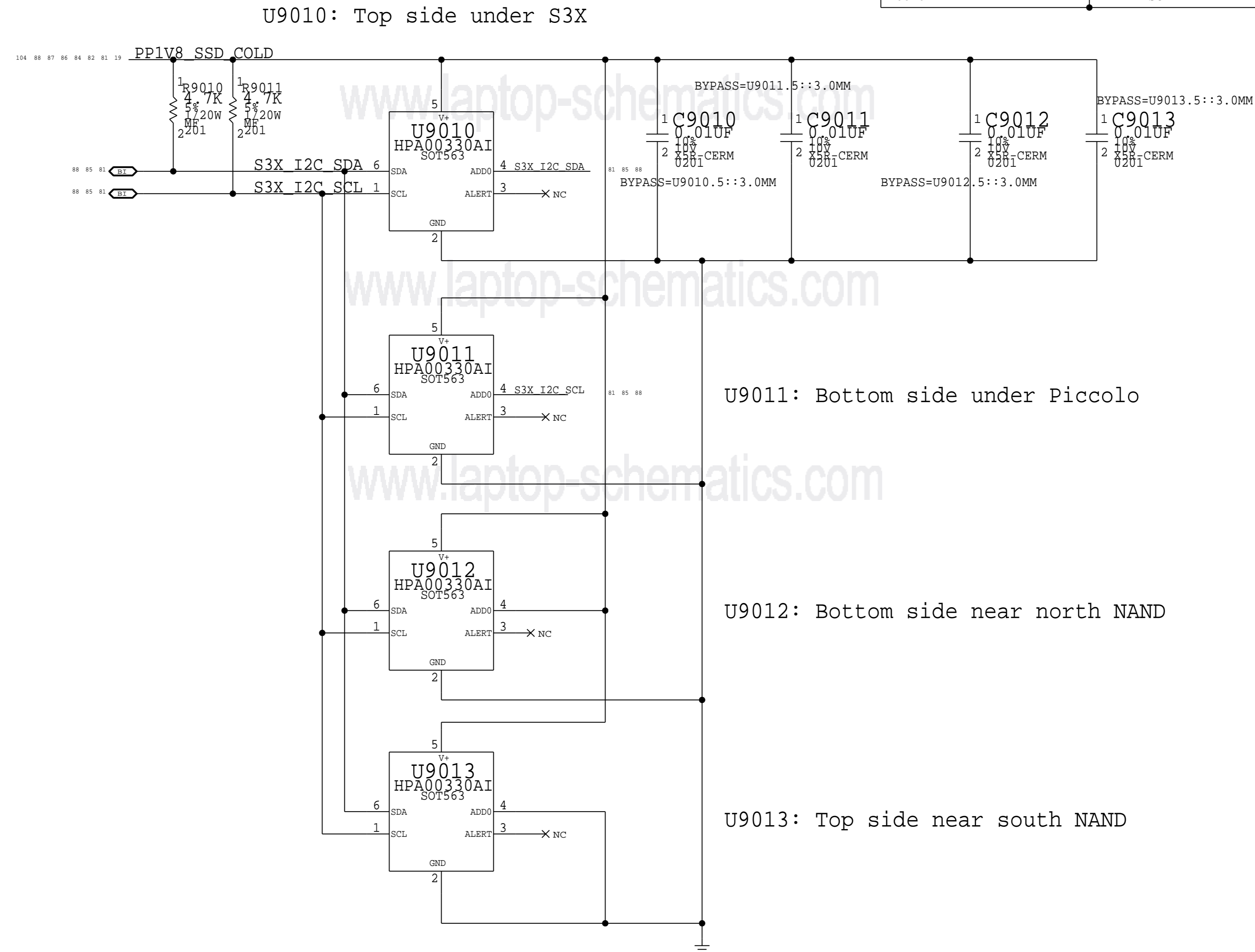


| | | | | | |
|--------|------------------------|-------|--------|---------------|----------------------|
| 91 | PCIE_SSD_R2D_LB_C_P<0> | C8910 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_LB_P<0> |
| 91 | PCIE_SSD_R2D_LB_C_N<0> | C8911 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_LB_N<0> |
| 105 15 | PCIE_SSD_R2D_C_P<1> | C8913 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_P<1> |
| 105 15 | PCIE_SSD_R2D_C_N<1> | C8912 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_N<1> |
| 105 15 | PCIE_SSD_R2D_C_P<2> | C8914 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_P<2> |
| 105 15 | PCIE_SSD_R2D_C_N<2> | C8915 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_N<2> |
| 105 15 | PCIE_SSD_R2D_C_P<3> | C8917 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_P<3> |
| 105 15 | PCIE_SSD_R2D_C_N<3> | C8916 | 0.22UF | GND_VOID=TRUE | PCIE_SSD_R2D_N<3> |

| | | | |
|---|----------------|-----------|-------------|
| PAGE TITLE | | Connector | |
| Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 89 OF 145 |
| | | SHEET | 84 OF 119 |

BOM_COST_GROUP=SSD

| DEVICE | 2-WIRE ADDRESS | ADD0 | PIN CONNECTION |
|---------|----------------|------|----------------|
| 1001000 | | | GND |
| 1001001 | | | V+ |
| 1001010 | | | SDA |
| 1001011 | | | SCL |



BOM_COST_GROUP=SSD

| | | | | |
|---|--|----------------|--|-------------|
| PAGE TITLE | | DRAWING NUMBER | | SIZE |
| NAND VR, I2C ROM, TEMP SENSORS | | 051-00777 | | D |
| Apple Inc. | | REVISION | | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | | dvt-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | | 90 OF 145 |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | SHEET | | 85 OF 119 |
| II NOT TO REPRODUCE OR COPY IT | | | | |
| III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | | | |
| IV ALL RIGHTS RESERVED | | | | |

D

C

B

A

D

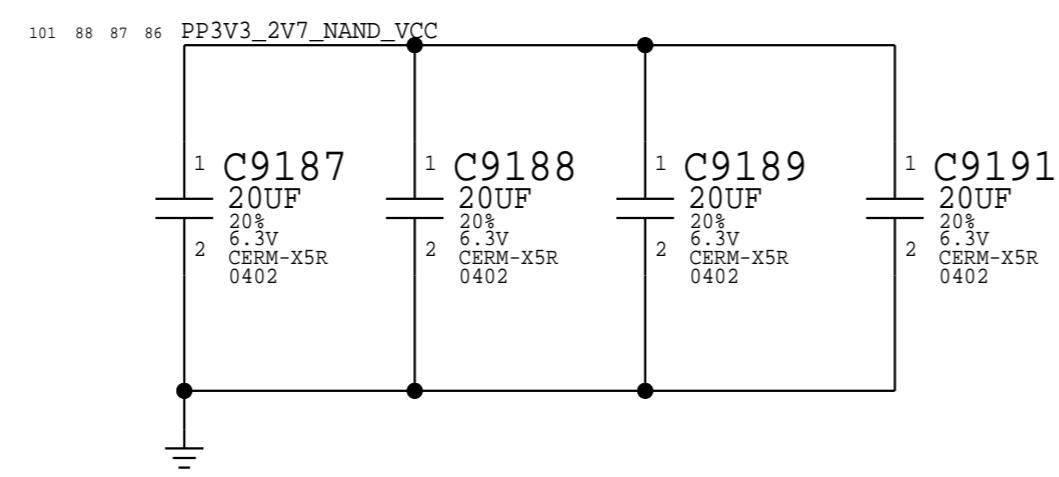
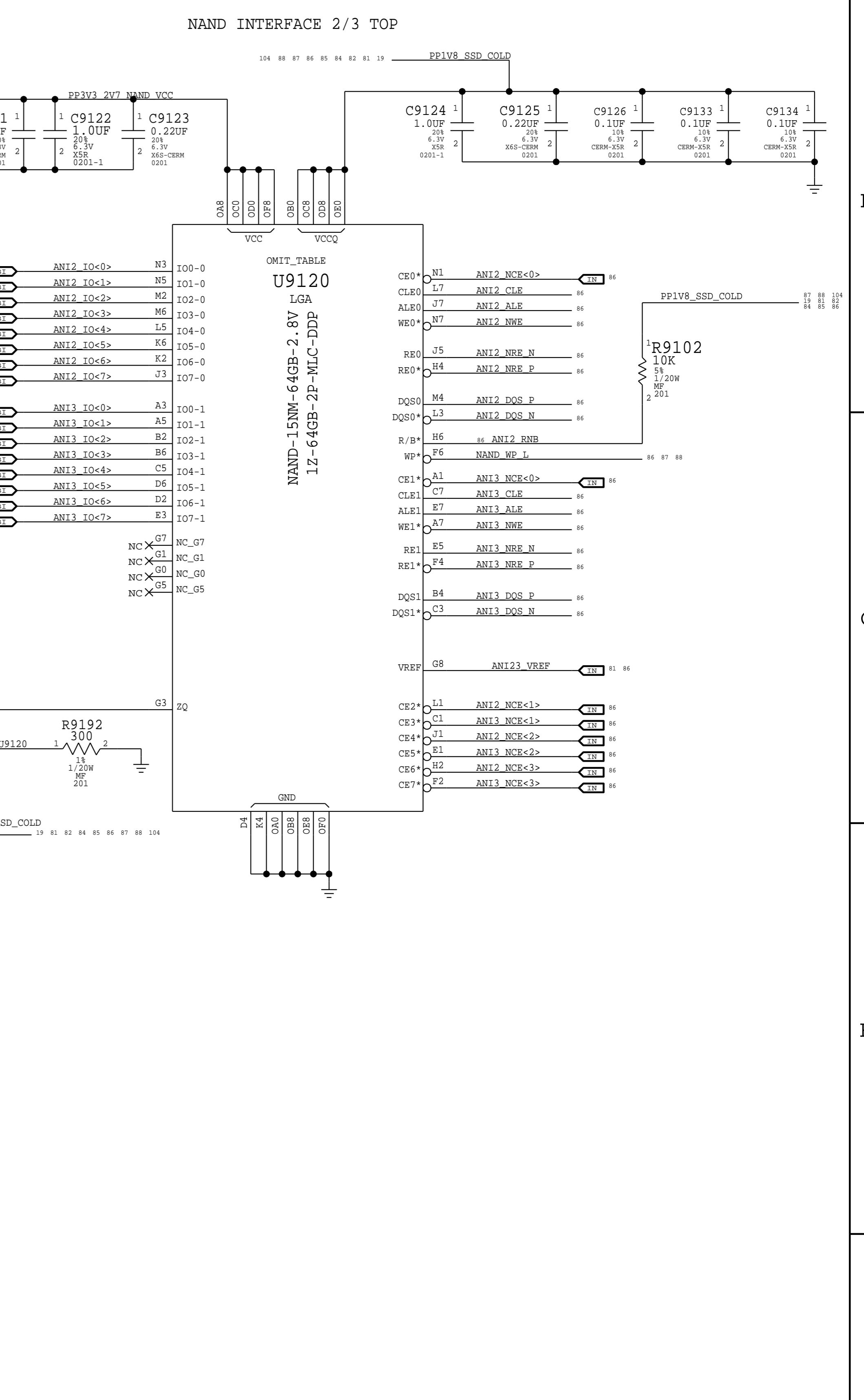
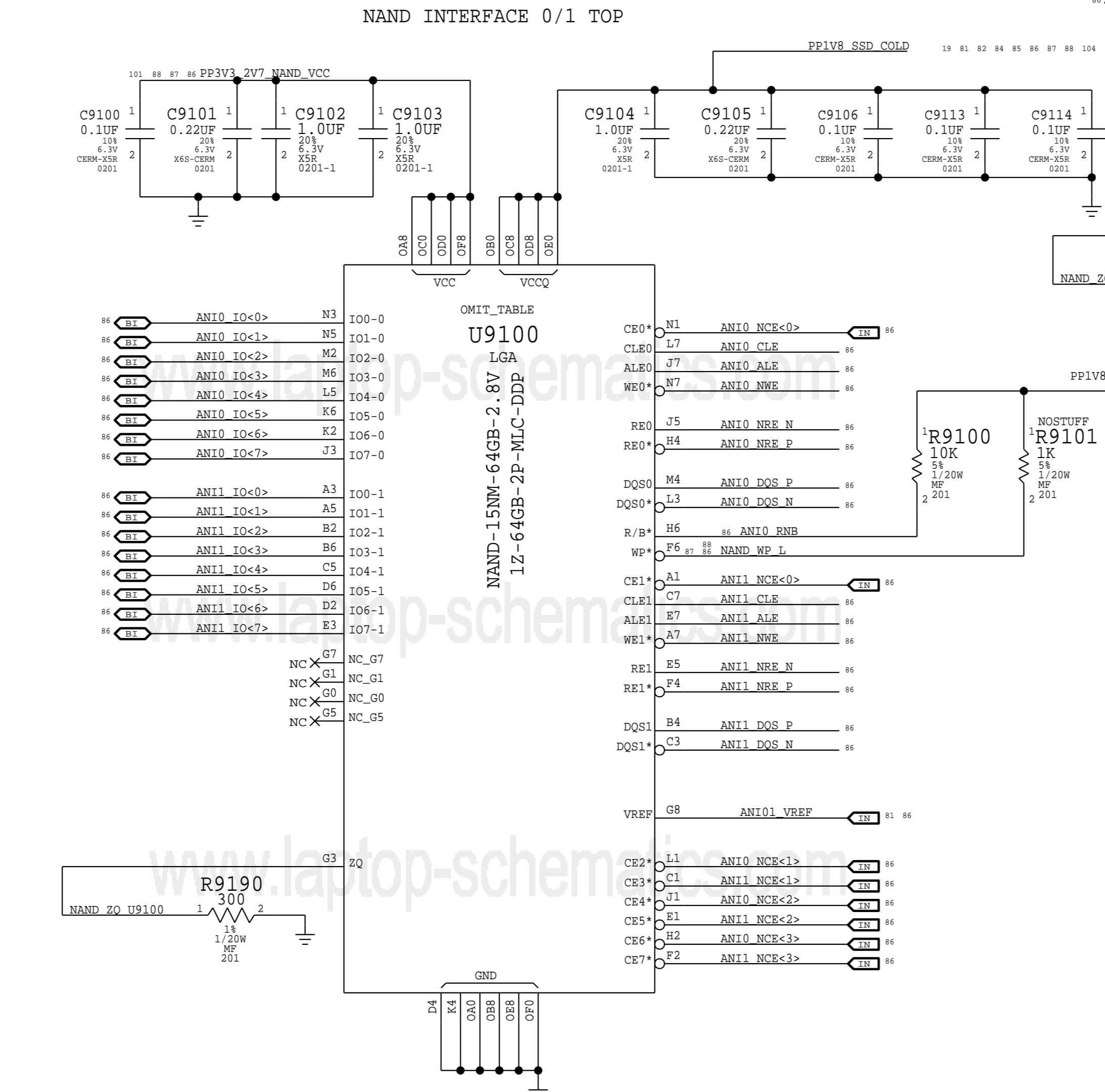
C

B

A

OMIT_TABLE

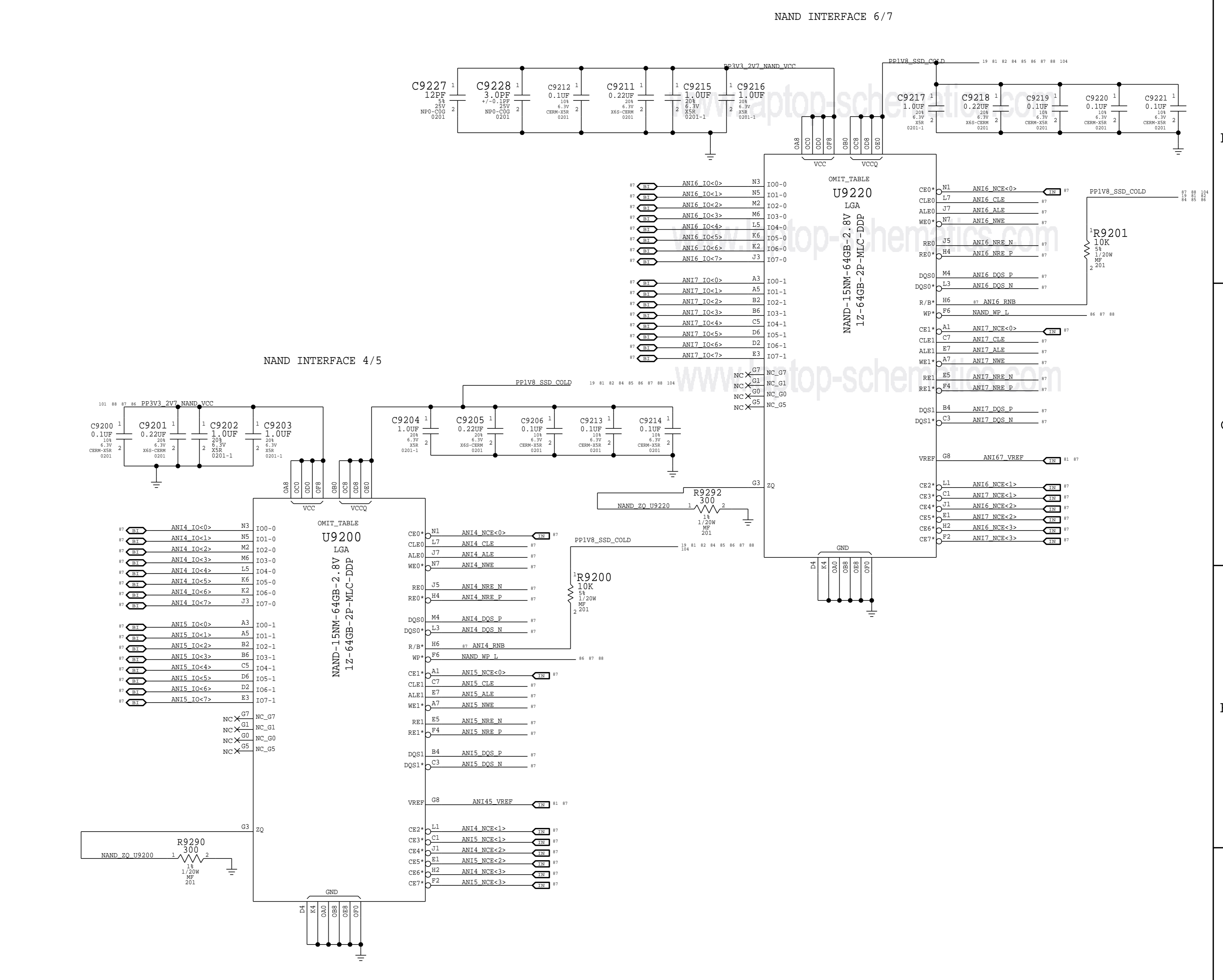
| | | | | | |
|------|--------------|------------|--------------|------|--------------|
| AC29 | ANI0_I00 | U8600 | ANI1_I00 | T29 | ANI1_I0<0> |
| AD30 | ANI0_I0<1> | S3X | ANI1_I01 | U30 | ANI1_I0<1> |
| AD29 | ANI0_I0<2> | BGA-HIP35 | ANI1_I02 | U29 | ANI1_I0<2> |
| AD28 | ANI0_I0<3> | SYM 1 OF 7 | ANI1_I03 | U28 | ANI1_I0<3> |
| AG30 | ANI0_I0<4> | | ANI1_I04 | Y30 | ANI1_I0<4> |
| AG29 | ANI0_I0<5> | | ANI1_I05 | Y29 | ANI1_I0<5> |
| AH30 | ANI0_I0<6> | | ANI1_I06 | AA30 | ANI1_I0<6> |
| AH29 | ANI0_I0<7> | | ANI1_I07 | AA29 | ANI1_I0<7> |
| AG22 | ANI0_NCE<0> | | ANI1_NCE(0) | AJ24 | ANI1_NCE<0> |
| AD23 | ANI0_NCE<1> | | ANI1_NCE(1) | AG26 | ANI1_NCE<1> |
| AF21 | ANI0_NCE<2> | | ANI1_NCE(2) | AH26 | ANI1_NCE<2> |
| AD22 | ANI0_NCE<3> | | ANI1_NCE(3) | AF24 | ANI1_NCE<3> |
| AF22 | NC ANI0_NCE4 | | ANI1_NCE(4) | AF26 | NC ANI1_NCE4 |
| AF23 | NC ANI0_NCE5 | | ANI1_NCE(5) | AK24 | NC ANI1_NCE5 |
| AJ20 | NC ANI0_NCE6 | | ANI1_NCE(6) | AE24 | NC ANI1_NCE6 |
| AK20 | NC ANI0_NCE7 | | ANI1_NCE(7) | AH24 | NC ANI1_NCE7 |
| AH23 | ANI0_ALE | | ANI1_ALE | AK26 | ANI1_ALE |
| AH22 | ANI0_CLE | | ANI1_CLE | AG24 | ANI1_CLE |
| AH28 | ANI0_NWE | | ANI1_NWE | AA28 | ANI1_NWE |
| AJ22 | ANI0_RNB | | ANI1_RNB | AJ26 | NC ANI1_RNB |
| AH22 | ANI0_PPM_IN | | ANI1_PPM_IN | AF25 | NC |
| AH21 | ANI0_PPM_OUT | | ANI1_PPM_OUT | AH25 | NC |
| AF30 | ANI0_NRE_P | | ANI1_NRE_P | W30 | ANI1_NRE_P |
| AF29 | ANI0_NRE_N | | ANI1_NRE_N | W29 | ANI1_NRE_N |
| AE30 | ANI0_DQS_P | | ANI1_DQS_P | V30 | ANI1_DQS_P |
| AE29 | ANI0_DQS_N | | ANI1_DQS_N | V29 | ANI1_DQS_N |
| AC30 | ANI0_VREF | | ANI1_VREF | T30 | ANI01_VREF |
| H29 | ANI2_I00 | | ANI3_I00 | R29 | ANI3_I0<0> |
| G28 | ANI2_I0<1> | | ANI3_I01 | F28 | ANI3_I0<1> |
| G29 | ANI2_I0<2> | | ANI3_I02 | F29 | ANI3_I0<2> |
| G30 | ANI2_I0<3> | | ANI3_I03 | F30 | ANI3_I0<3> |
| D29 | ANI2_I0<4> | | ANI3_I04 | L29 | ANI3_I0<4> |
| D30 | ANI2_I0<5> | | ANI3_I05 | L30 | ANI3_I0<5> |
| C29 | ANI2_I0<6> | | ANI3_I06 | K29 | ANI3_I0<6> |
| C30 | ANI2_I0<7> | | ANI3_I07 | K30 | ANI3_I0<7> |
| B22 | ANI2_NCE<0> | | ANI3_NCE(0) | A26 | ANI3_NCE<0> |
| C19 | ANI2_NCE<1> | | ANI3_NCE(1) | D24 | ANI3_NCE<1> |
| D22 | ANI2_NCE<2> | | ANI3_NCE(2) | A24 | ANI3_NCE<2> |
| E22 | ANI2_NCE<3> | | ANI3_NCE(3) | D25 | ANI3_NCE<3> |
| F21 | NC ANI2_NCE4 | | ANI3_NCE(4) | D23 | NC ANI3_NCE4 |
| D19 | NC ANI2_NCE5 | | ANI3_NCE(5) | E24 | NC ANI3_NCE5 |
| D21 | NC ANI2_NCE6 | | ANI3_NCE(6) | D26 | NC ANI3_NCE6 |
| E21 | NC ANI2_NCE7 | | ANI3_NCE(7) | B25 | NC ANI3_NCE7 |
| E20 | ANI2_ALE | | ANI3_ALE | E25 | ANI3_ALE |
| A22 | ANI2_CLE | | ANI3_CLE | E26 | ANI3_CLE |
| C28 | ANI2_NWE | | ANI3_NWE | K28 | ANI3_NWE |
| D20 | ANI2_RNB | | ANI3_RNB | B24 | NC ANI3_RNB |
| F23 | ANI2_PPM_IN | | ANI3_PPM_IN | F23 | NC |
| E23 | ANI2_PPM_OUT | | ANI3_PPM_OUT | E23 | NC |
| E29 | ANI2_NRE_P | | ANI3_NRE_P | M29 | ANI3_NRE_P |
| E30 | ANI2_NRE_N | | ANI3_NRE_N | M30 | ANI3_NRE_N |
| F29 | ANI2_DQS_P | | ANI3_DQS_P | N29 | ANI3_DQS_P |
| F30 | ANI2_DQS_N | | ANI3_DQS_N | N30 | ANI3_DQS_N |
| H30 | ANI23_VREF | | ANI3_VREF | R30 | ANI23_VREF |



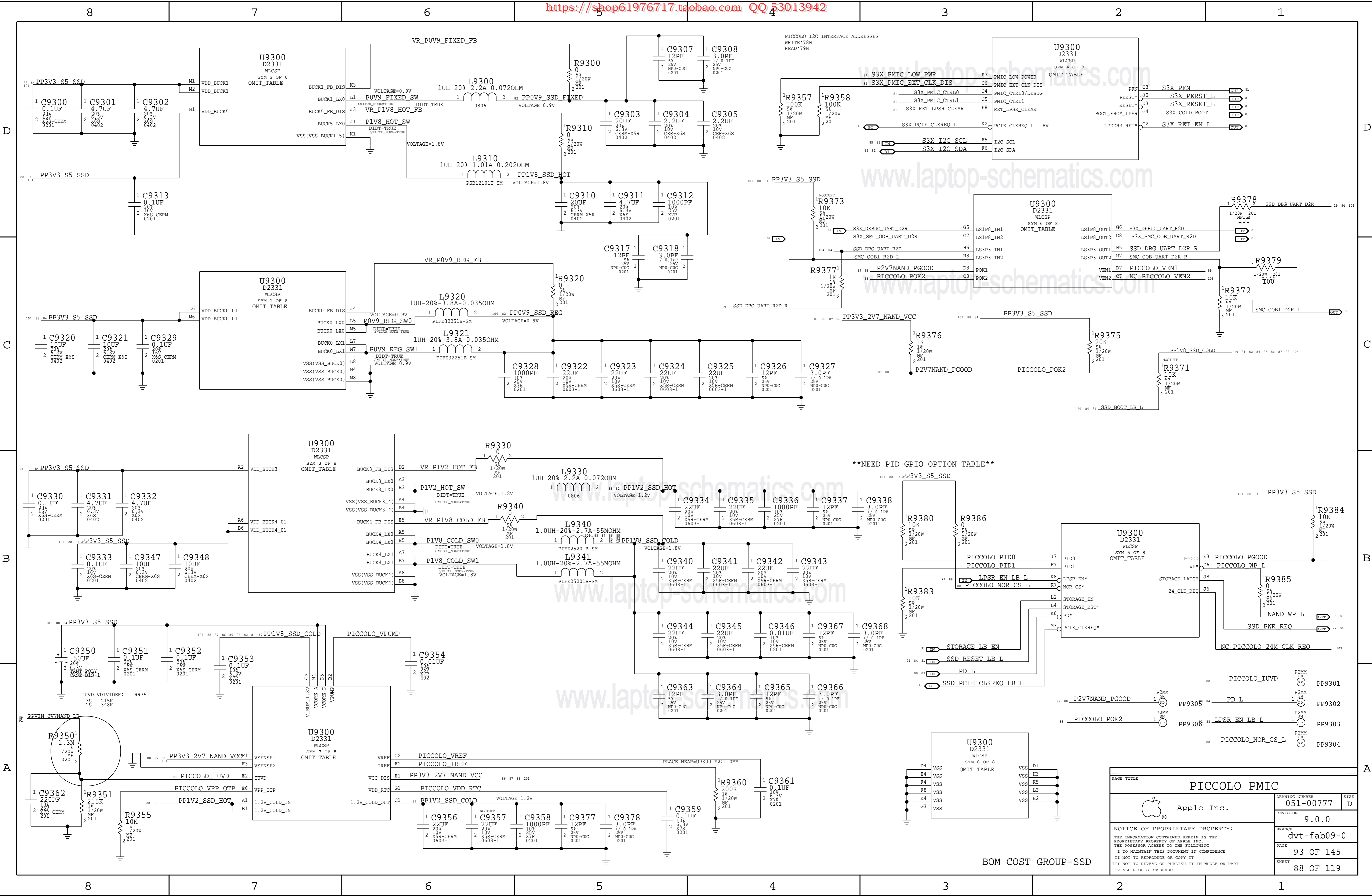
| | | | |
|---|--|----------------|-------------|
| PAGE TITLE | | ANI[3:0] | |
| Apple Inc. | | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | 91 OF 145 |
| 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | SHEET | 86 OF 119 |
| 11 NOT TO REPRODUCE OR COPY IT | | | |
| 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | | |
| 11V ALL RIGHTS RESERVED | | | |

BOM_COST_GROUP=SSD

| OMIT_TABLE | | U8600 | |
|------------|--------------|-------|--------------|
| IN | ANI4_IO<0> | H2 | ANI4_I00 |
| IN | ANI4_IO<1> | G3 | ANI4_I01 |
| IN | ANI4_IO<2> | G2 | ANI4_I02 |
| IN | ANI4_IO<3> | G1 | ANI4_I03 |
| IN | ANI4_IO<4> | D2 | ANI4_I04 |
| IN | ANI4_IO<5> | D1 | ANI4_I05 |
| IN | ANI4_IO<6> | C2 | ANI4_I06 |
| IN | ANI4_IO<7> | C1 | ANI4_I07 |
| OUT | ANI4_NCE<0> | G6 | ANI4_NCE(0) |
| OUT | ANI4_NCE<1> | E7 | ANI4_NCE(1) |
| OUT | ANI4_NCE<2> | E6 | ANI4_NCE(2) |
| OUT | ANI4_NCE<3> | G7 | ANI4_NCE(3) |
| OUT | NC ANI4_NCE4 | D8 | ANI4_NCE(4) |
| OUT | NC ANI4_NCE5 | A6 | ANI4_NCE(5) |
| OUT | NC ANI4_NCE6 | H9 | ANI4_NCE(6) |
| OUT | NC ANI4_NCE7 | G8 | ANI4_NCE(7) |
| IN | ANI4_ALE | D7 | ANI4_ALE |
| IN | ANI4_CLE | F6 | ANI5_CLE |
| IN | ANI4_NWE | C3 | ANI4_NWE |
| IN | ANI4_RNB | D6 | ANI4_RNB |
| NC | ANI4_PPM_IN | B6 | ANI4_PPM_IN |
| NC | ANI4_PPM_OUT | C6 | ANI4_PPM_OUT |
| OUT | ANI4_NRE_P | E2 | ANI4_NRE_P |
| OUT | ANI4_NRE_N | E1 | ANI4_NRE_N |
| OUT | ANI4_DQS_P | F2 | ANI4_DQS_P |
| OUT | ANI4_DQS_N | F1 | ANI4_DQS_N |
| OUT | ANI45_VREF | H1 | ANI45_VREF |
| IN | ANI6_IO<0> | AC2 | ANI6_I00 |
| IN | ANI6_IO<1> | AD1 | ANI6_I01 |
| IN | ANI6_IO<2> | AD2 | ANI6_I02 |
| IN | ANI6_IO<3> | AD3 | ANI6_I03 |
| IN | ANI6_IO<4> | AG1 | ANI6_I04 |
| IN | ANI6_IO<5> | AG2 | ANI6_I05 |
| IN | ANI6_IO<6> | AH1 | ANI6_I06 |
| IN | ANI6_IO<7> | AH2 | ANI6_I07 |
| OUT | ANI6_NCE<0> | AK11 | ANI6_NCE(0) |
| OUT | ANI6_NCE<1> | AJ11 | ANI6_NCE(1) |
| OUT | ANI6_NCE<2> | AH10 | ANI6_NCE(2) |
| OUT | ANI6_NCE<3> | AH9 | ANI6_NCE(3) |
| OUT | NC ANI6_NCE4 | AH12 | ANI6_NCE(4) |
| OUT | NC ANI6_NCE5 | AH11 | ANI6_NCE(5) |
| OUT | NC ANI6_NCE6 | AG9 | ANI6_NCE(6) |
| OUT | NC ANI6_NCE7 | AG11 | ANI6_NCE(7) |
| IN | ANI6_ALE | AJ9 | ANI6_ALE |
| IN | ANI6_CLE | AK9 | ANI6_CLE |
| IN | ANI6_NWE | AH3 | ANI6_NWE |
| IN | ANI6_RNB | AG12 | ANI6_RNB |
| NC | ANI6_PPM_IN | AG10 | ANI6_PPM_IN |
| NC | ANI6_PPM_OUT | AE10 | ANI6_PPM_OUT |
| OUT | ANI6_NRE_P | AF1 | ANI6_NRE_P |
| OUT | ANI6_NRE_N | AF2 | ANI6_NRE_N |
| OUT | ANI6_DQS_P | AE1 | ANI6_DQS_P |
| OUT | ANI6_DQS_N | AE2 | ANI6_DQS_N |
| OUT | ANI67_VREF | AC1 | ANI67_VREF |
| IN | ANI7_IO<0> | R2 | ANI7_I00 |
| IN | ANI7_IO<1> | P3 | ANI7_I01 |
| IN | ANI7_IO<2> | P2 | ANI7_I02 |
| IN | ANI7_IO<3> | P1 | ANI7_I03 |
| IN | ANI7_IO<4> | L2 | ANI7_I04 |
| IN | ANI7_IO<5> | L1 | ANI7_I05 |
| IN | ANI7_IO<6> | K2 | ANI7_I06 |
| IN | ANI7_IO<7> | K1 | ANI7_I07 |
| OUT | ANI7_NCE<0> | B3 | ANI7_NCE(0) |
| OUT | ANI7_NCE<1> | D4 | ANI7_NCE(1) |
| OUT | ANI7_NCE<2> | E4 | ANI7_NCE(2) |
| OUT | ANI7_NCE<3> | B4 | ANI7_NCE(3) |
| OUT | NC ANI7_NCE4 | A4 | ANI7_NCE(4) |
| OUT | NC ANI7_NCE5 | D5 | ANI7_NCE(5) |
| OUT | NC ANI7_NCE6 | B5 | ANI7_NCE(6) |
| OUT | NC ANI7_NCE7 | A5 | ANI7_NCE(7) |
| IN | ANI7_ALE | F4 | ANI7_ALE |
| IN | ANI7_CLE | A3 | ANI7_CLE |
| IN | ANI7_NWE | K3 | ANI7_NWE |
| IN | ANI7_RNB | C4 | ANI7_RNB |
| NC | ANI7_PPM_IN | G5 | ANI7_PPM_IN |
| NC | ANI7_PPM_OUT | E5 | ANI7_PPM_OUT |
| OUT | ANI7_NRE_P | M2 | ANI7_NRE_P |
| OUT | ANI7_NRE_N | M1 | ANI7_NRE_N |
| OUT | ANI7_DQS_P | N2 | ANI7_DQS_P |
| OUT | ANI7_DQS_N | N1 | ANI7_DQS_N |
| OUT | ANI75_VREF | R1 | ANI75_VREF |
| IN | ANI7_IO<0> | T2 | ANI7_I00 |
| IN | ANI7_IO<1> | U1 | ANI7_I01 |
| IN | ANI7_IO<2> | U2 | ANI7_I02 |
| IN | ANI7_IO<3> | U3 | ANI7_I03 |
| IN | ANI7_IO<4> | Y1 | ANI7_I04 |
| IN | ANI7_IO<5> | Y2 | ANI7_I05 |
| IN | ANI7_IO<6> | AA1 | ANI7_I06 |
| IN | ANI7_IO<7> | AA2 | ANI7_I07 |
| OUT | ANI7_NCE<0> | AK5 | ANI7_NCE(0) |
| OUT | ANI7_NCE<1> | AK7 | ANI7_NCE(1) |
| OUT | ANI7_NCE<2> | AJ7 | ANI7_NCE(2) |
| OUT | ANI7_NCE<3> | AJ5 | ANI7_NCE(3) |
| OUT | NC ANI7_NCE4 | AH5 | ANI7_NCE(4) |
| OUT | NC ANI7_NCE5 | AH7 | ANI7_NCE(5) |
| OUT | NC ANI7_NCE6 | AG7 | ANI7_NCE(6) |
| OUT | NC ANI7_NCE7 | AG5 | ANI7_NCE(7) |
| IN | ANI7_ALE | AG6 | ANI7_ALE |
| IN | ANI7_CLE | AH6 | ANI7_CLE |
| IN | ANI7_NWE | AA3 | ANI7_NWE |
| IN | ANI7_RNB | AF6 | ANI7_RNB |
| NC | ANI7_PPM_IN | AG8 | ANI7_PPM_IN |
| NC | ANI7_PPM_OUT | AH8 | ANI7_PPM_OUT |
| OUT | ANI7_NRE_P | W1 | ANI7_NRE_P |
| OUT | ANI7_NRE_N | W2 | ANI7_NRE_N |
| OUT | ANI7_DQS_P | V1 | ANI7_DQS_P |
| OUT | ANI7_DQS_N | V2 | ANI7_DQS_N |
| OUT | ANI67_VREF | T1 | ANI67_VREF |

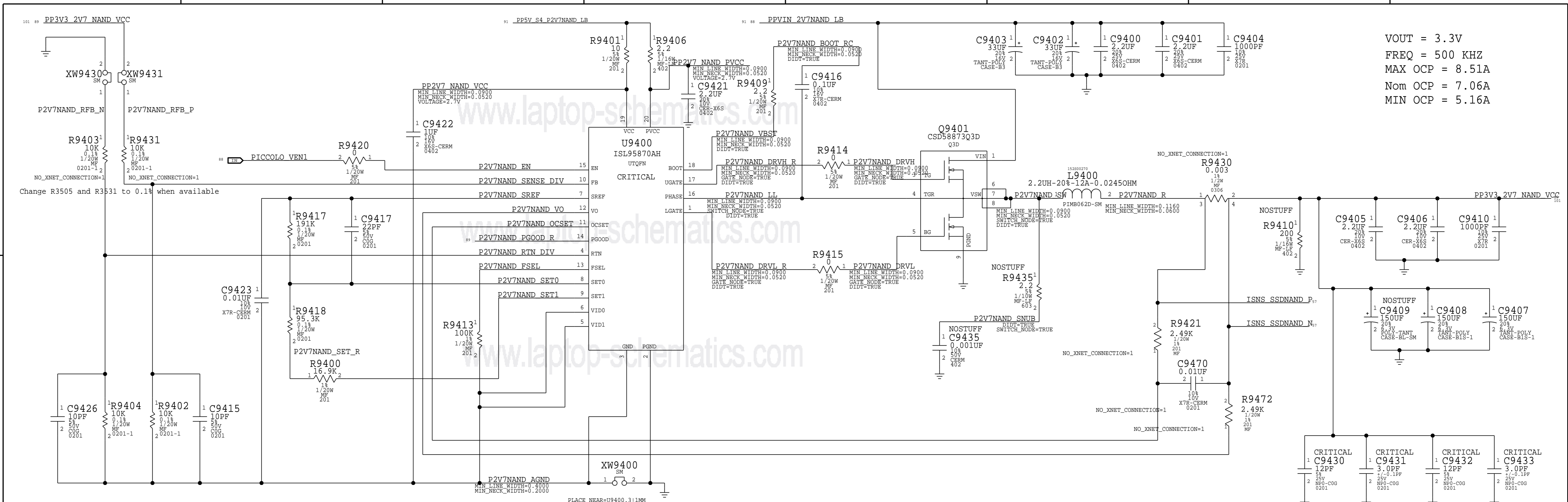


| | | | |
|---|--|--------------------|-------------|
| PAGE TITLE | | ANI[7:4] | |
| Apple Inc. | | DRAWING NUMBER | 051-00777 |
| NOTICE OF PROPRIETARY PROPERTY: | | REVISION | 9.0.0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | BRANCH | dvt-fab09-0 |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | PAGE | 92 OF 145 |
| I WILL NOT REPRODUCE OR PUBLISH IT IN WHOLE OR PART | | SHEET | 87 OF 119 |
| I WILL NOT REPRODUCE OR PUBLISH IT IN WHOLE OR PART | | BOM_COST_GROUP=SSD | |

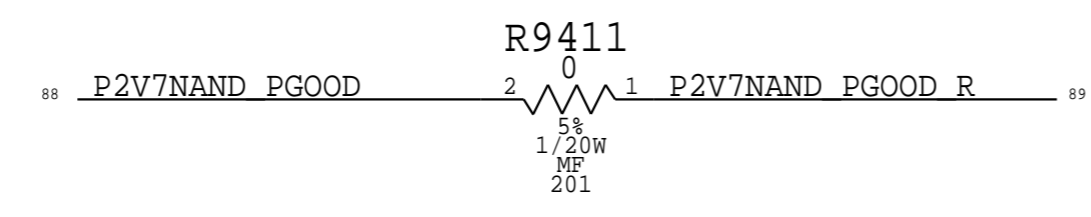


| | | | | |
|---|--|----------------|--|-----|
| PAGE TITLE | | DRAWING NUMBER | | STR |
| PICCOLO PMIC | | 051-00777 | | D |
| Apple Inc. | | REVISION | | |
| | | 9.0.0 | | |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | | |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | dvt-fab09-0 | | |
| 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | PAGE | | |
| 11 NOT TO REPRODUCE OR COPY IT | | 93 OF 145 | | |
| 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | SHEET | | |
| 112 ALL RIGHTS RESERVED | | 88 OF 119 | | |

BOM_COST_GROUP=SSD



VOUT = 3.3V
 FREQ = 500 KHZ
 MAX OCP = 8.51A
 Nom OCP = 7.06A
 MIN OCP = 5.16A



| | | | | |
|---|--|--------------------|-------------|-----|
| PAGE TITLE | | | SSD NAND VR | |
| | | DRAWING NUMBER | 051-00777 | STR |
| | | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 | |
| | | PAGE | 94 OF 145 | |
| | | SHEET | 89 OF 119 | |
| | | BOM_COST_GROUP=SSD | | |

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6


5

4

3

2

1

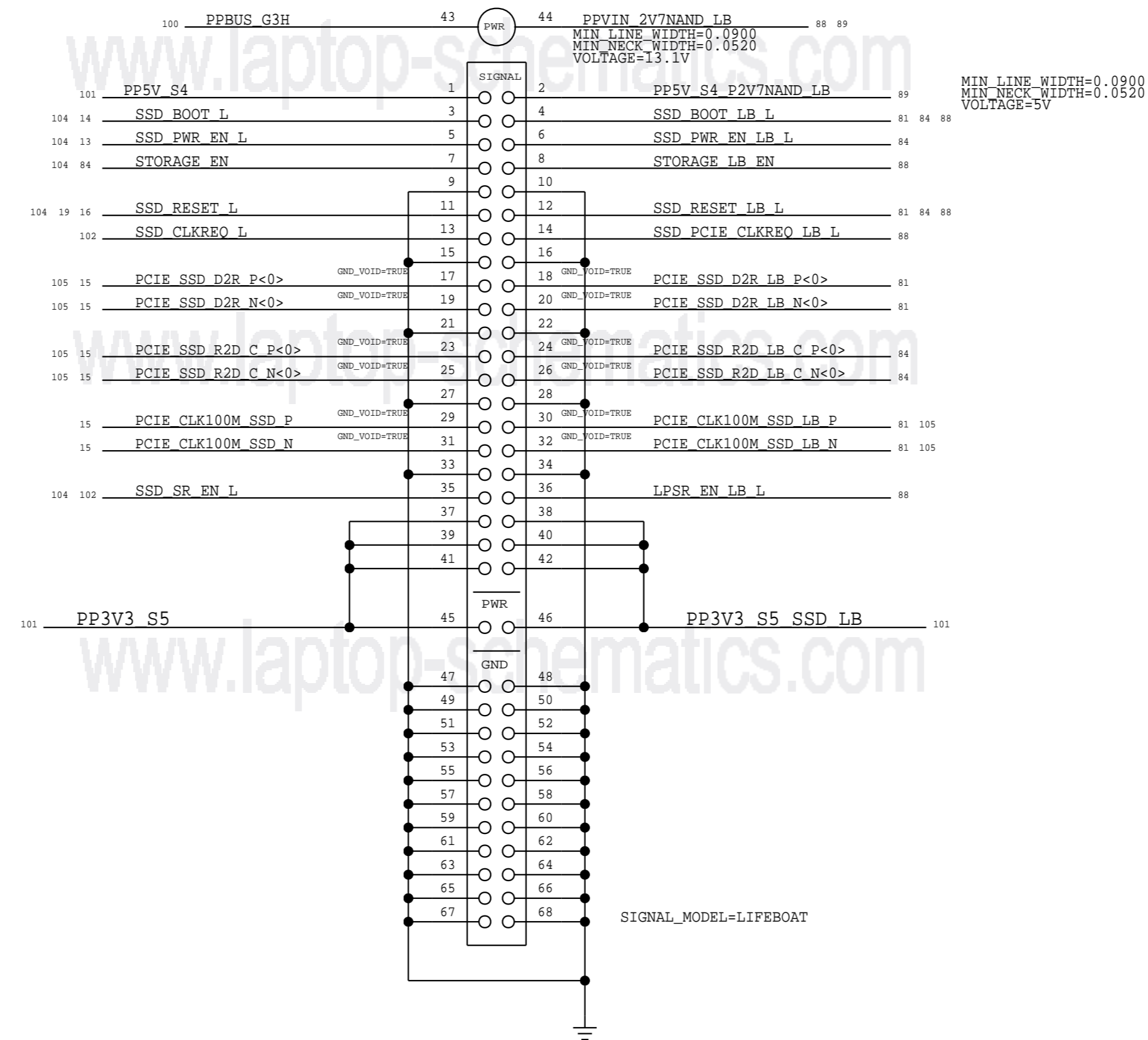
| | | | |
|---|----------------|----------------------|------|
| SYNC_MASTER=J14 | | SYNC_DATE=10/23/2012 | |
| PAGE TITLE | | | |
| Empty | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 95 OF 145 | |
| | SHEET | 90 OF 119 | |

LIFEBOAT

J9600
20759-042E-02
P-ST-SM

PCH Side

SSD Side

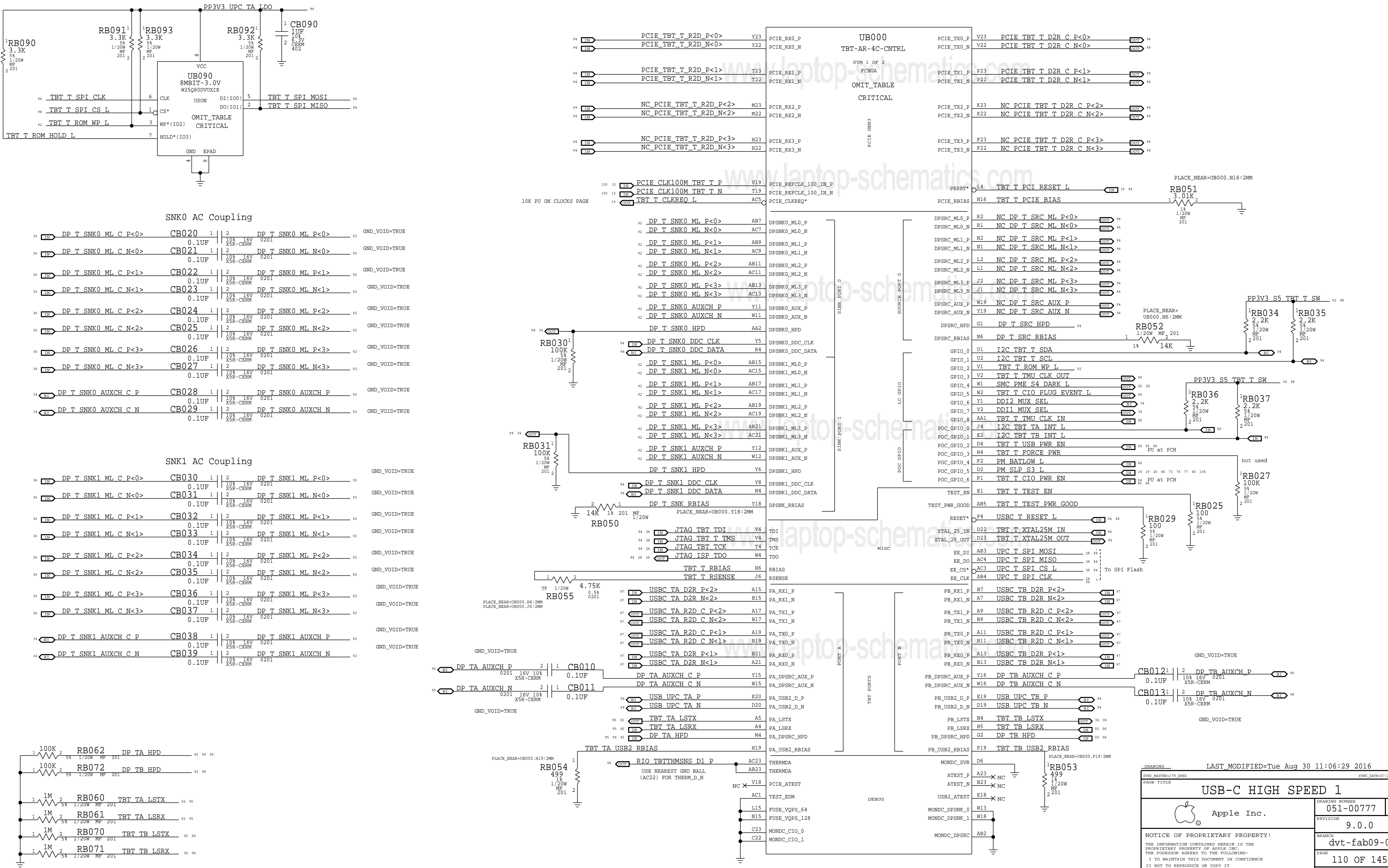


MIN LINE WIDTH=0.0900
MIN NECK WIDTH=0.0520
VOLTAGE=5V

SIGNAL_MODEL=LIFEBOAT

BOM_COST_GROUP=SSD

| | | | |
|--|----------------|----------------------|-------------|
| SYNC_MASTER=j79_RUENJOU | | SYNC_DATE=09/09/2015 | |
| PAGE TITLE | | | |
| LIFEBOAT | | | |
| | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 96 OF 145 |
| | | SHEET | 91 OF 119 |



SNK0 AC Coupling

| | | | | | |
|---------------------|-------|---|---|-------------------|---------------|
| DP T SNK0 ML C P<0> | CB020 | 1 | 2 | DP T SNK0 ML P<0> | GND_VOID=TRUE |
| DP T SNK0 ML C N<0> | CB021 | 1 | 2 | DP T SNK0 ML N<0> | GND_VOID=TRUE |
| DP T SNK0 ML C P<1> | CB022 | 1 | 2 | DP T SNK0 ML P<1> | GND_VOID=TRUE |
| DP T SNK0 ML C N<1> | CB023 | 1 | 2 | DP T SNK0 ML N<1> | GND_VOID=TRUE |
| DP T SNK0 ML C P<2> | CB024 | 1 | 2 | DP T SNK0 ML P<2> | GND_VOID=TRUE |
| DP T SNK0 ML C N<2> | CB025 | 1 | 2 | DP T SNK0 ML N<2> | GND_VOID=TRUE |
| DP T SNK0 ML C P<3> | CB026 | 1 | 2 | DP T SNK0 ML P<3> | GND_VOID=TRUE |
| DP T SNK0 ML C N<3> | CB027 | 1 | 2 | DP T SNK0 ML N<3> | GND_VOID=TRUE |
| DP T SNK0 AUXCH C P | CB028 | 1 | 2 | DP T SNK0 AUXCH P | GND_VOID=TRUE |
| DP T SNK0 AUXCH C N | CB029 | 1 | 2 | DP T SNK0 AUXCH N | GND_VOID=TRUE |

SNK1 AC Coupling

| | | | | | |
|---------------------|-------|---|---|-------------------|---------------|
| DP T SNK1 ML C P<0> | CB030 | 1 | 2 | DP T SNK1 ML P<0> | GND_VOID=TRUE |
| DP T SNK1 ML C N<0> | CB031 | 1 | 2 | DP T SNK1 ML N<0> | GND_VOID=TRUE |
| DP T SNK1 ML C P<1> | CB032 | 1 | 2 | DP T SNK1 ML P<1> | GND_VOID=TRUE |
| DP T SNK1 ML C N<1> | CB033 | 1 | 2 | DP T SNK1 ML N<1> | GND_VOID=TRUE |
| DP T SNK1 ML C P<2> | CB034 | 1 | 2 | DP T SNK1 ML P<2> | GND_VOID=TRUE |
| DP T SNK1 ML C N<2> | CB035 | 1 | 2 | DP T SNK1 ML N<2> | GND_VOID=TRUE |
| DP T SNK1 ML C P<3> | CB036 | 1 | 2 | DP T SNK1 ML P<3> | GND_VOID=TRUE |
| DP T SNK1 ML C N<3> | CB037 | 1 | 2 | DP T SNK1 ML N<3> | GND_VOID=TRUE |
| DP T SNK1 AUXCH C P | CB038 | 1 | 2 | DP T SNK1 AUXCH P | GND_VOID=TRUE |
| DP T SNK1 AUXCH C N | CB039 | 1 | 2 | DP T SNK1 AUXCH N | GND_VOID=TRUE |

DRAWING: LAST MODIFIED=Tue Aug 30 11:06:29 2016

Apple Inc.

051-00777

9.0.0

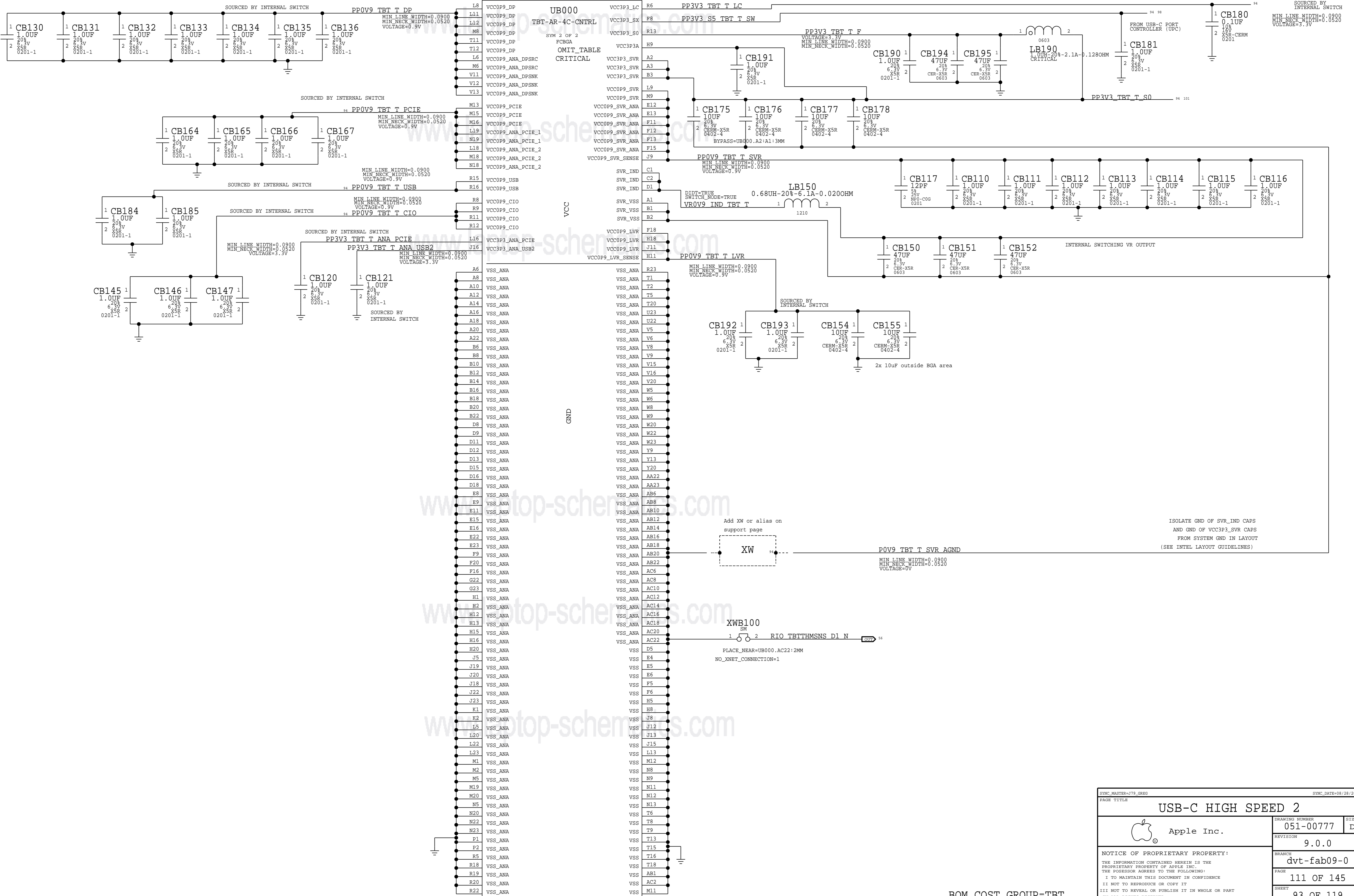
dvt-fab09-0

110 OF 145

92 OF 119

NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 112 ALL RIGHTS RESERVED

BOM_COST_GROUP=TBT



| | | | |
|---|--|----------------------|-------------|
| SYNC_MASTER=779_0REG | | SYNC_DATE=08/28/2015 | |
| PAGE TITLE | | | |
| | | DRAWING NUMBER | 51-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 2 NOT TO REPRODUCE OR COPY IT 3 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 4 ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 111 OF 145 |
| | | SHEET | 93 OF 119 |
| | | STAR | |

BOM_COST_GROUP=TBT

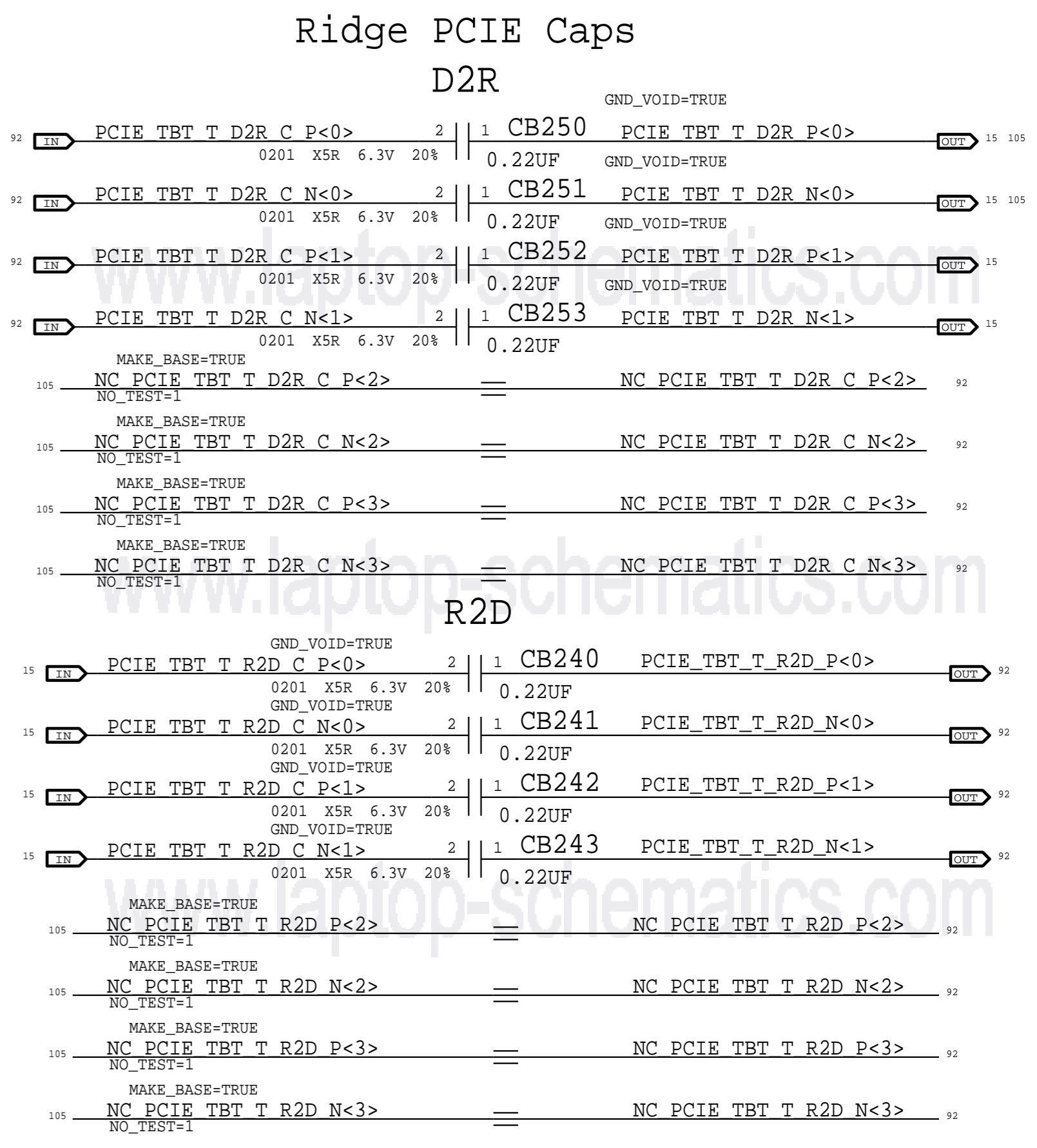
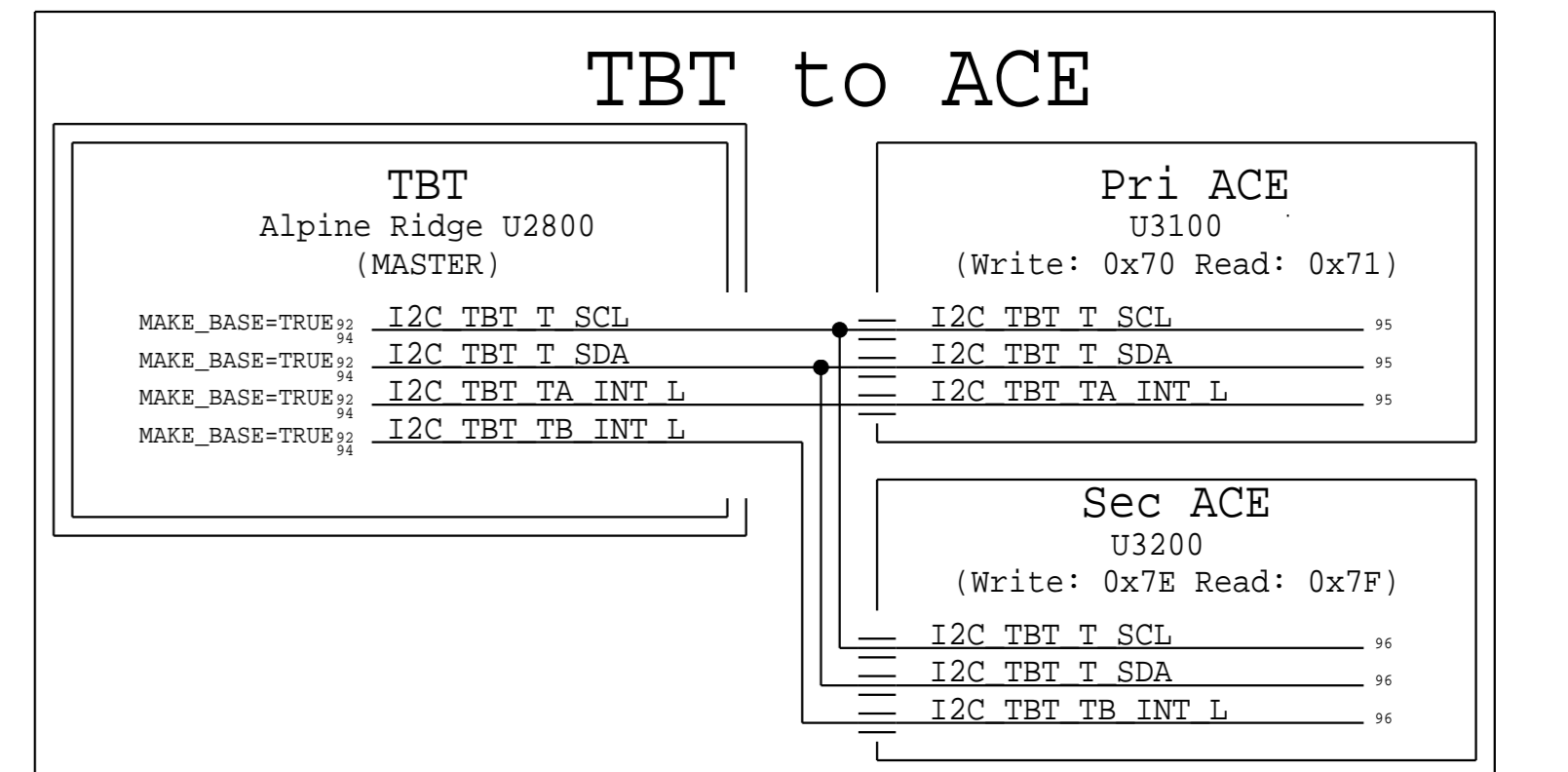
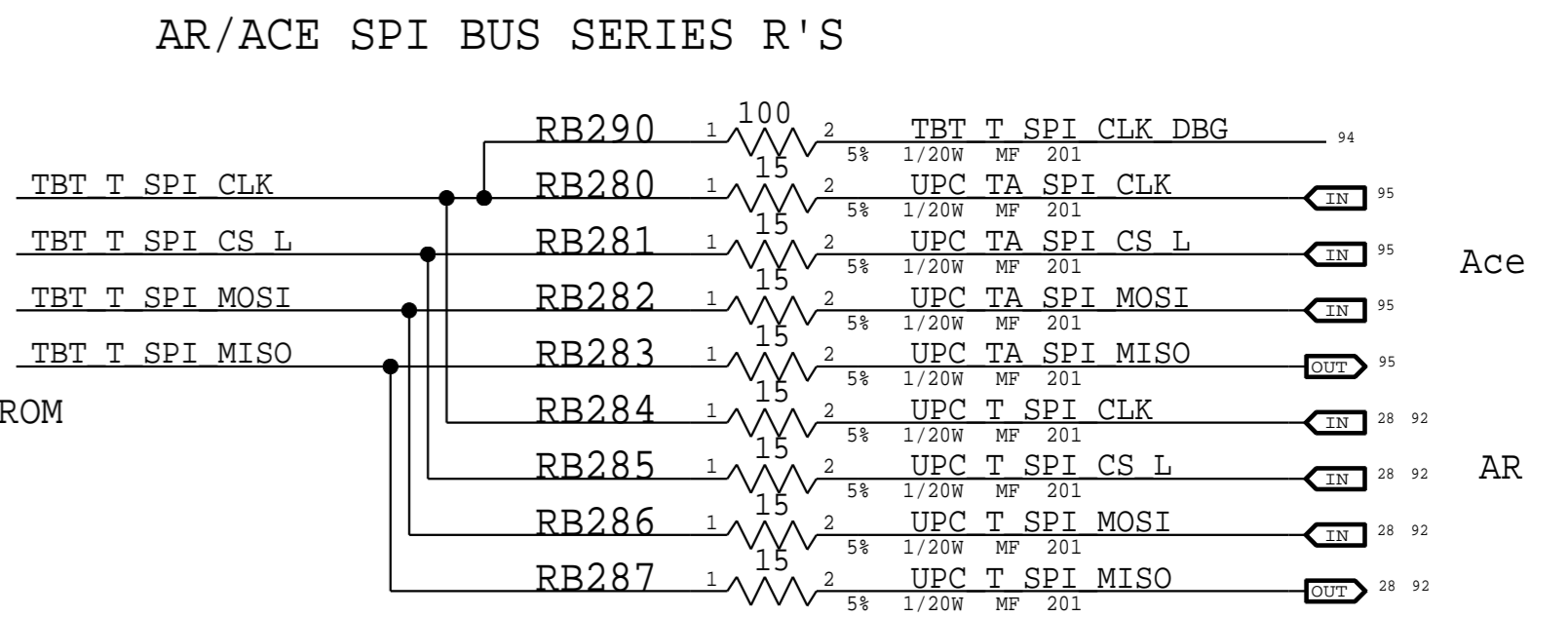
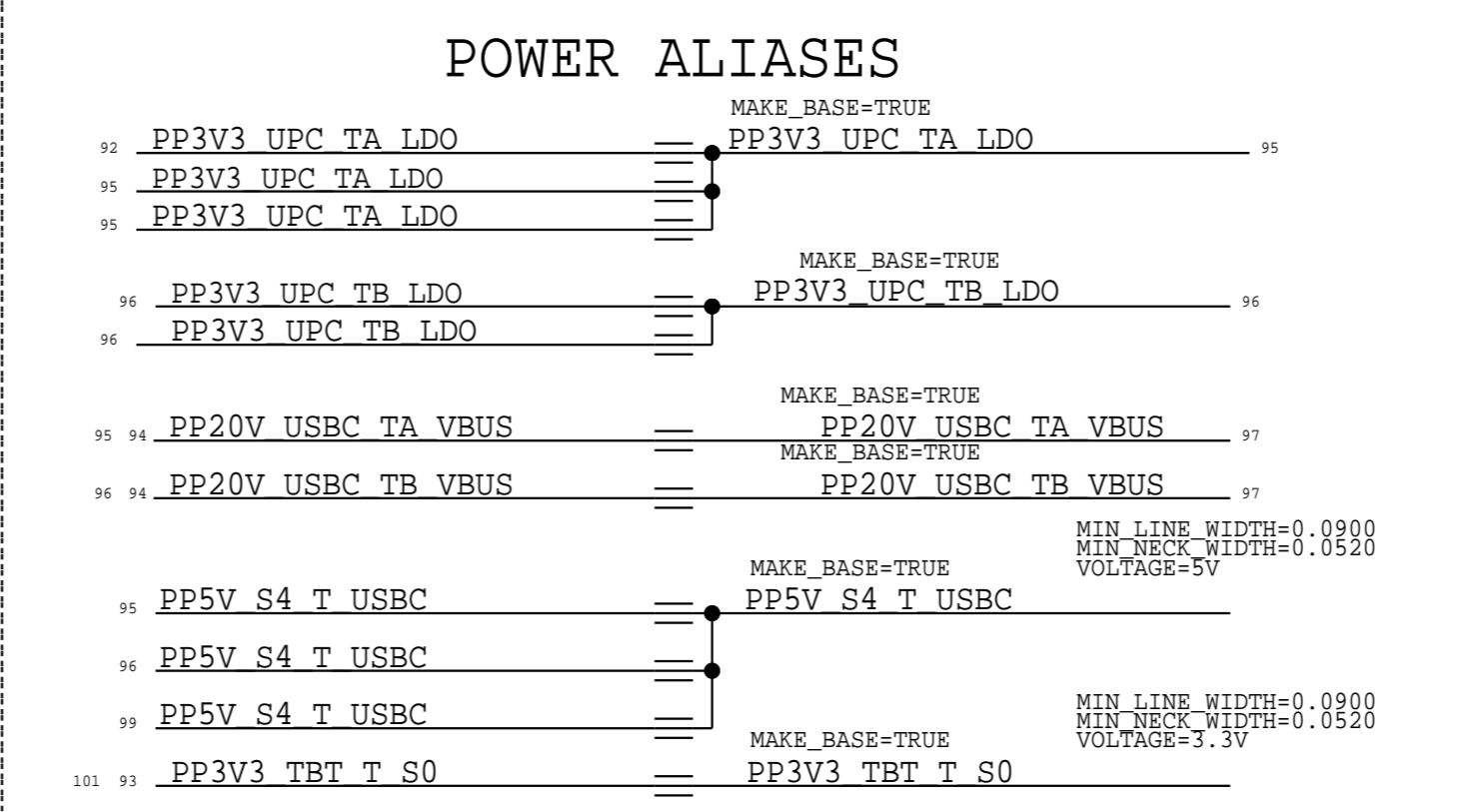
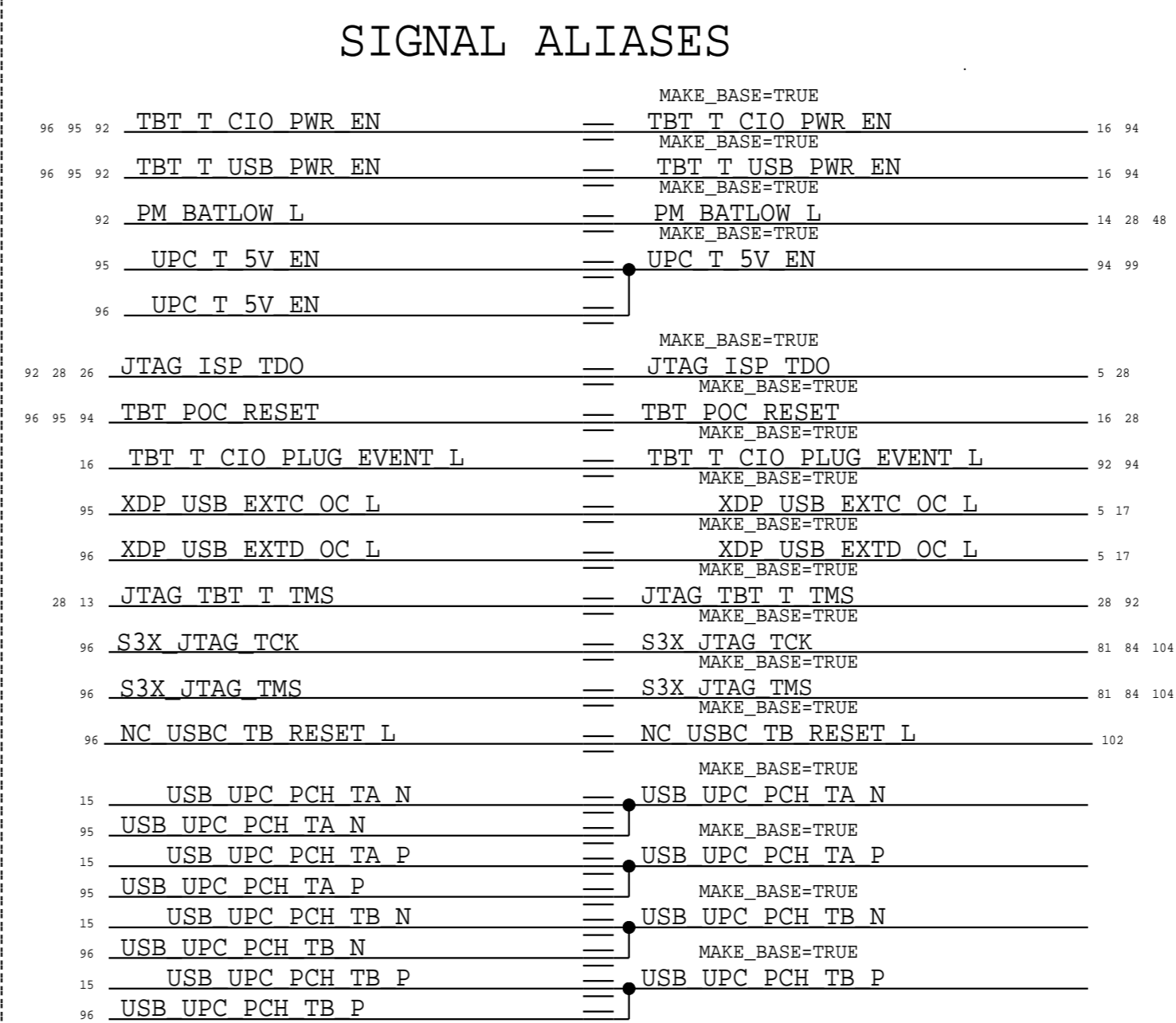
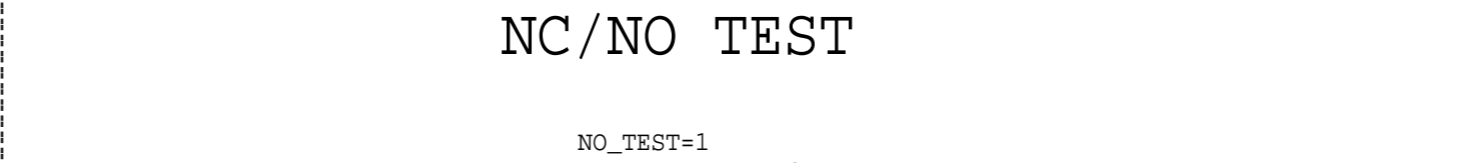
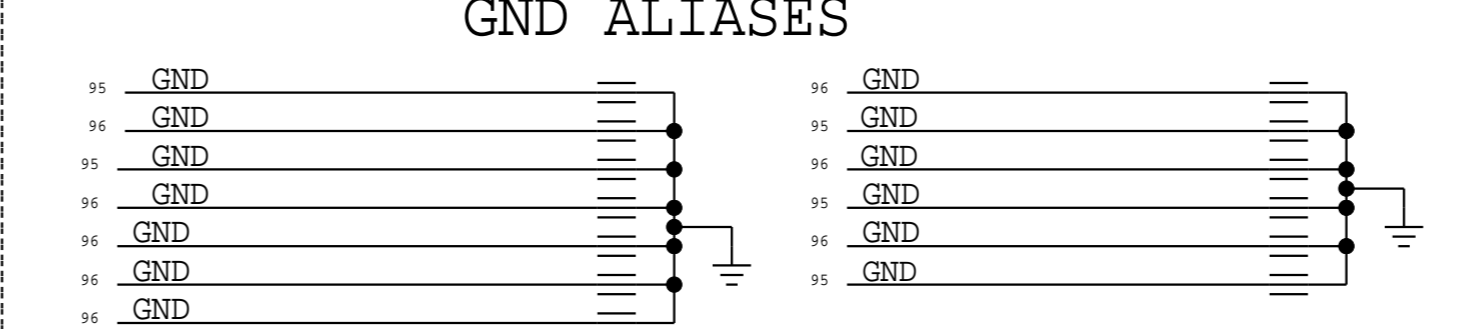
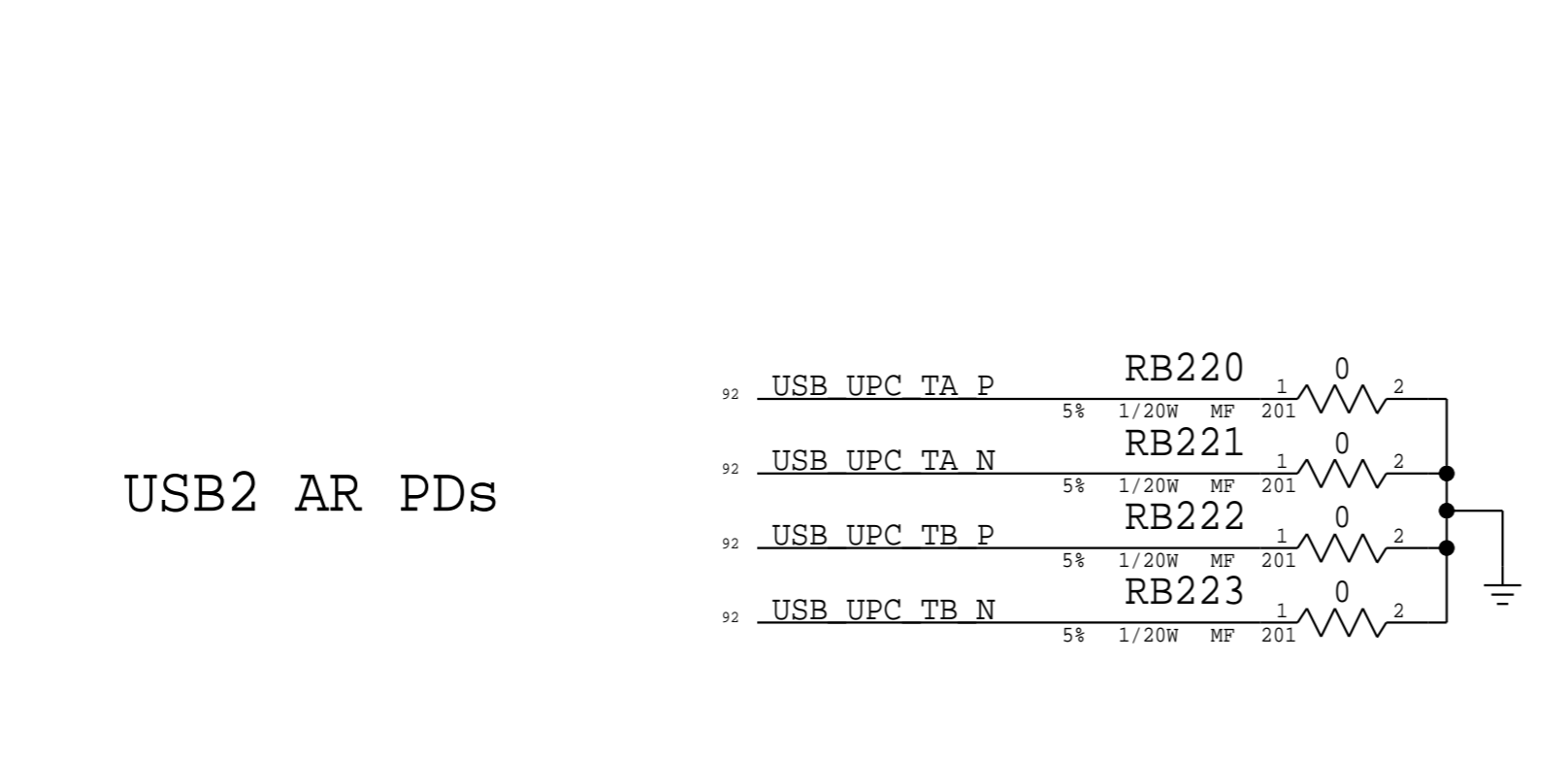
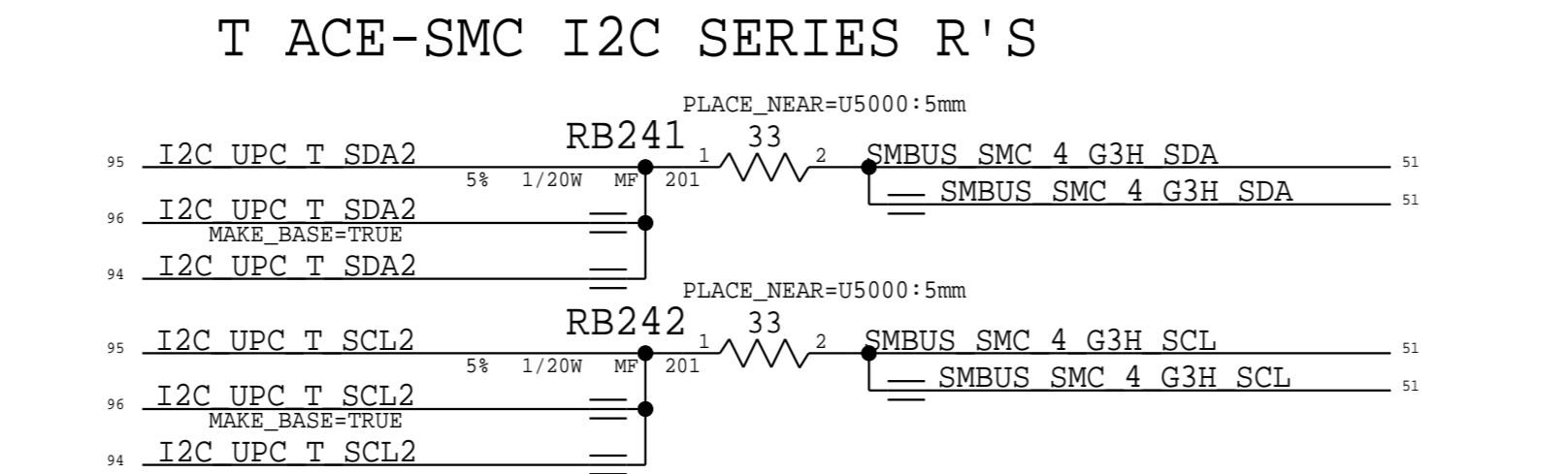
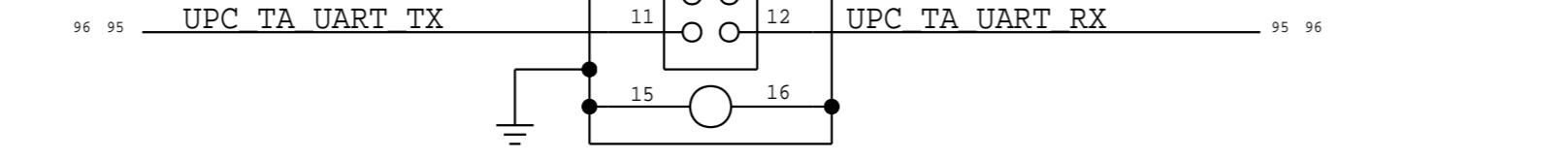
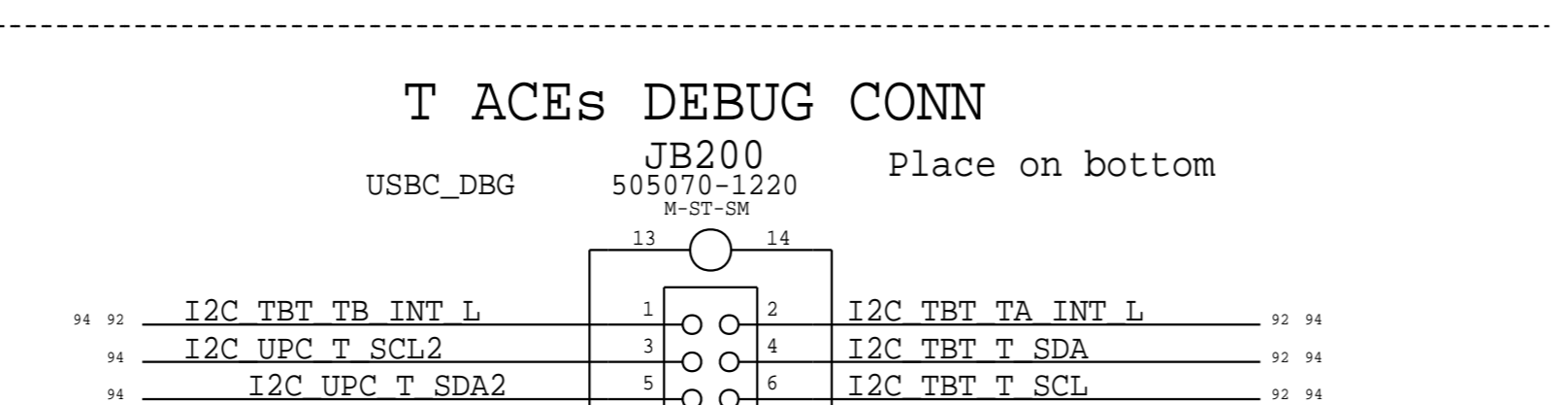
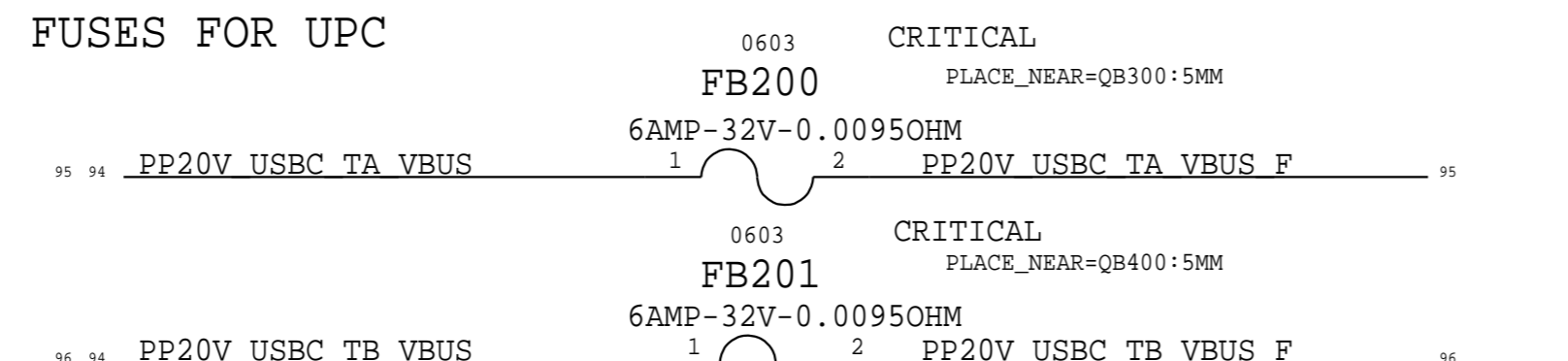
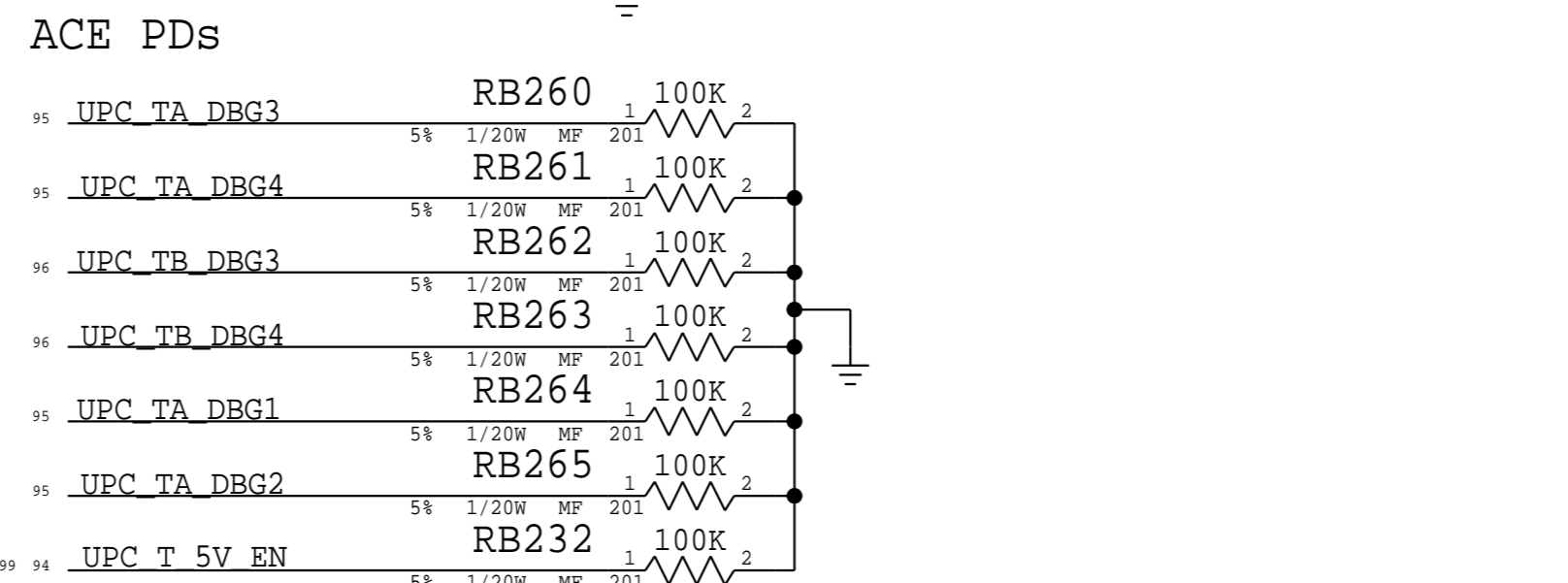
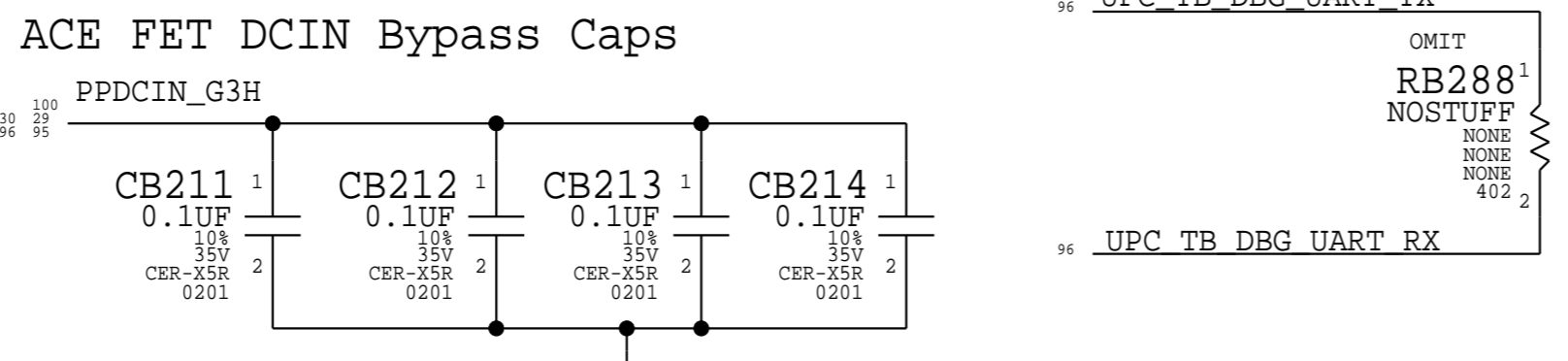
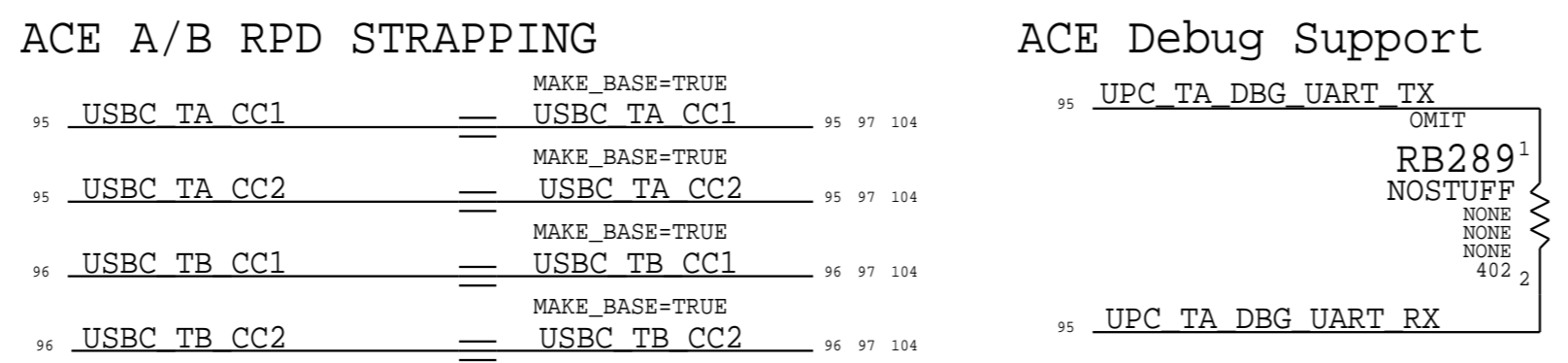
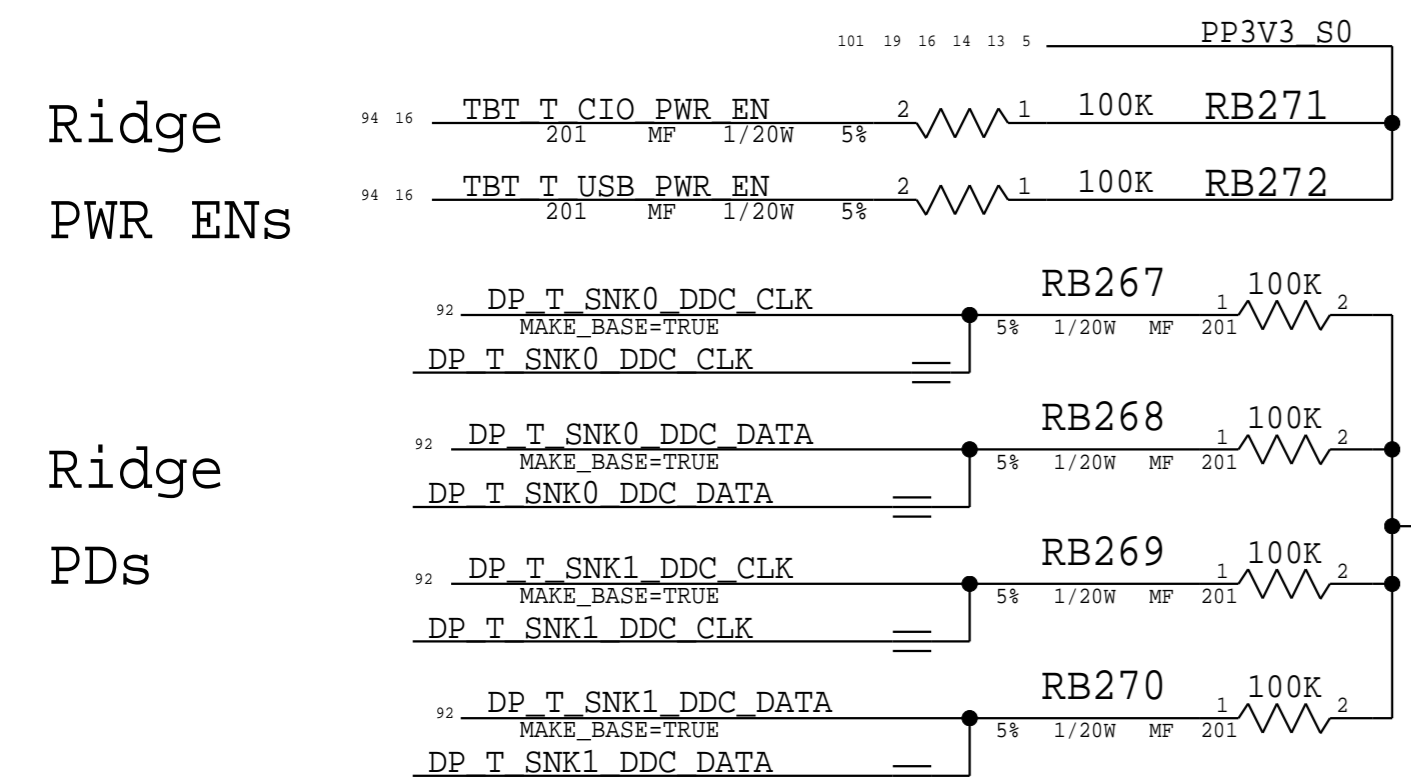
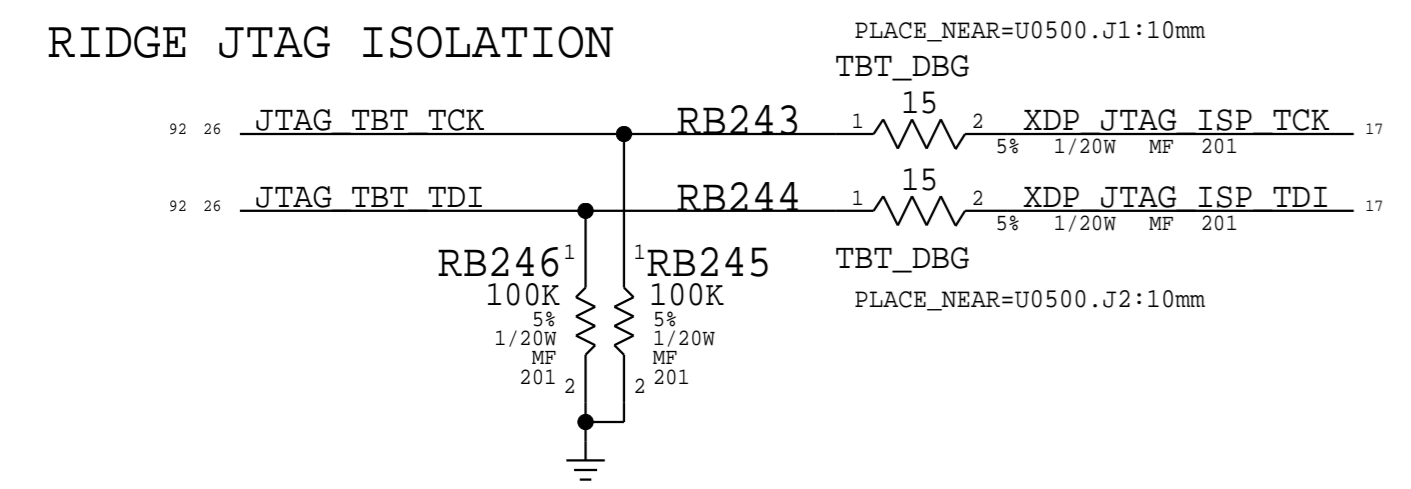
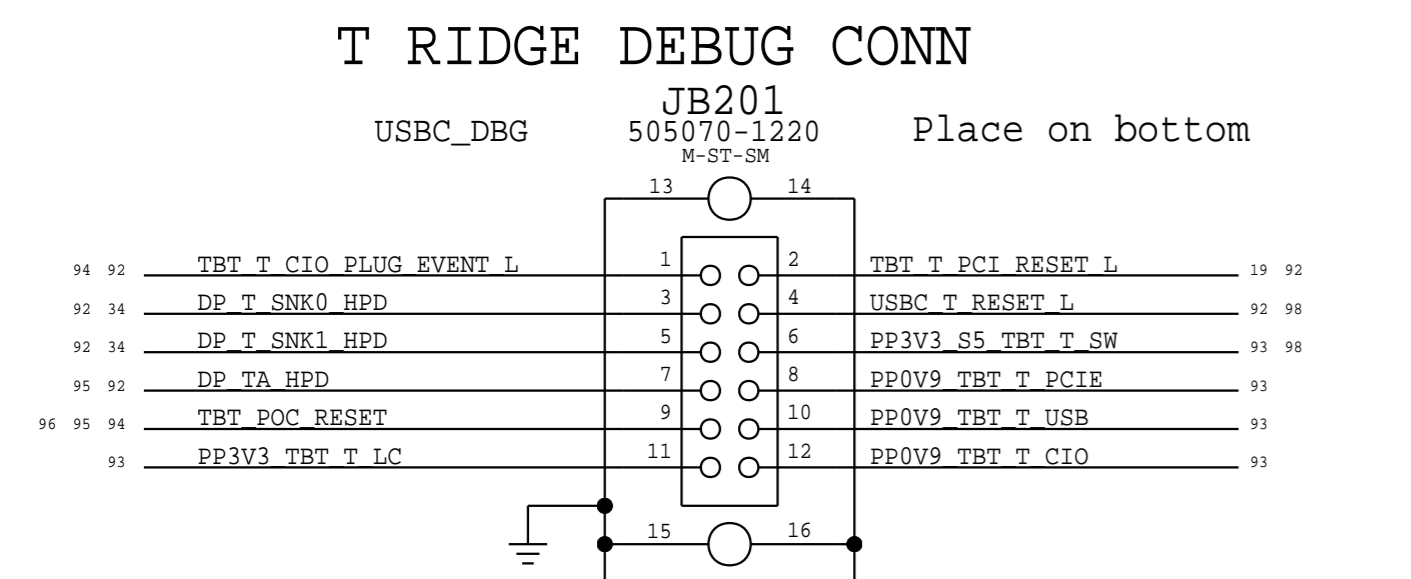
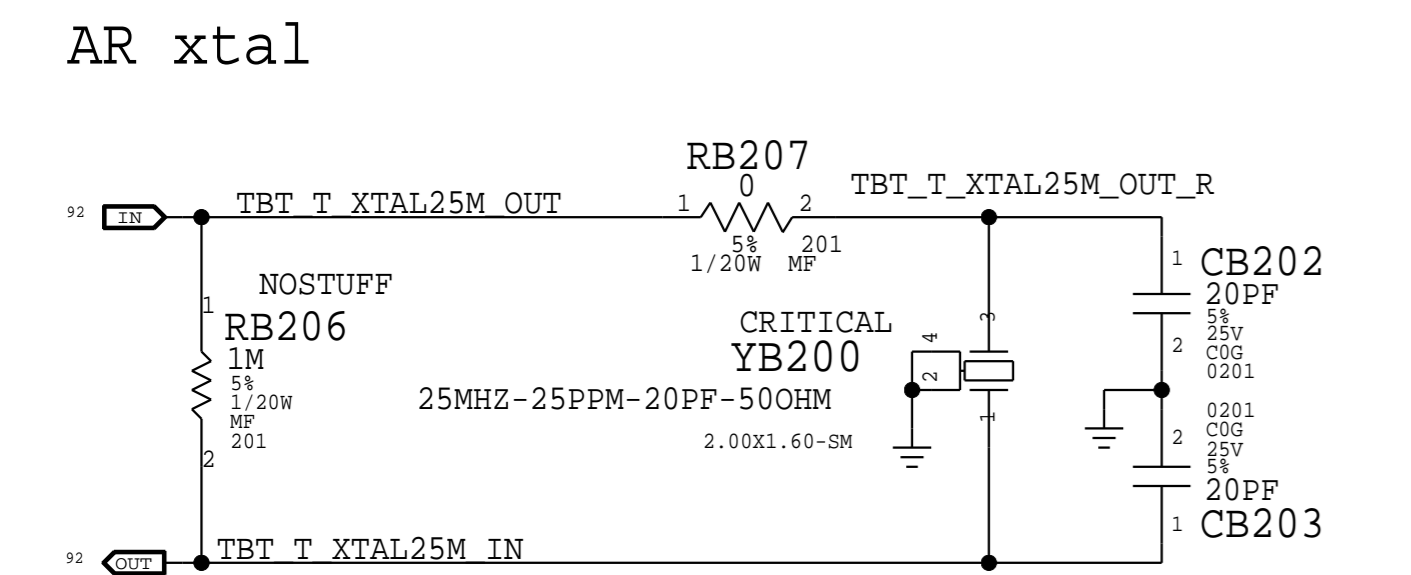
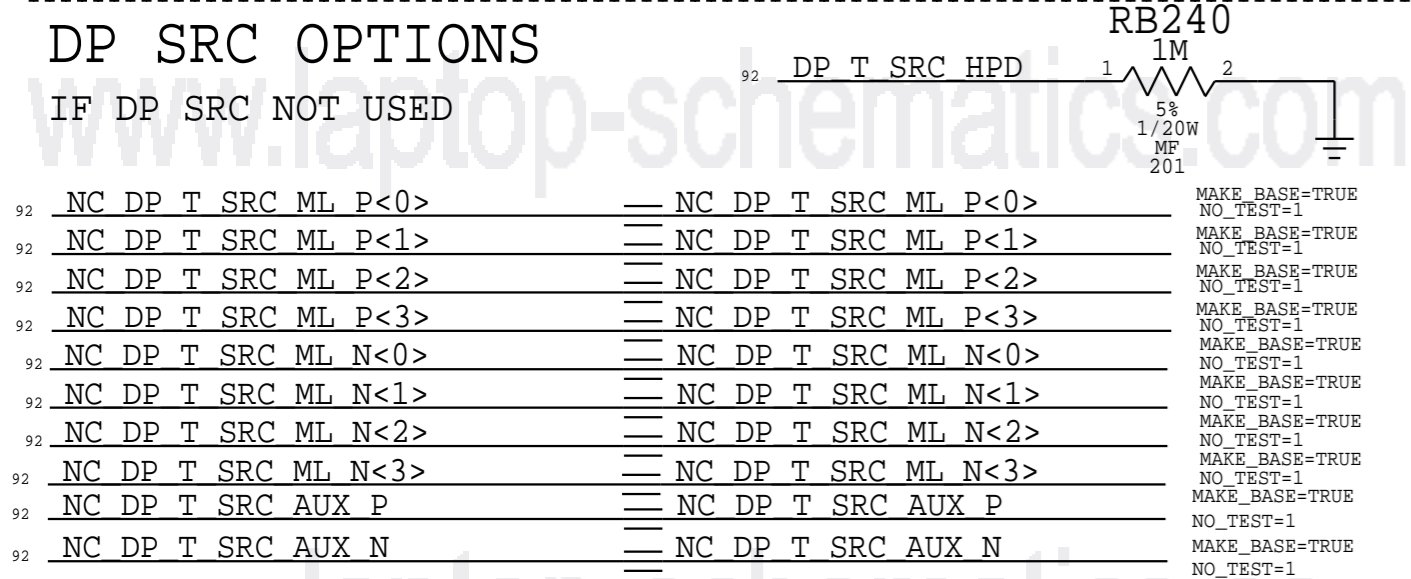
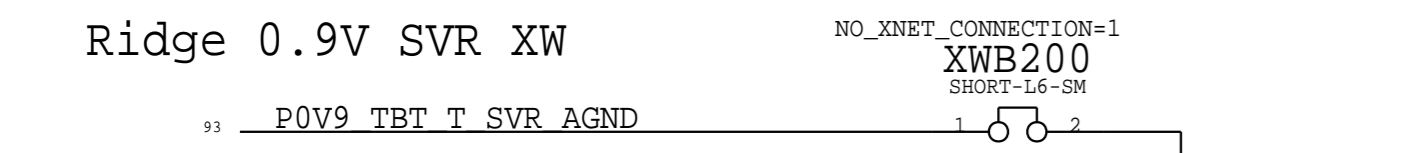
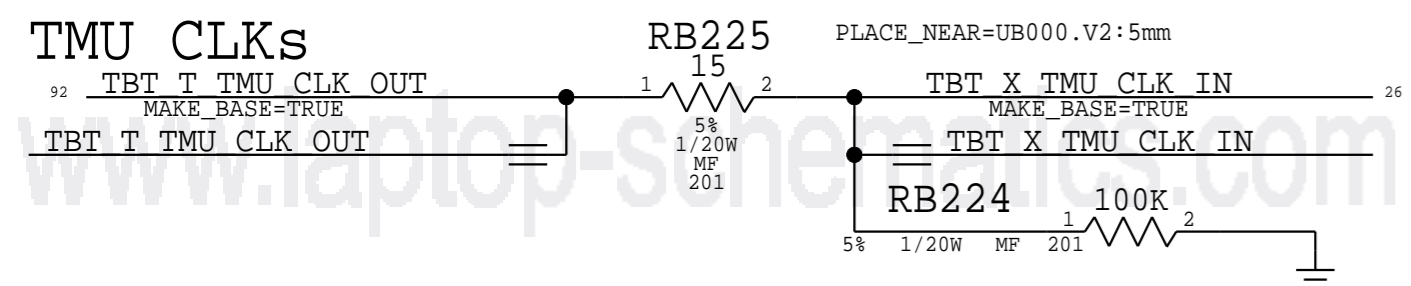
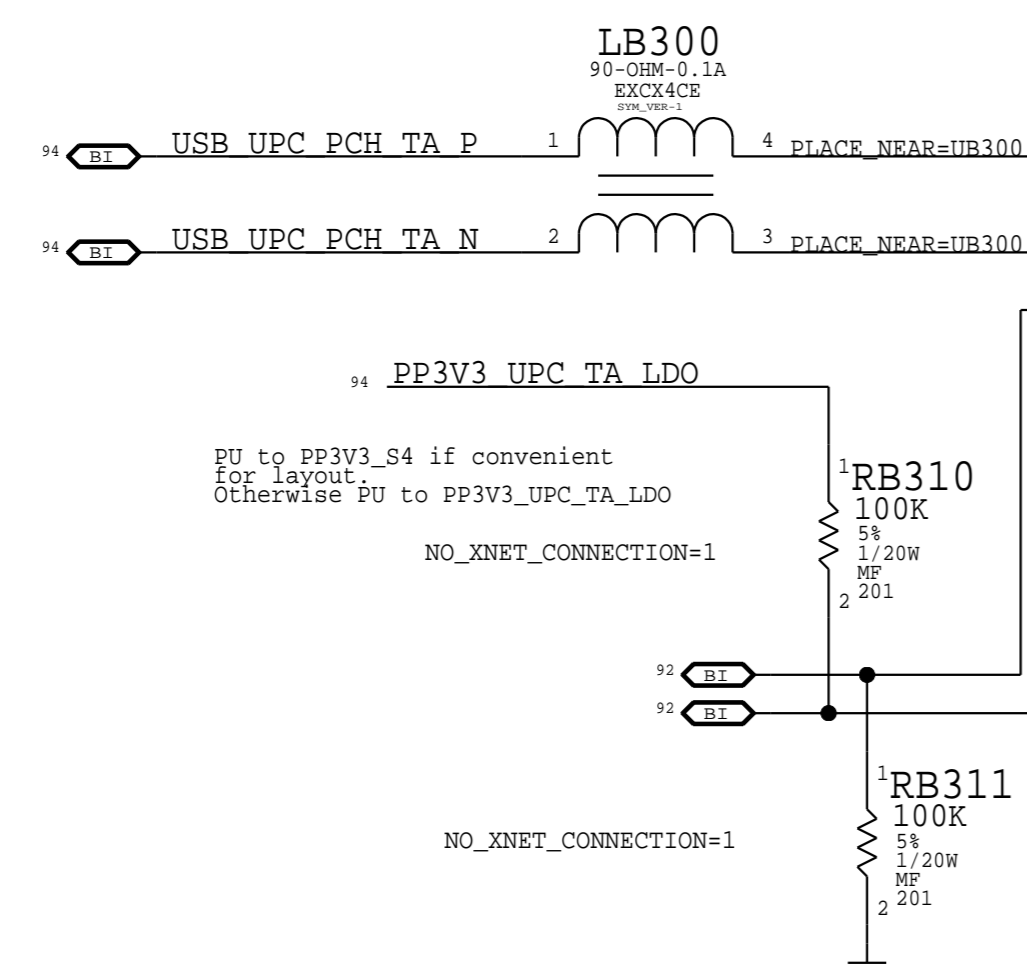
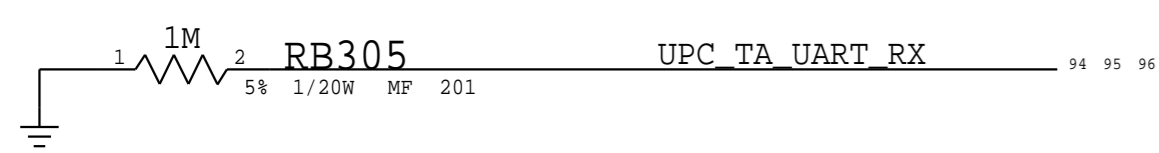
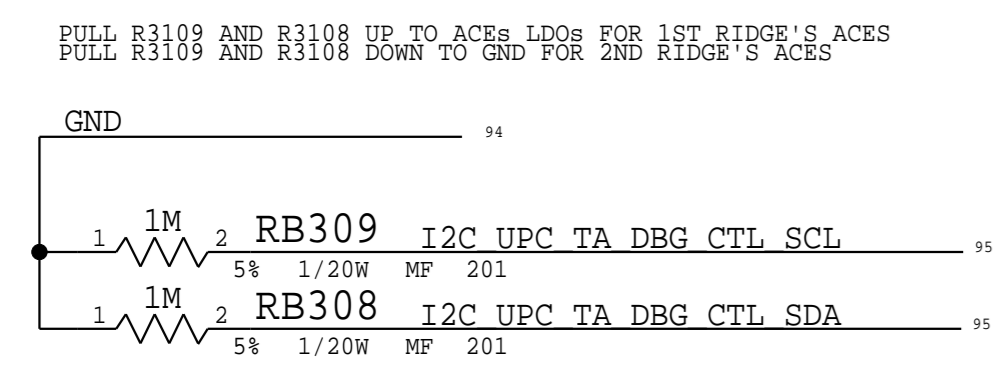
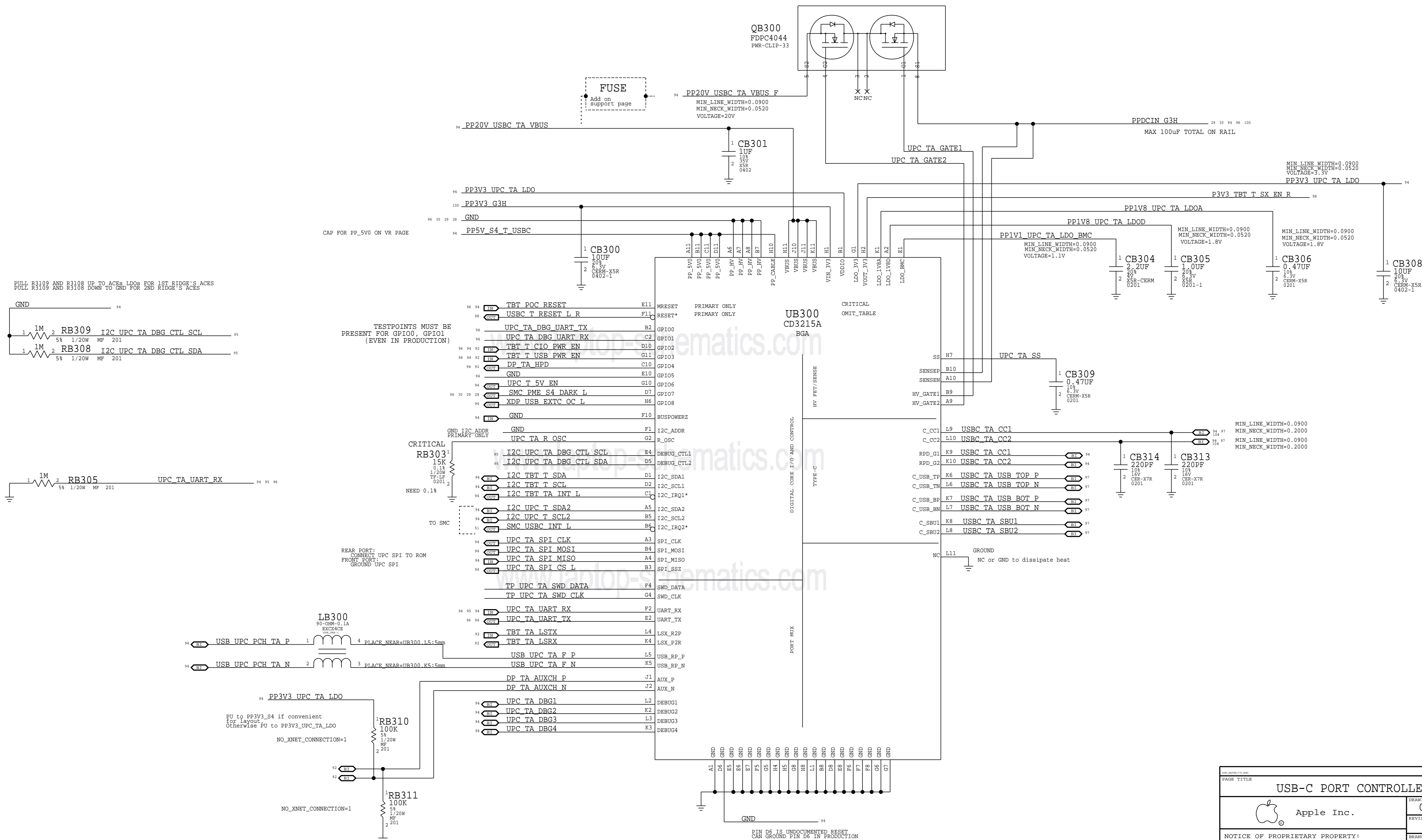


Table with 2 columns: Apple Inc. logo and text, and drawing information including drawing number 051-00777, revision 9.0.0, page 112 OF 145, and sheet 94 OF 119.

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

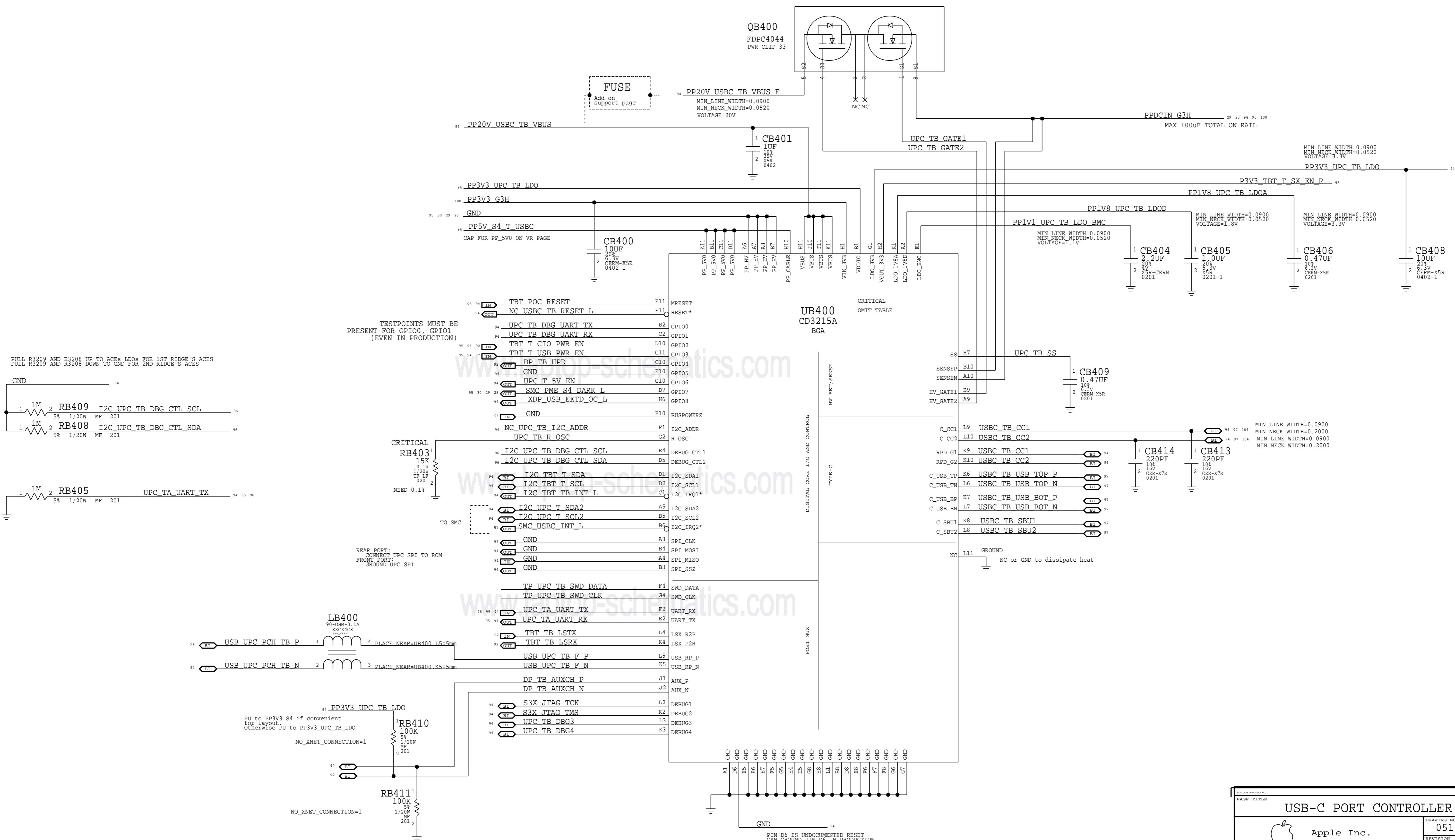


| USB-C PORT CONTROLLER A | | |
|---|----------------|-------------|
| Apple Inc. | DRAWING NUMBER | 051-00777 |
| | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1V ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 |
| | PAGE | 113 OF 145 |
| | SHEET | 95 OF 119 |

BOM_COST_GROUP=USB-C

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

SECONDARY ACE USB-C PORT CONTROLLER (UPC)



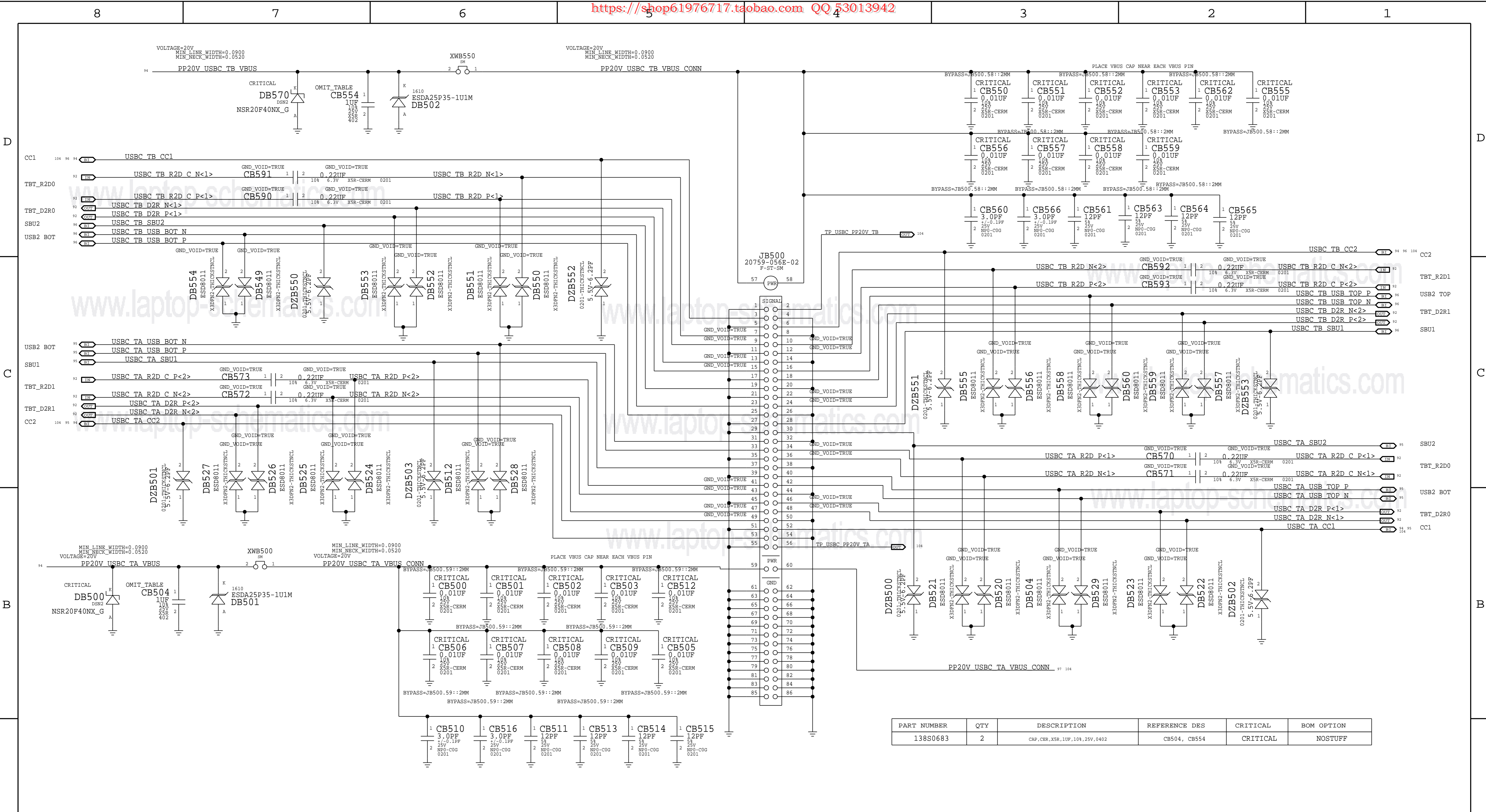
PULL R3209 AND R3208 UP TO ACES LDOs FOR 1ST RIDGE'S ACES
 PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

REAR PORT: CONNECT UPC SPI TO ROM
 FRONT PORT: GROUND UPC SPI

| | | |
|------------------------------------|------------------|--|
| | | |
| USB-C PORT CONTROLLER B | | |
| DRAWING NUMBER 051-00777 | SIZE D | |
| REVISION 9.0.0 | | |
| BRANCH dvt-fab09-0 | | |
| PAGE 114 OF 145 | | |
| SHEET 96 OF 119 | | |

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 11 NOT TO REPRODUCE OR COPY IT
 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 1111 ALL RIGHTS RESERVED



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|------------------------------------|---------------|----------|------------|
| 138S0683 | 2 | CAP, CER, XSR, 1UF, 10%, 25V, 0402 | CB504, CB554 | CRITICAL | NOSTUFF |

LAST CHANGE: Wed Apr 1 22:57:37 2015

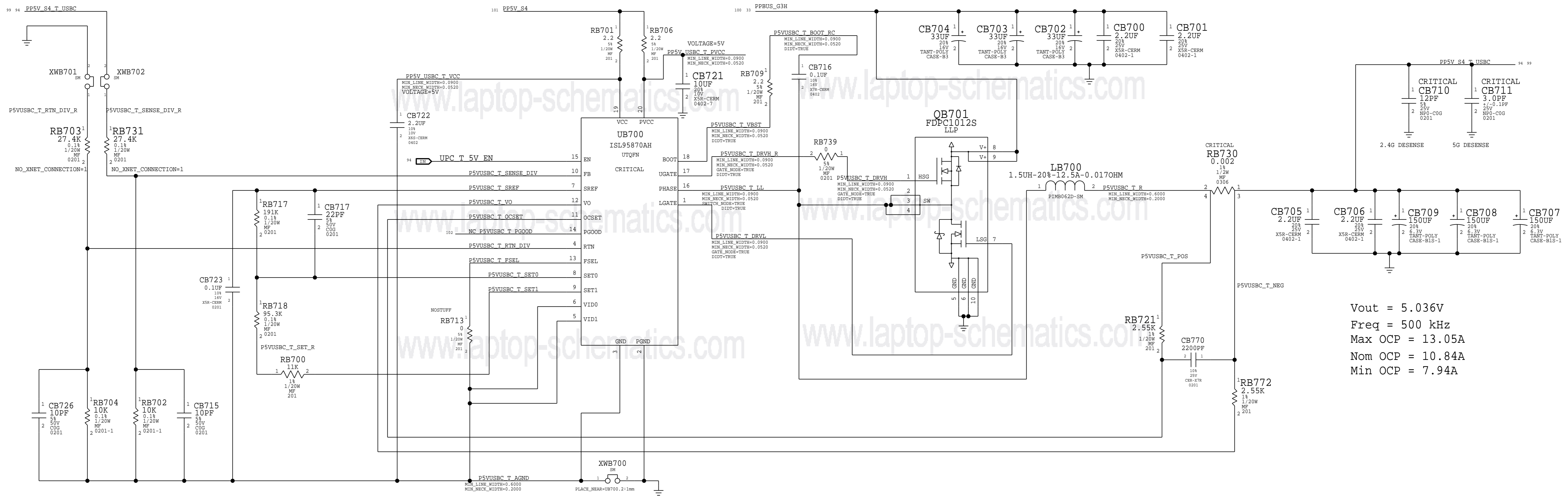
PAGE TITLE: **USB-C CONNECTOR A**

Apple Inc.

| | | | |
|----------------|------------|--------|-------------|
| DRAWING NUMBER | 051-00777 | SIZE | D |
| REVISION | 9.0.0 | BRANCH | dvt-fab09-0 |
| PAGE | 115 OF 145 | SHEET | 97 OF 119 |

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 I NOT TO REPRODUCE OR COPY IT
 I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 I ALL RIGHTS RESERVED

BOM_COST_GROUP=USB-C



Vout = 5.036V
 Freq = 500 kHz
 Max OCP = 13.05A
 Nom OCP = 10.84A
 Min OCP = 7.94A

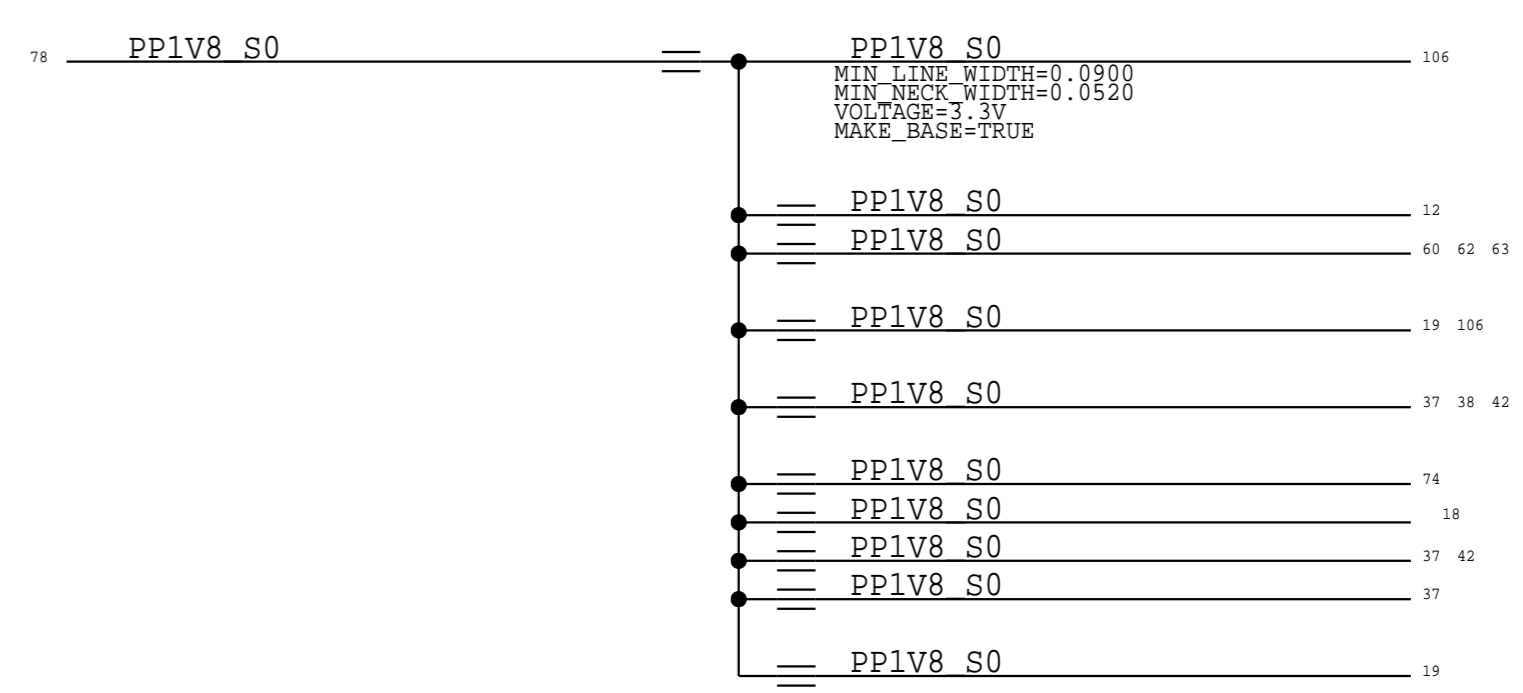
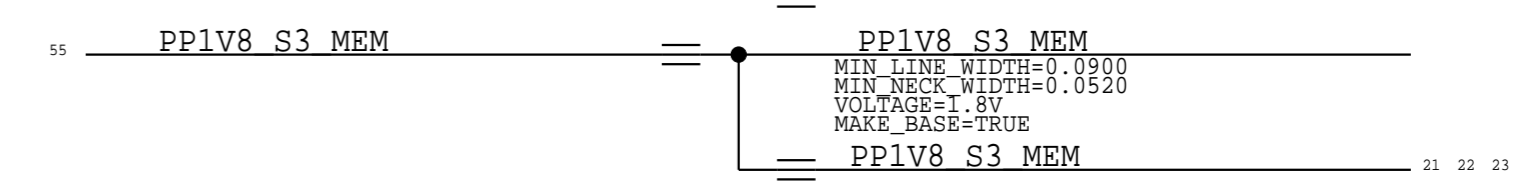
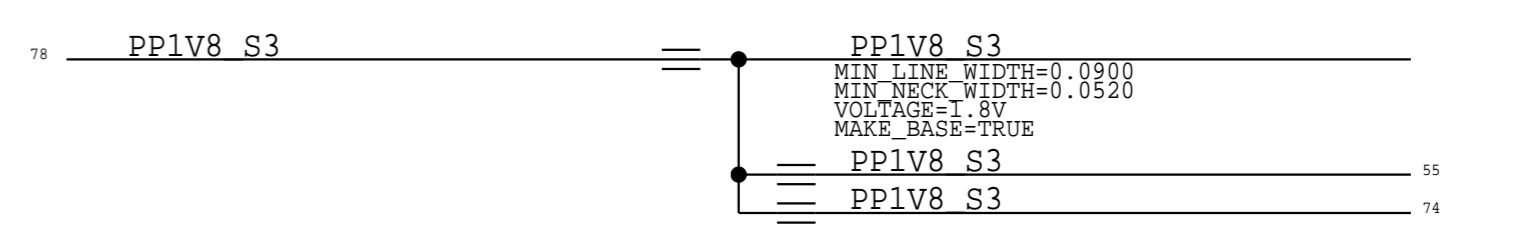
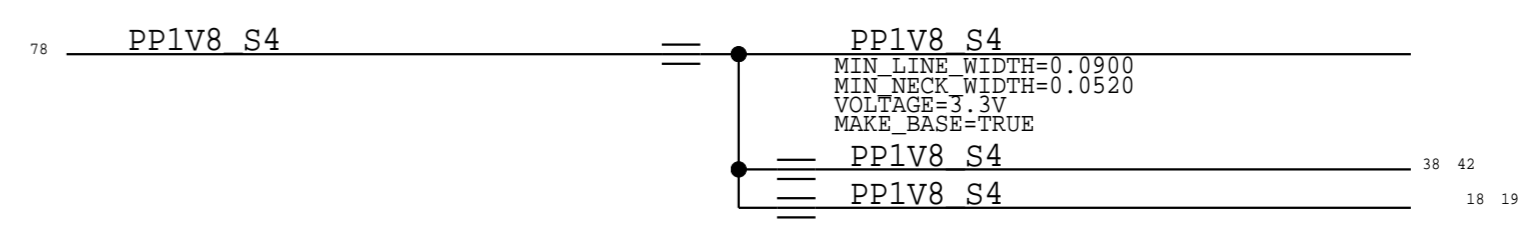
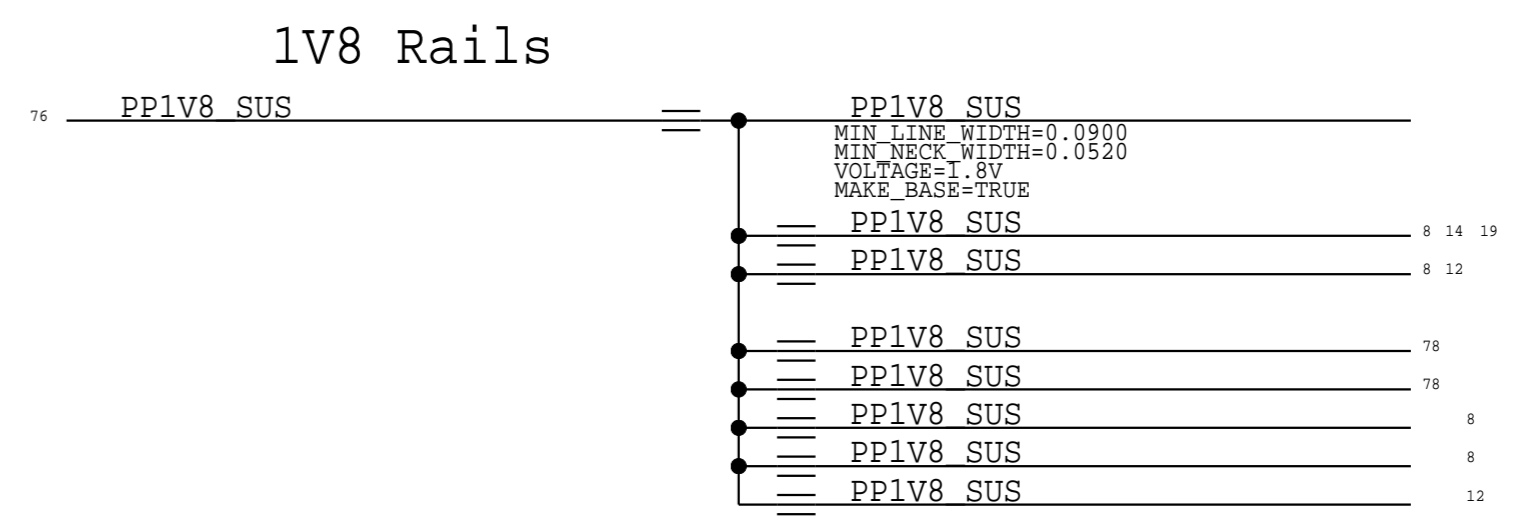
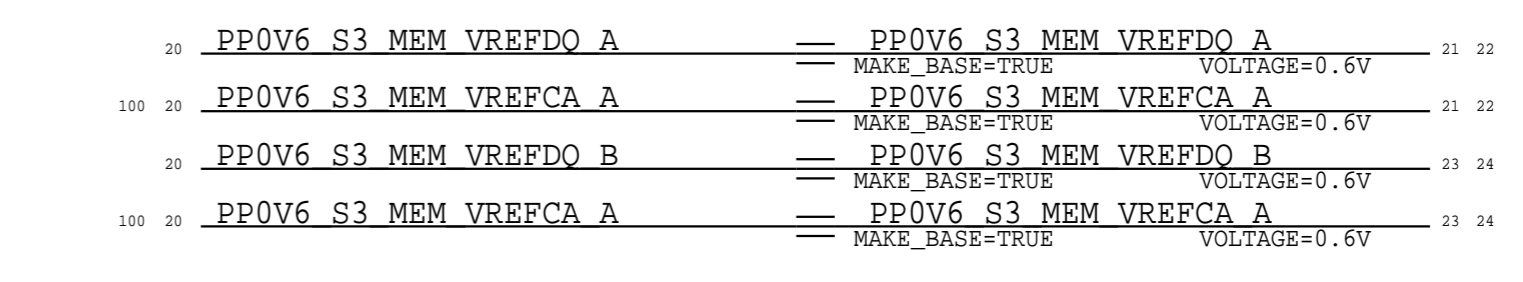
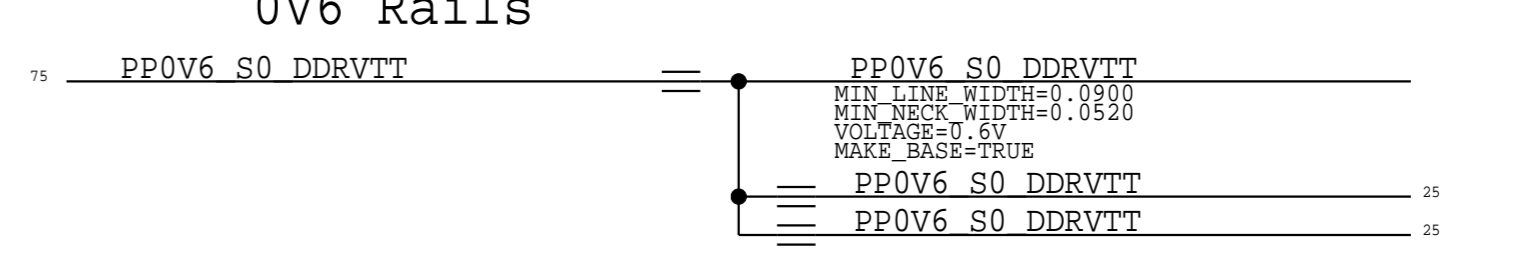
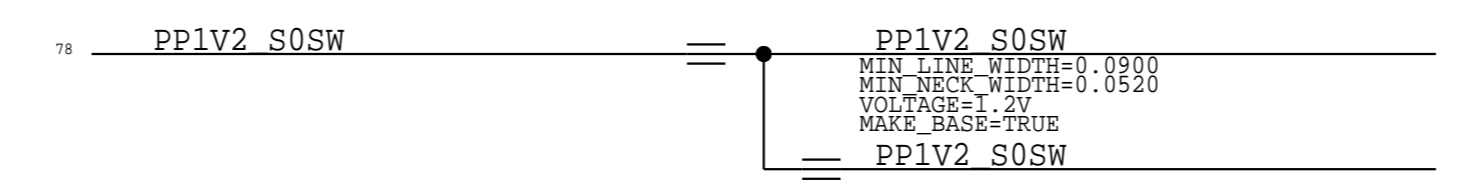
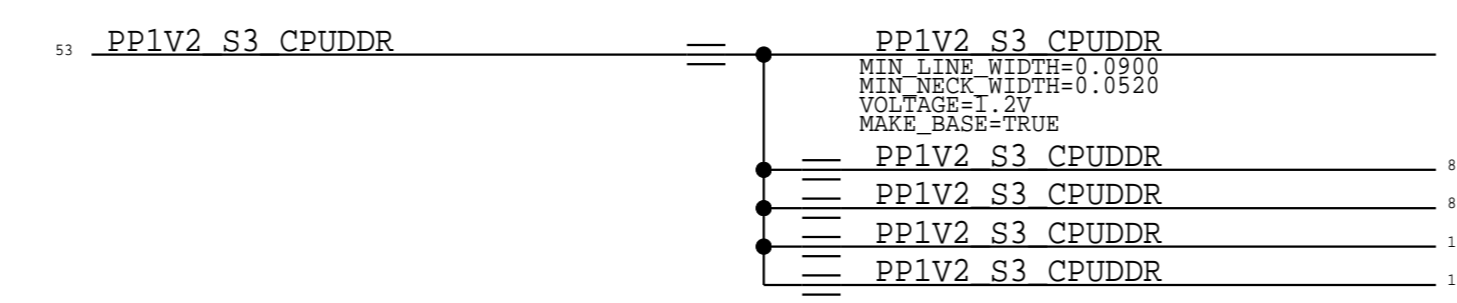
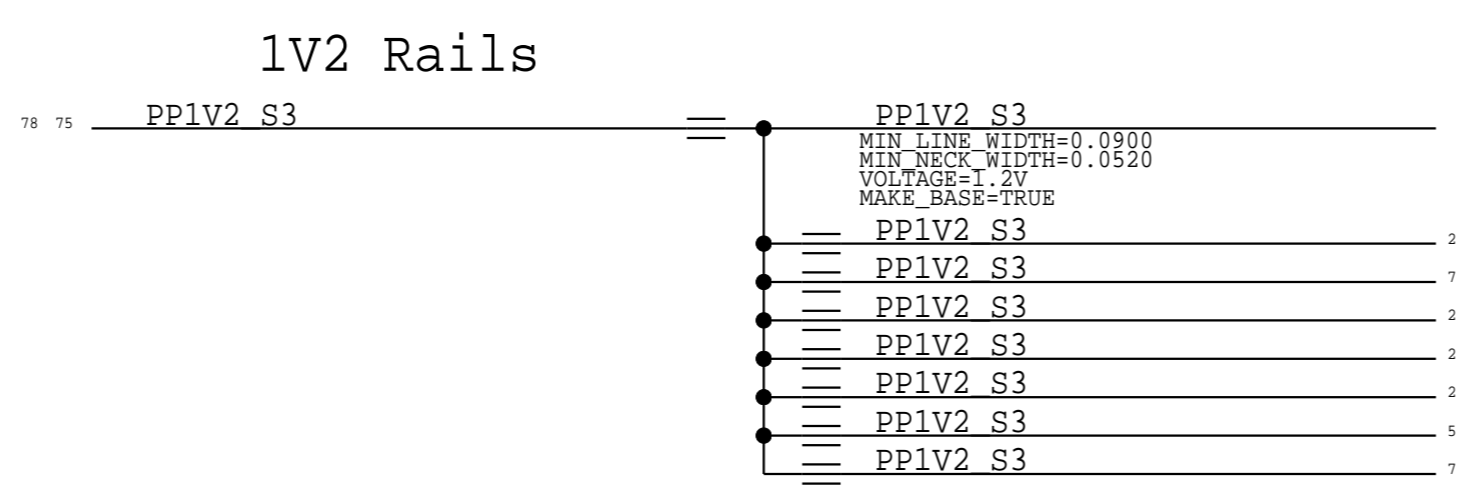
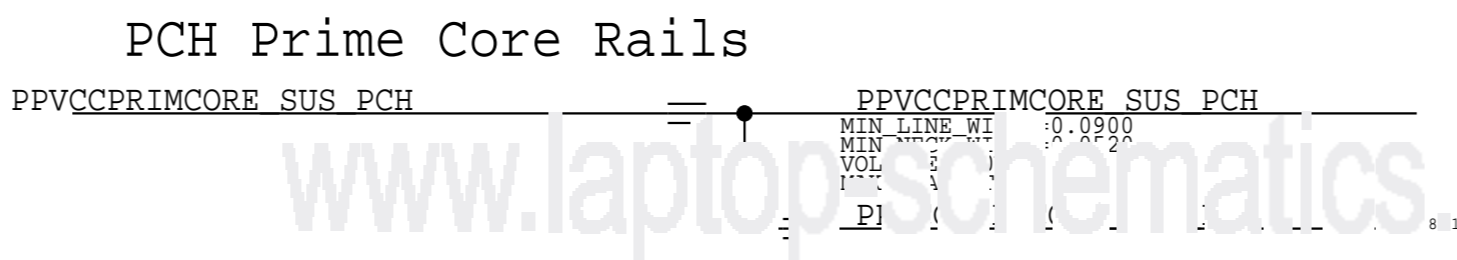
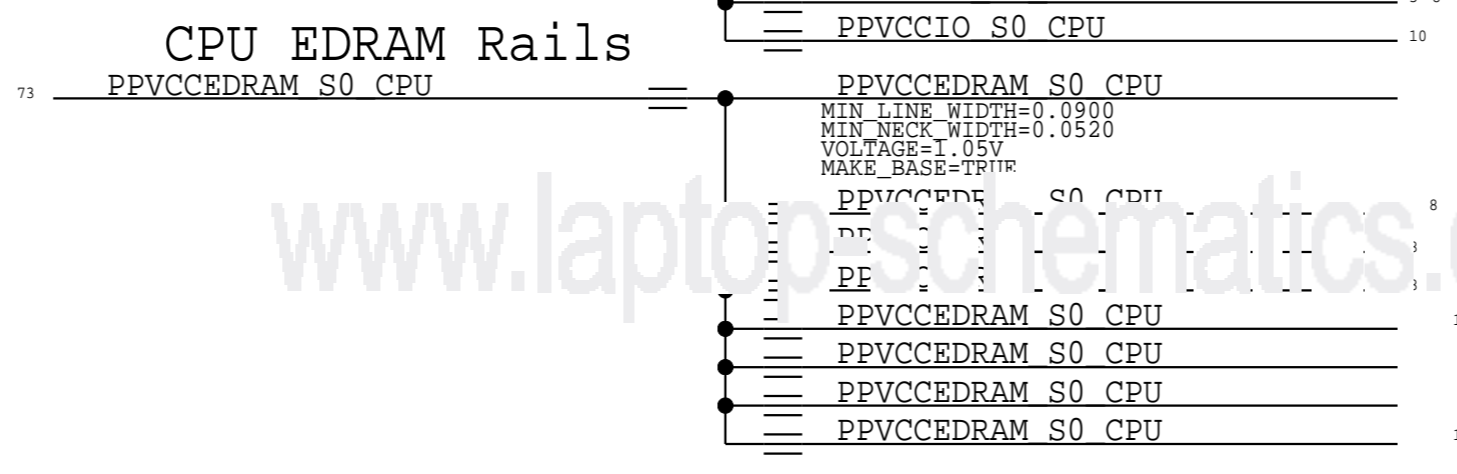
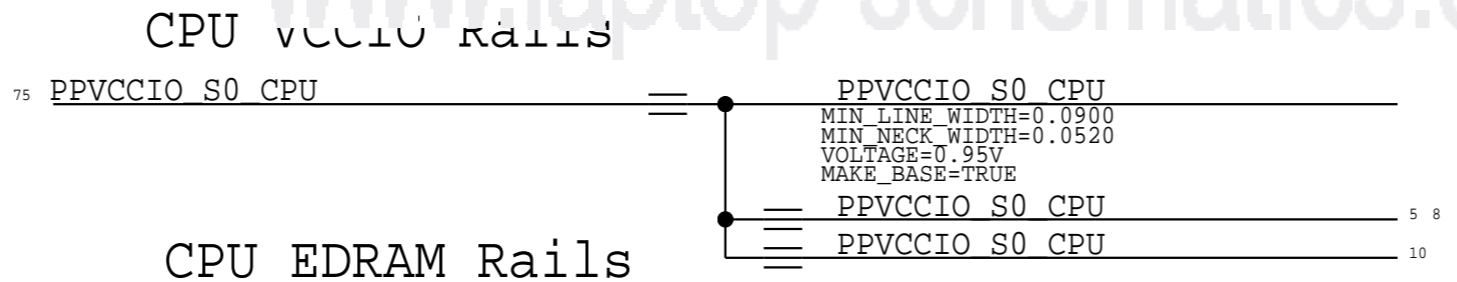
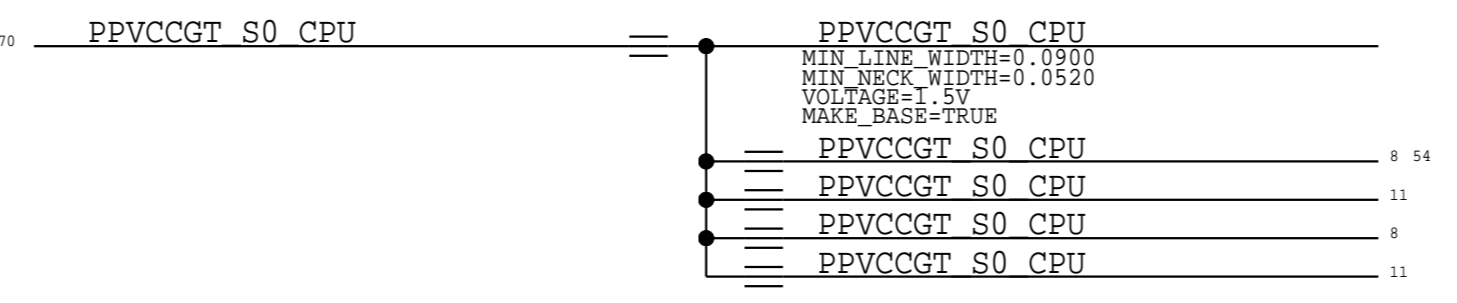
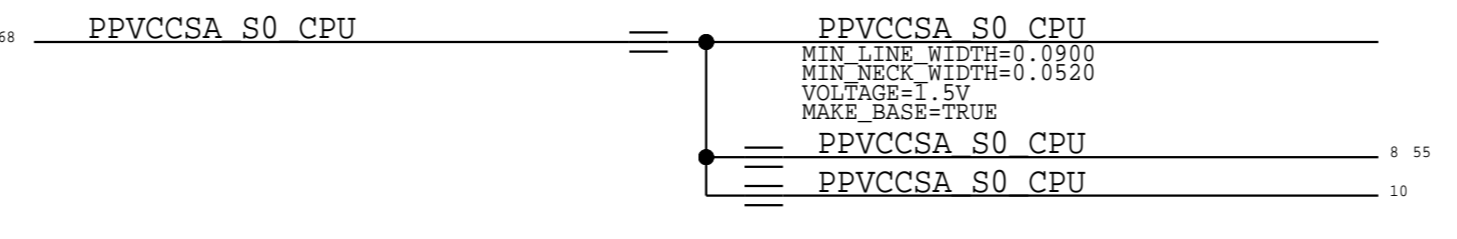
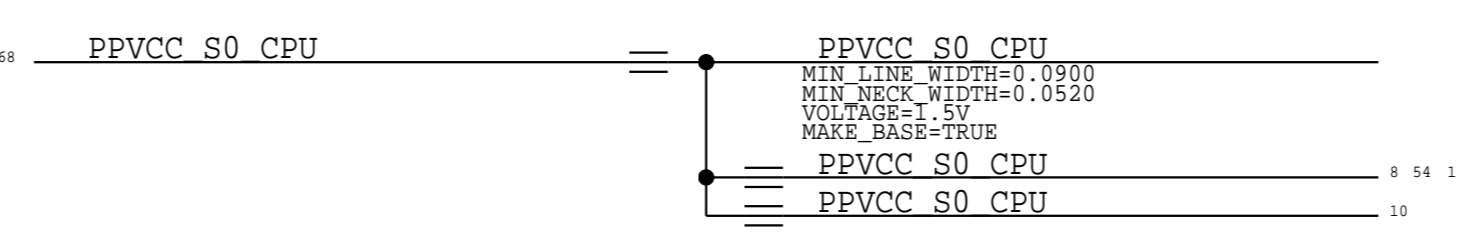
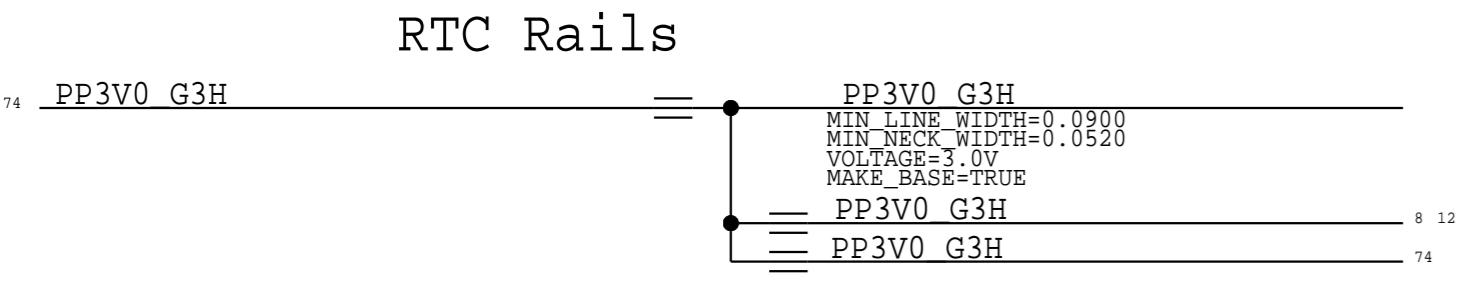
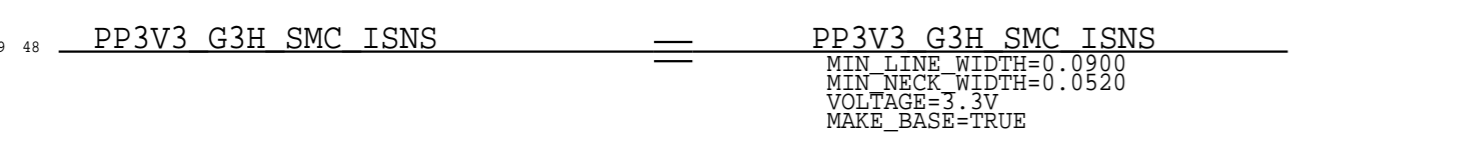
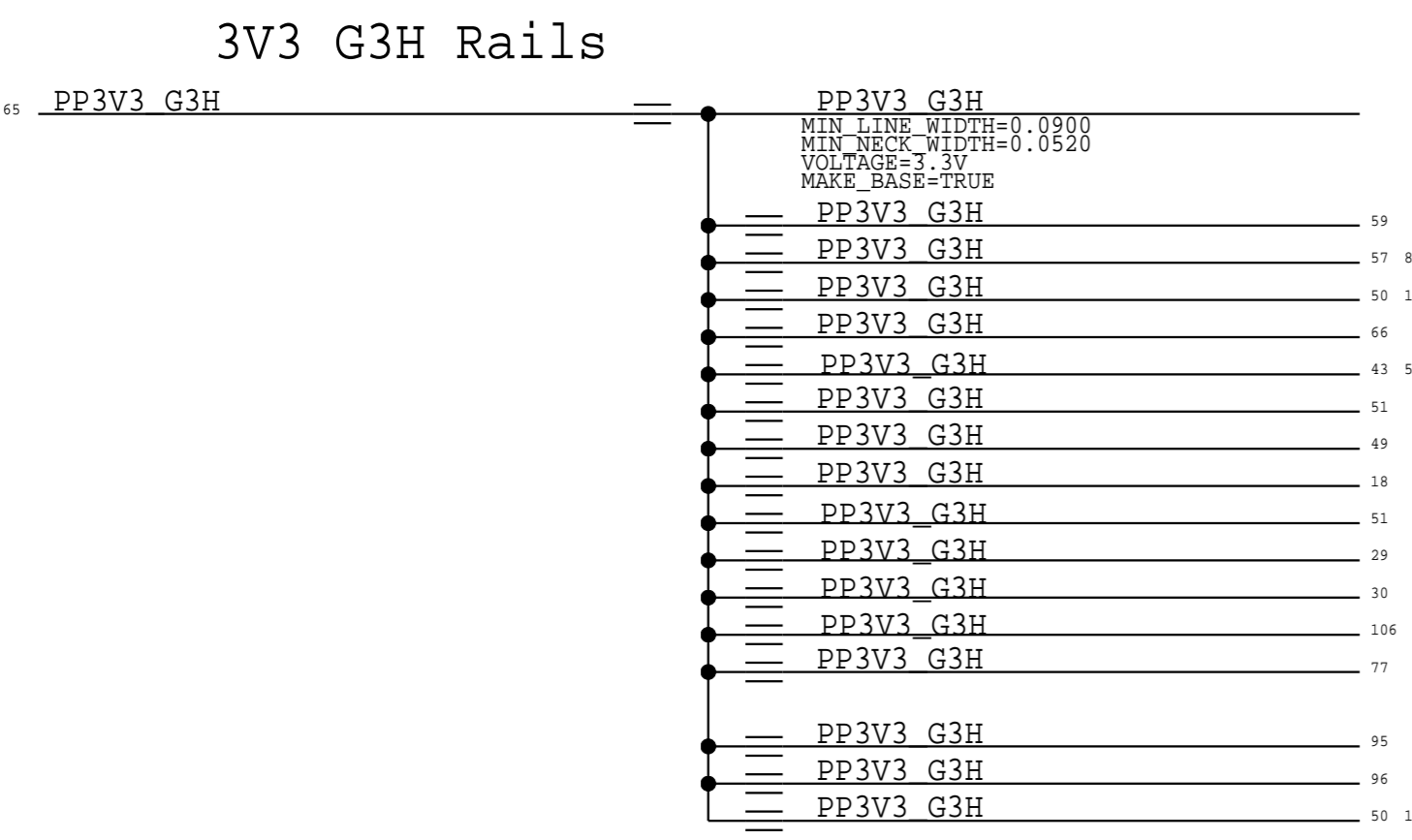
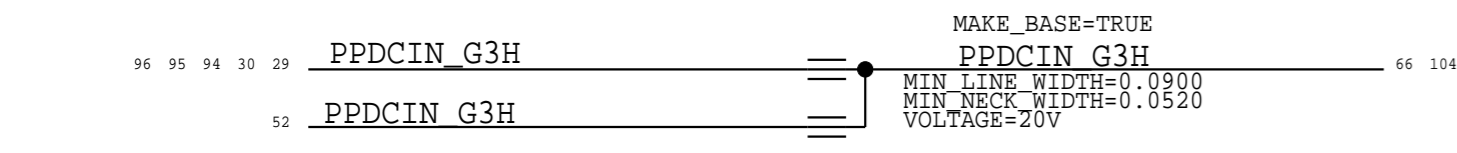
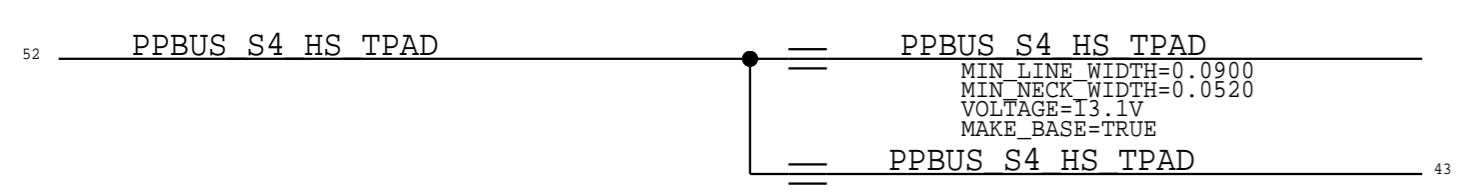
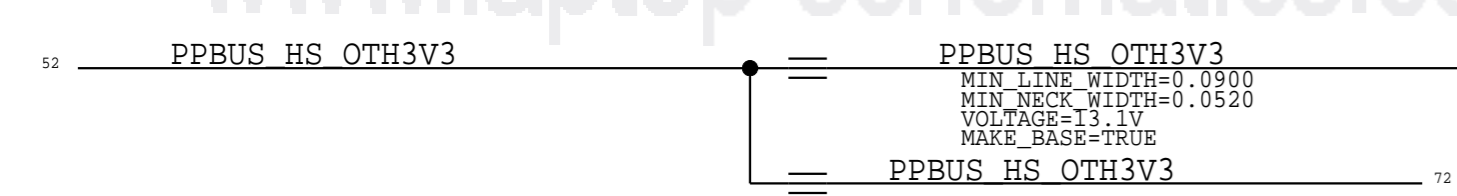
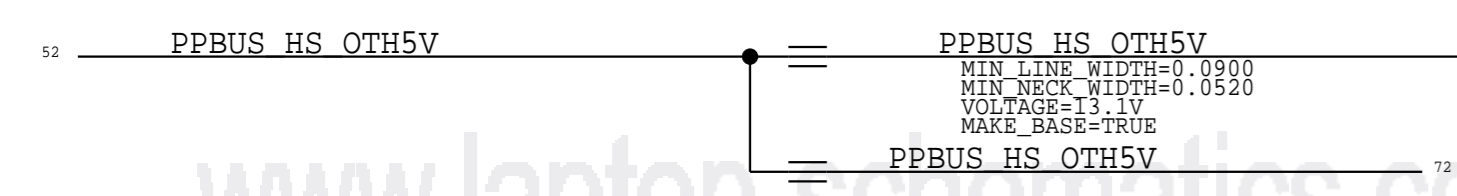
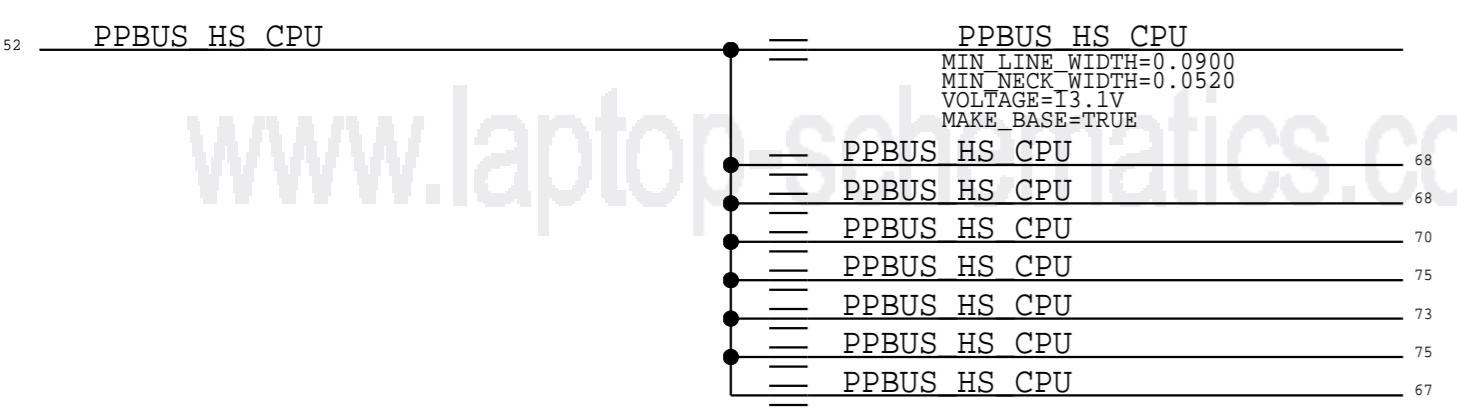
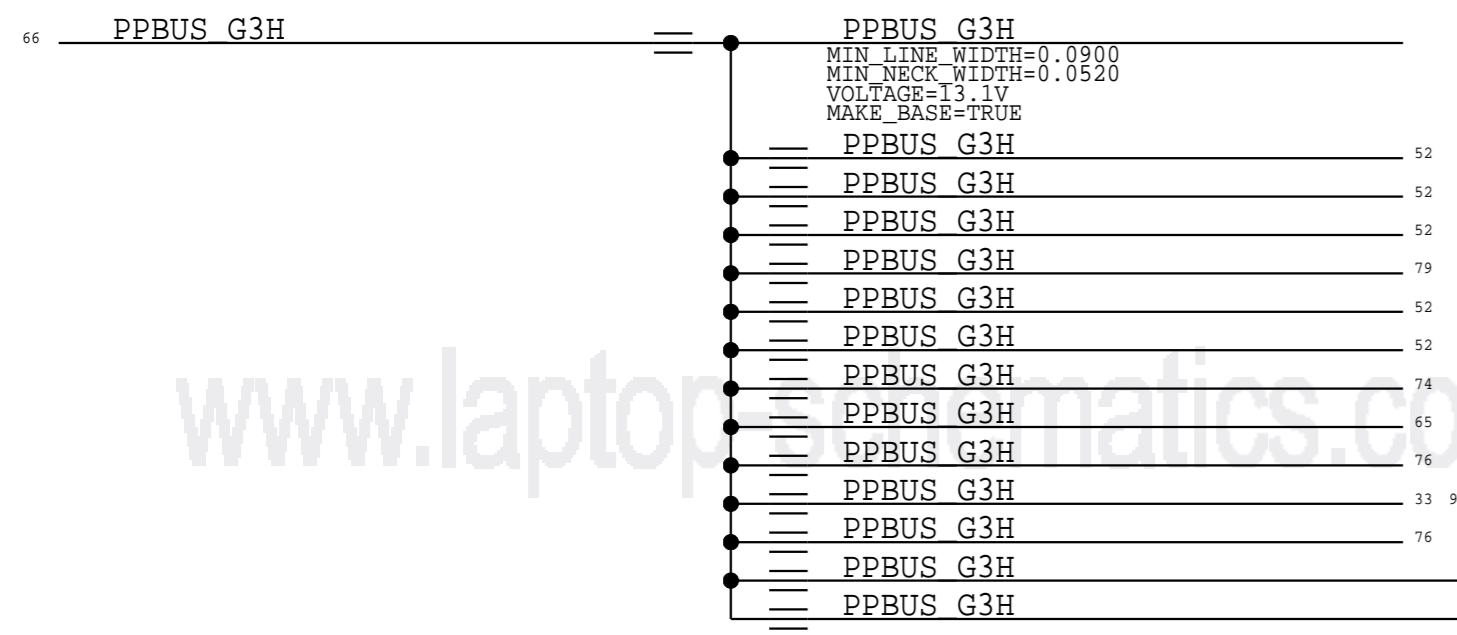
BOM_COST_GROUP=USB-C

| | | | |
|--|--|------------------|-------------|
| PAGE TITLE | | TBT 5V REGULATOR | |
| Apple Inc. | | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I NOT TO REPRODUCE OR PUBLISH IT IN WHOLE OR PART I NOT TO REPRODUCE OR PUBLISH IT IN WHOLE OR PART | | BRANCH | dvt-fab09-0 |
| | | PAGE | 117 OF 145 |
| | | SHEET | 99 OF 119 |

PBUS Rails

IMVP Rails

OV6 Rails



| | | | |
|---|--|-------------------|-------------|
| PAGE TITLE | | Power Aliases - 1 | |
| Apple Inc. | | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: | | BRANCH | dvt-fab09-0 |
| THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: | | PAGE | 120 OF 145 |
| I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE | | SHEET | 100 OF 119 |
| I I NOT TO REPRODUCE OR COPY IT | | | |
| I I I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART | | | |
| I I I I ALL RIGHTS RESERVED | | | |

UNUSED TP ALIASES

UNUSED TP ALIASES

UNUSED SIGNAL ALIAS

| | | | |
|----|------------------------|----|------------------------|
| 83 | NC S3X VSS S | == | NC S3X VSS S |
| 82 | NC S3X VDD S | == | NC S3X VDD S |
| 81 | NC S3X PMIC CTRL 2 | == | NC S3X PMIC CTRL 2 |
| 81 | NC S3X PCIE ATB1 | == | NC S3X PCIE ATB1 |
| 81 | NC S3X PCIE ATB0 | == | NC S3X PCIE ATB0 |
| 81 | NC S3X DT1 | == | NC S3X DT1 |
| 81 | NC S3X DT0 | == | NC S3X DT0 |
| 81 | NC S3X DDR ATO | == | NC S3X DDR ATO |
| 74 | NC PMIC PGG | == | NC PMIC PGG |
| 74 | NC PMIC PGF | == | NC PMIC PGF |
| 74 | NC PMIC PGE | == | NC PMIC PGE |
| 74 | NC PMIC PGD | == | NC PMIC PGD |
| 74 | NC PMIC PGC | == | NC PMIC PGC |
| 88 | NC PICCOLO 24M CLK REQ | == | NC PICCOLO 24M CLK REQ |
| 14 | NC PCH SLP A L | == | NC PCH SLP A L |
| 14 | NC PCH PME L | == | NC PCH PME L |
| 14 | NC PCH LANPHYC | == | NC PCH LANPHYC |
| 14 | NC PCH GPP F9 | == | NC PCH GPP F9 |
| 14 | NC PCH GPP F8 | == | NC PCH GPP F8 |
| 14 | NC PCH GPP F10 | == | NC PCH GPP F10 |
| 16 | NC PCH GPP D4 | == | NC PCH GPP D4 |
| 16 | NC PCH GPP D3 | == | NC PCH GPP D3 |
| 16 | NC PCH GPP D1 | == | NC PCH GPP D1 |
| 14 | NC PCH GPP D0 | == | NC PCH GPP D0 |
| 14 | NC PCH GPD7 | == | NC PCH GPD7 |
| 99 | NC P5VUSBC T PGOOD | == | NC P5VUSBC T PGOOD |
| 34 | NC DPMUX SAK 20 | == | NC DPMUX SAK 20 |
| 34 | NC DPMUX SAK 19 | == | NC DPMUX SAK 19 |
| 34 | NC DPMUX SAK 18 | == | NC DPMUX SAK 18 |
| 34 | NC DPMUX SAK 17 | == | NC DPMUX SAK 17 |
| 34 | NC DPMUX SAK 16 | == | NC DPMUX SAK 16 |
| 34 | NC DPMUX SAK 15 | == | NC DPMUX SAK 15 |
| 34 | NC DPMUX SAK 14 | == | NC DPMUX SAK 14 |

| | | | |
|----|---------------------|----|---------------------|
| 6 | NC CPU RSVD BB69 | == | NC CPU RSVD BB69 |
| 6 | NC CPU RSVD BB68 | == | NC CPU RSVD BB68 |
| 6 | NC CPU RSVD BA70 | == | NC CPU RSVD BA70 |
| 6 | NC CPU RSVD BA68 | == | NC CPU RSVD BA68 |
| 6 | NC CPU RSVD AW71 | == | NC CPU RSVD AW71 |
| 6 | NC CPU RSVD AW70 | == | NC CPU RSVD AW70 |
| 6 | NC CPU RSVD AK13 | == | NC CPU RSVD AK13 |
| 6 | NC CPU RSVD AK12 | == | NC CPU RSVD AK12 |
| 9 | NC CPU NCTFVSS C1 | == | NC CPU NCTFVSS C1 |
| 9 | NC CPU NCTFVSS BB70 | == | NC CPU NCTFVSS BB70 |
| 9 | NC CPU NCTFVSS BA71 | == | NC CPU NCTFVSS BA71 |
| 9 | NC CPU NCTFVSS BA1 | == | NC CPU NCTFVSS BA1 |
| 9 | NC CPU NCTFVSS B71 | == | NC CPU NCTFVSS B71 |
| 9 | NC CPU NCTFVSS AV1 | == | NC CPU NCTFVSS AV1 |
| 9 | NC CPU NCTFVSS A70 | == | NC CPU NCTFVSS A70 |
| 9 | NC CPU NCTFVSS A5 | == | NC CPU NCTFVSS A5 |
| 6 | NC CPU BB5 | == | NC CPU BB5 |
| 6 | NC CPU BB3 | == | NC CPU BB3 |
| 6 | NC CPU AY4 | == | NC CPU AY4 |
| 6 | NC CPU AU5 | == | NC CPU AU5 |
| 6 | NC CPU AT5 | == | NC CPU AT5 |
| 13 | NC CPU MSM L | == | NC CPU MSM L |
| 28 | NC USBC XA RESET L | == | NC USBC XA RESET L |
| 34 | NC USBC TB RESET L | == | NC USBC TB RESET L |

UNUSED SIGNALS

| | | | | | |
|-----|--------------------------|----|------|--------------------------|---------|
| 14 | NC PCH SLP WLAN L | == | TRUE | NC PCH SLP WLAN L | 105 |
| 102 | NC SPI CS1 L | == | TRUE | NC SPI CS1 L | 102 105 |
| 102 | NC SPI CS2 L | == | TRUE | NC SPI CS2 L | 102 105 |
| 102 | NC SPI CS1 L | == | TRUE | NC SPI CS1 L | 102 105 |
| 102 | NC SPI CS2 L | == | TRUE | NC SPI CS2 L | 102 105 |
| 15 | NC PCIE CAMERA D2R N | == | TRUE | NC PCIE CAMERA D2R N | 105 |
| 15 | NC PCIE CAMERA D2R P | == | TRUE | NC PCIE CAMERA D2R P | 105 |
| 15 | NC PCIE CAMERA R2D C N | == | TRUE | NC PCIE CAMERA R2D C N | 105 |
| 15 | NC PCIE CAMERA R2D C P | == | TRUE | NC PCIE CAMERA R2D C P | 105 |
| 15 | NC PCIE CLK100M CAMERA N | == | TRUE | NC PCIE CLK100M CAMERA N | 105 |
| 15 | NC PCIE CLK100M CAMERA P | == | TRUE | NC PCIE CLK100M CAMERA P | 105 |
| 15 | NC USB EXTA N | == | TRUE | NC USB EXTA N | TRUE |
| 15 | NC USB EXTA P | == | TRUE | NC USB EXTA P | TRUE |
| 15 | NC USB EXTB N | == | TRUE | NC USB EXTB N | TRUE |
| 15 | NC USB EXTB P | == | TRUE | NC USB EXTB P | TRUE |
| 6 | NC XDP BPM L<1> | == | TRUE | NC XDP BPM L<1> | TRUE |
| 6 | NC XDP BPM L<2> | == | TRUE | NC XDP BPM L<2> | TRUE |
| 6 | NC XDP BPM L<3> | == | TRUE | NC XDP BPM L<3> | TRUE |
| 15 | NC USB3 EXTB D2R N | == | TRUE | NC USB3 EXTB D2R N | TRUE |
| 15 | NC USB3 EXTB D2R P | == | TRUE | NC USB3 EXTB D2R P | TRUE |
| 15 | NC USB3 EXTB R2D C N | == | TRUE | NC USB3 EXTB R2D C N | TRUE |
| 15 | NC USB3 EXTB R2D C P | == | TRUE | NC USB3 EXTB R2D C P | TRUE |

| | | | | | |
|----|--------------|----|----------------|-----------|--------------|
| 86 | NC ANIO NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANIO NCE4 |
| 86 | NC ANIO NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANIO NCE5 |
| 86 | NC ANIO NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANIO NCE6 |
| 86 | NC ANIO NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANIO NCE7 |
| 86 | NC ANI1 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI1 NCE4 |
| 86 | NC ANI1 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI1 NCE5 |
| 86 | NC ANI1 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI1 NCE6 |
| 86 | NC ANI1 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI1 NCE7 |
| 86 | NC ANI2 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI2 NCE4 |
| 86 | NC ANI2 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI2 NCE5 |
| 86 | NC ANI2 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI2 NCE6 |
| 86 | NC ANI2 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI2 NCE7 |
| 86 | NC ANI3 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI3 NCE4 |
| 86 | NC ANI3 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI3 NCE5 |
| 86 | NC ANI3 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI3 NCE6 |
| 86 | NC ANI3 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI3 NCE7 |
| 87 | NC ANI4 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI4 NCE4 |
| 87 | NC ANI4 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI4 NCE5 |
| 87 | NC ANI4 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI4 NCE6 |
| 87 | NC ANI4 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI4 NCE7 |
| 87 | NC ANI5 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI5 NCE4 |
| 87 | NC ANI5 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI5 NCE5 |
| 87 | NC ANI5 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI5 NCE6 |
| 87 | NC ANI5 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI5 NCE7 |
| 87 | NC ANI6 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI6 NCE4 |
| 87 | NC ANI6 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI6 NCE5 |
| 87 | NC ANI6 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI6 NCE6 |
| 87 | NC ANI6 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI6 NCE7 |
| 87 | NC ANI7 NCE4 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI7 NCE4 |
| 87 | NC ANI7 NCE5 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI7 NCE5 |
| 87 | NC ANI7 NCE6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI7 NCE6 |
| 87 | NC ANI7 NCE7 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI7 NCE7 |
| 86 | NC ANI1 RNB | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI1 RNB |
| 86 | NC ANI3 RNB | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI3 RNB |
| 87 | NC ANI5 RNB | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI5 RNB |
| 87 | NC ANI7 RNB | == | MAKE_BASE=TRUE | NO_TEST=1 | NC ANI7 RNB |

S3X Aliasing

| | | | | | |
|----|-------------------|----|----------------|-----------|-------------------|
| 81 | NC S3X GPIO1 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC S3X GPIO1 |
| 81 | NC S3X BOOTSTRAP6 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC S3X BOOTSTRAP6 |
| 81 | NC S3X BOOTSTRAP1 | == | MAKE_BASE=TRUE | NO_TEST=1 | NC S3X BOOTSTRAP1 |
| 19 | SSD_CLKREQ L | == | SSD_CLKREQ L | 91 | |
| 14 | SSD_SR_EN L | == | SSD_SR_EN L | 91 104 | |

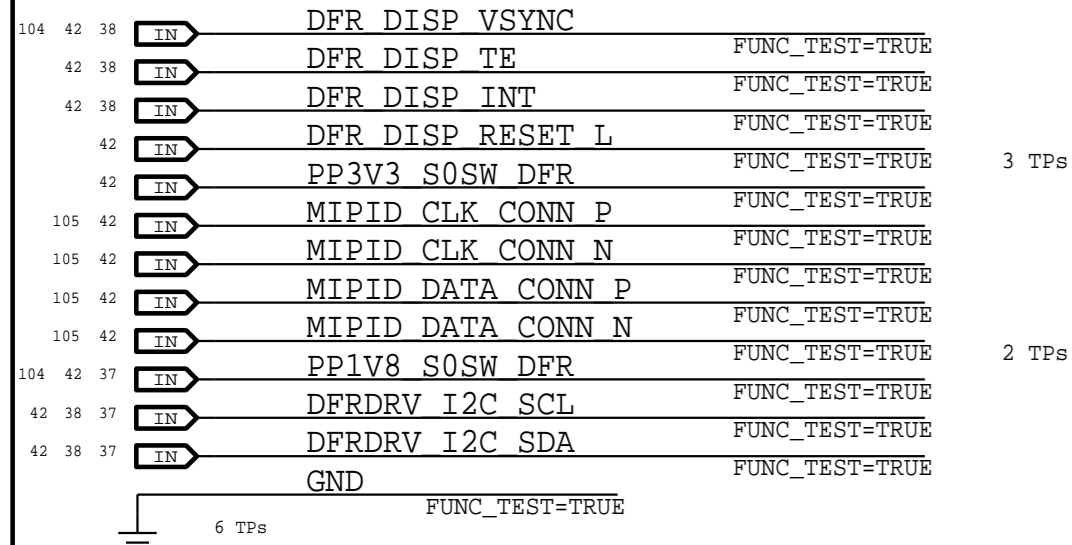
EPD PANEL

| | | | | | |
|----|--------------|----|------|--------------|--------|
| 79 | I2C_BKLT_SCL | == | TRUE | I2C_BKLT_SCL | 80 104 |
| 79 | I2C_BKLT_SDA | == | TRUE | I2C_BKLT_SDA | 80 104 |

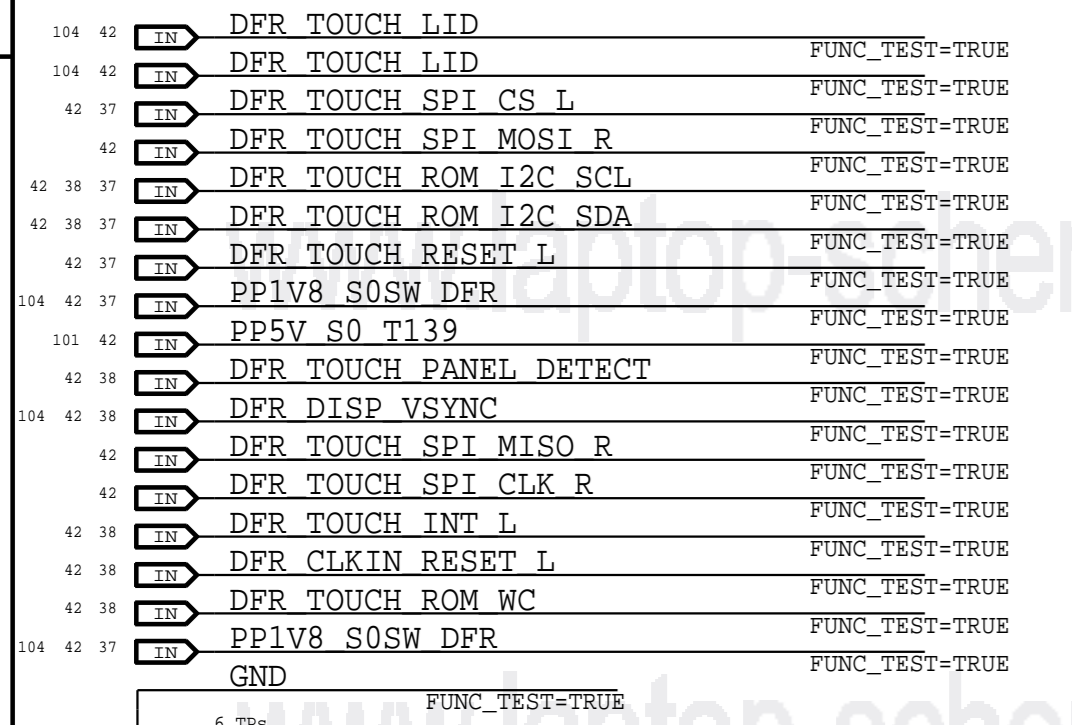
| | | | |
|---|--|-----------------------------|-----------|
| SYNC_MASTER=SHART_J44 | | SYNC_DATE=11/19/2012 | |
| PAGE TITLE | | | |
| Signal Aliases | | | |
| | | DRAWING NUMBER 051-00777 | STEP D |
| | | REVISION 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: 1 TO MAINTAIN THIS DOCUMENT IN CONFIDENCE 11 NOT TO REPRODUCE OR COPY IT 111 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART 1111 ALL RIGHTS RESERVED | | BRANCH dvt-fab09-0 | |
| | | PAGE 122 OF 145 | |
| | | SHEET 102 OF 119 | |
| | | | |

Functional Test Points

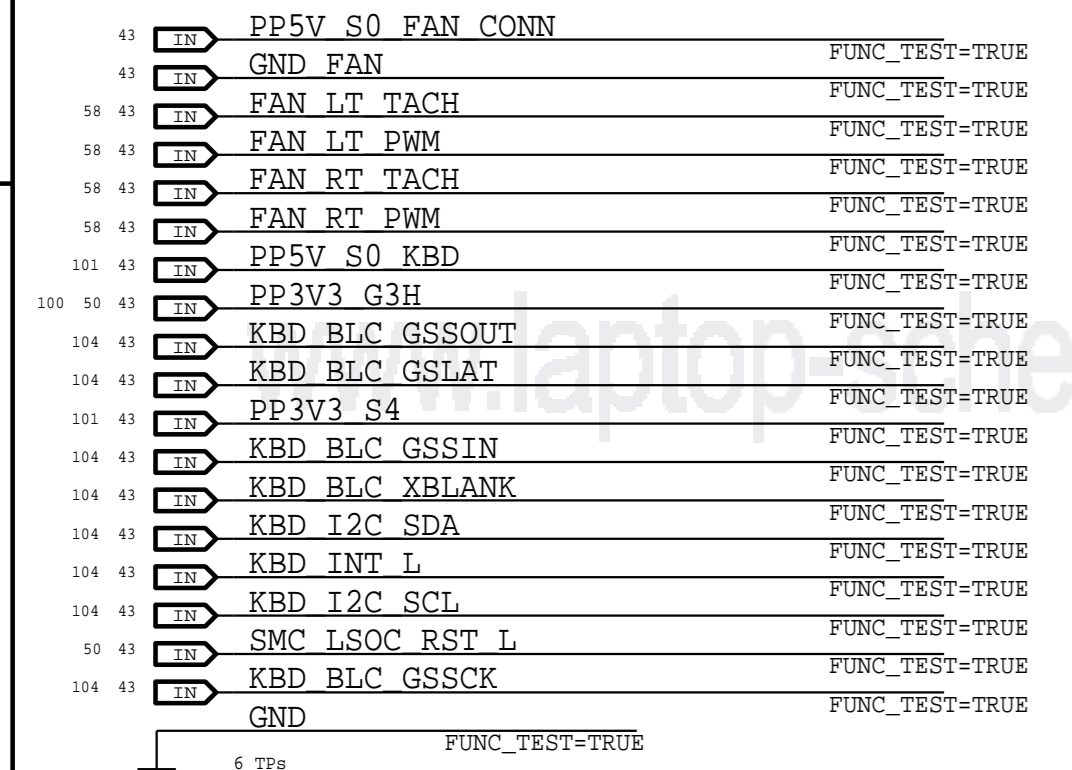
J4401 - DFR Display Connector



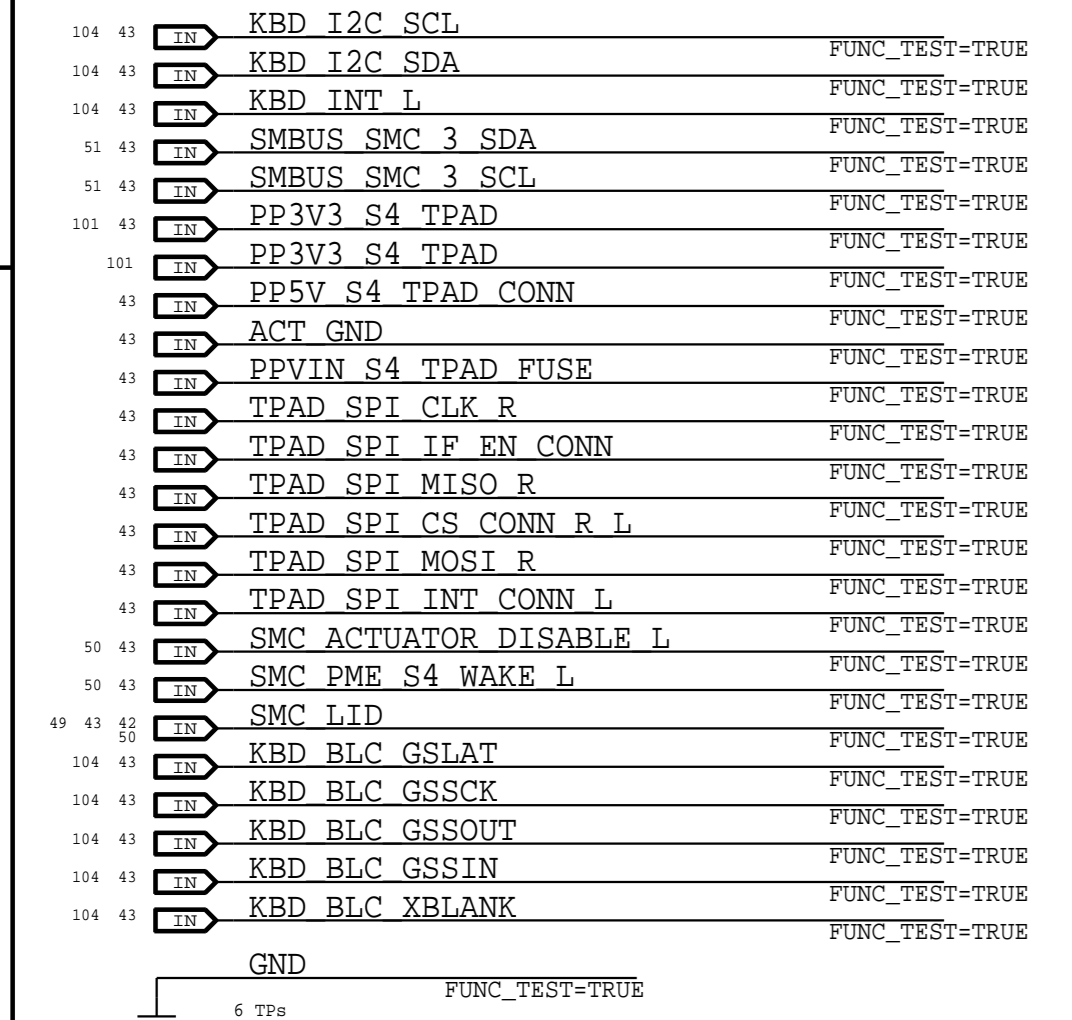
J4402 - DFR Touch Connector



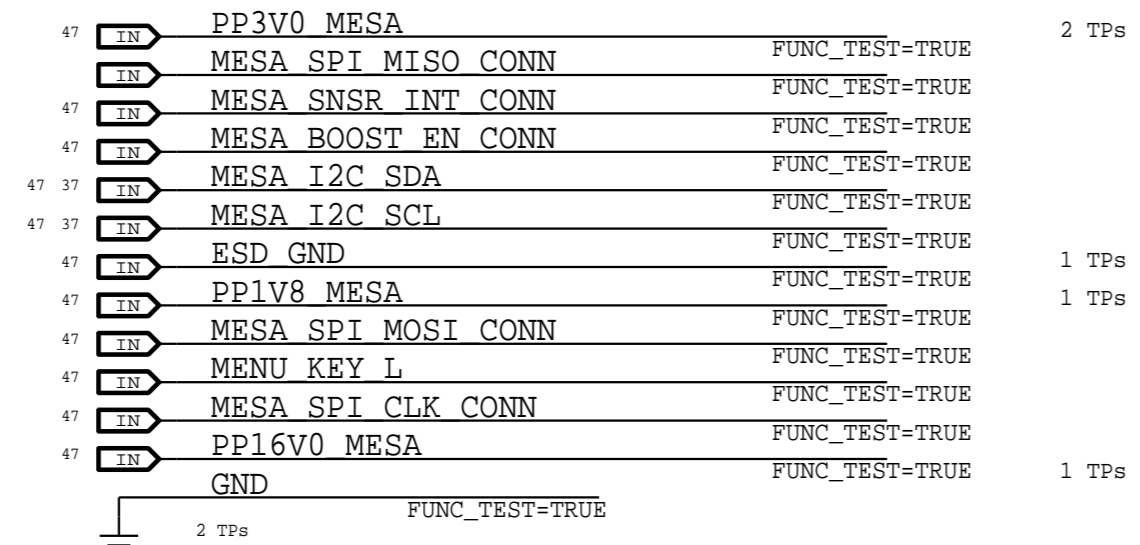
J4500 - Keyboard Connector



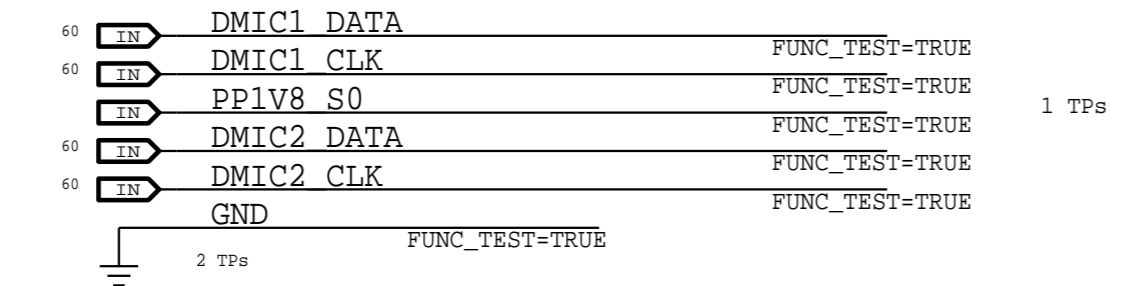
J4501 - Trackpad Connector



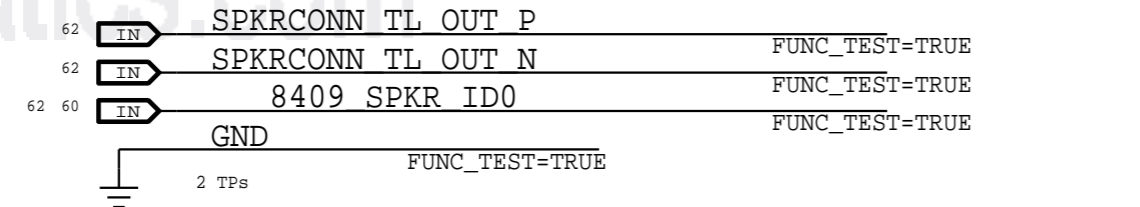
J4900 - Mesa Connector



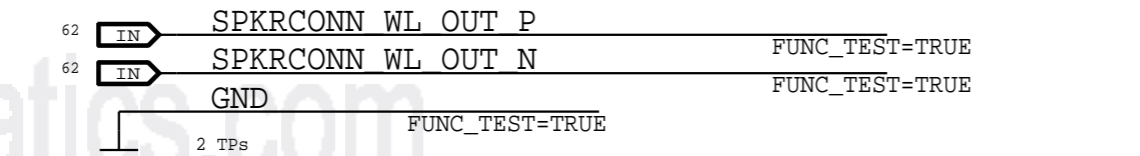
J6200 - MIC Connector



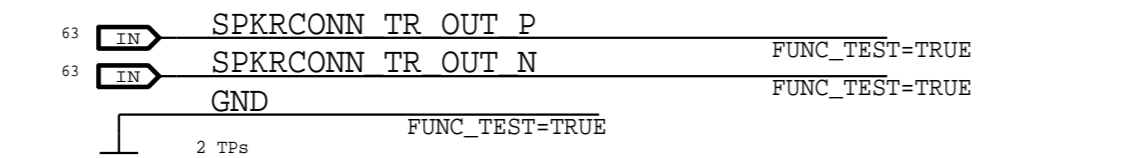
J6410 - Left Tweeter Connector



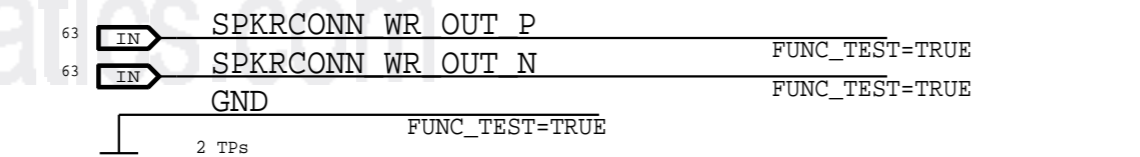
J6430 - Left Woofer Connector



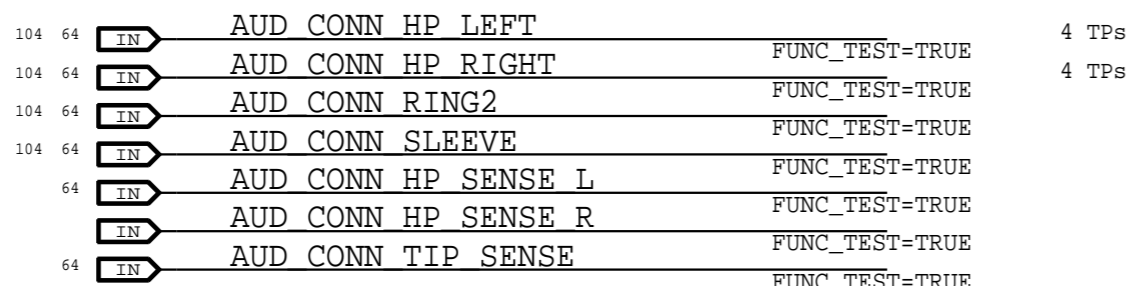
J6500 - Right Tweeter Connector



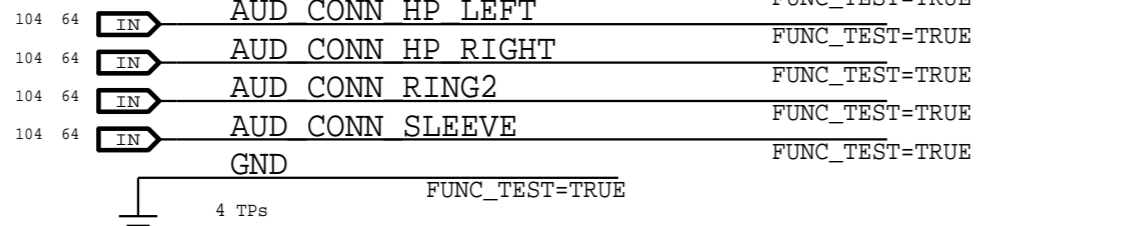
J6550 - Right Woofer Connector



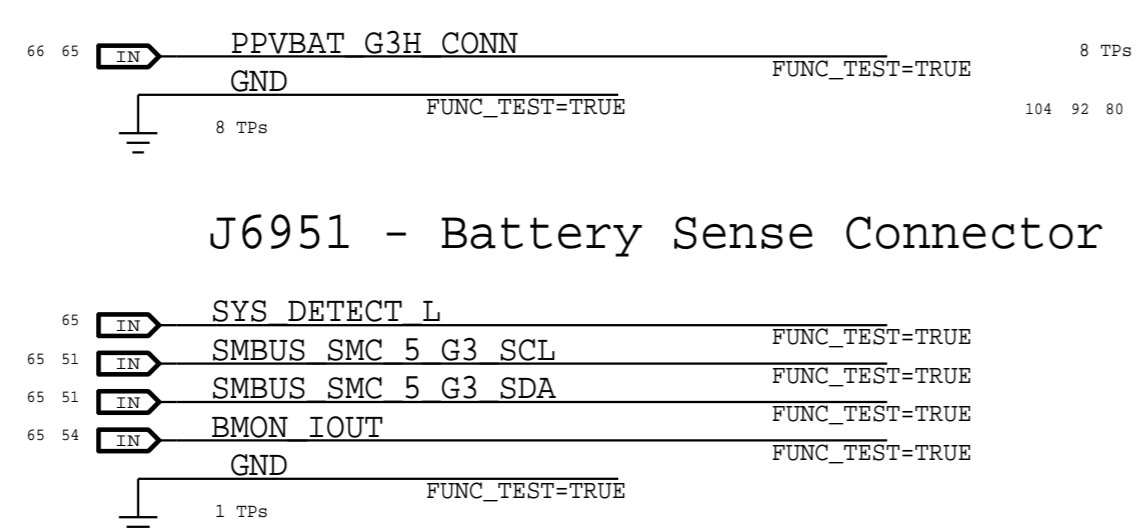
J6600 - Audio Jack Connector



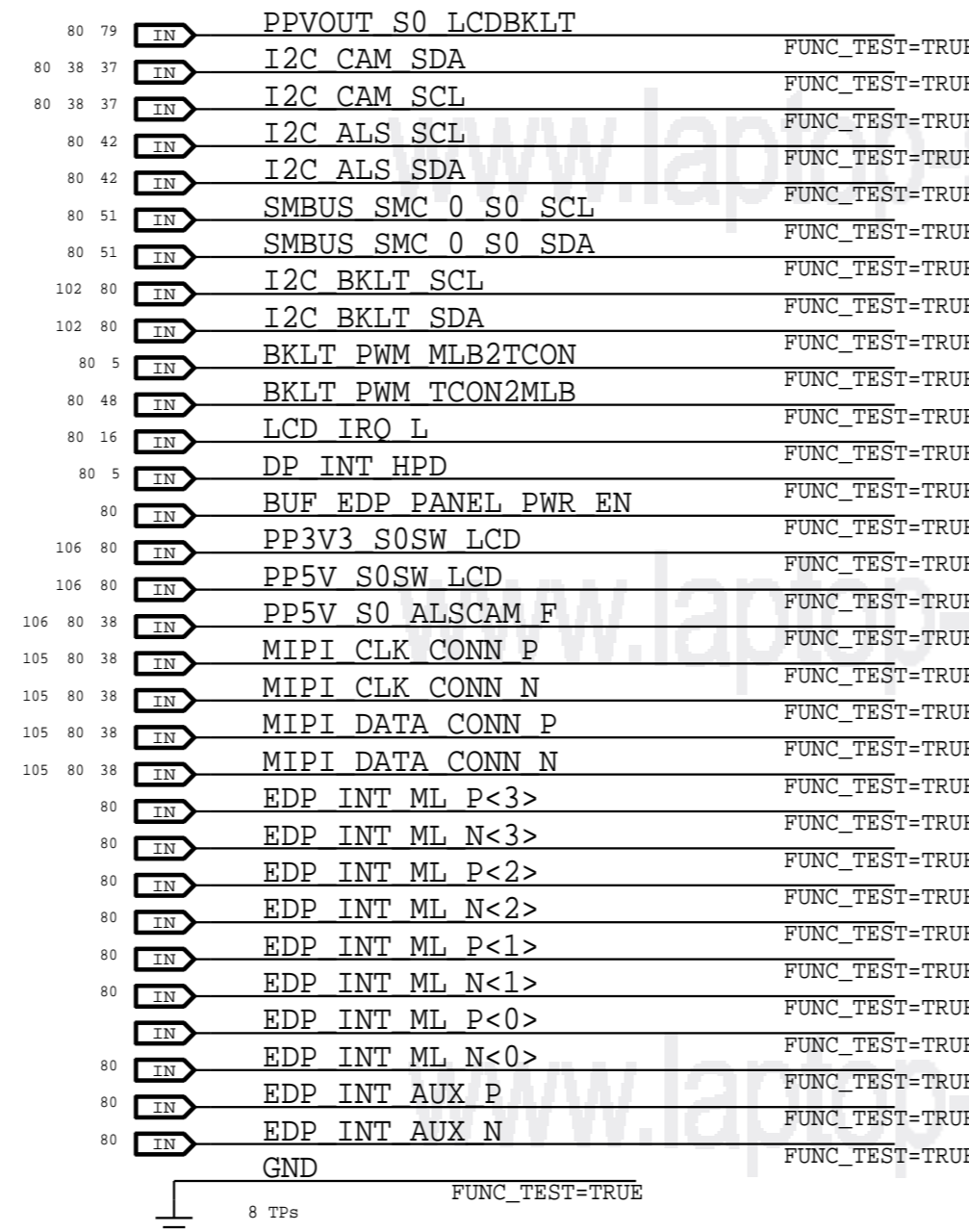
J6950 - Battery Connector



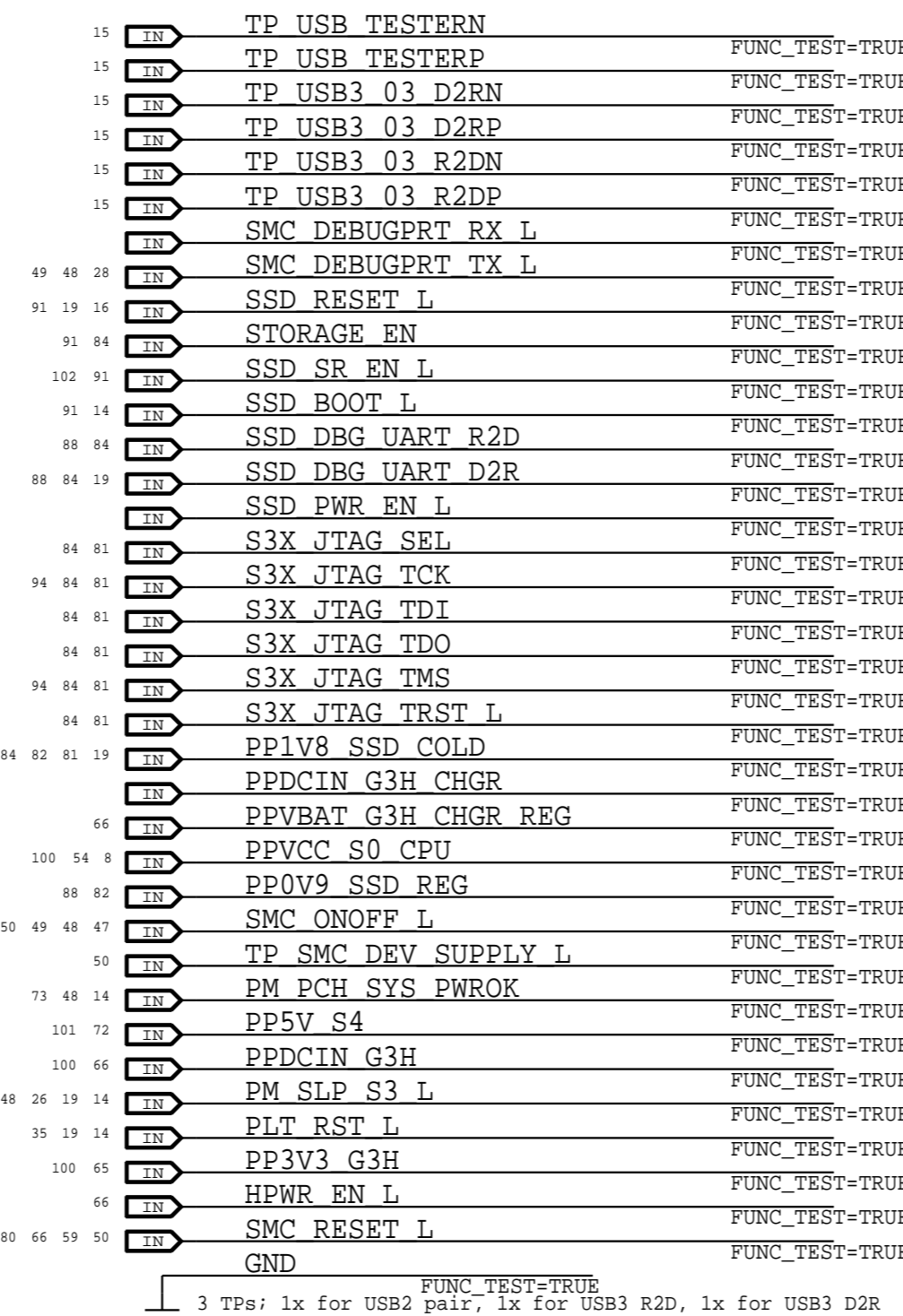
J6951 - Battery Sense Connector



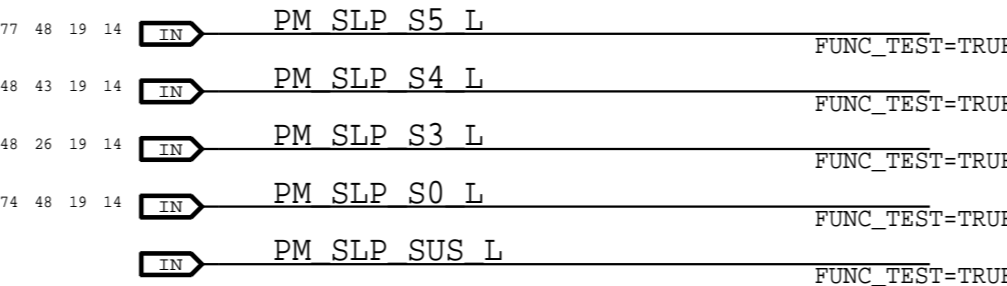
J8500 - eDP Connector



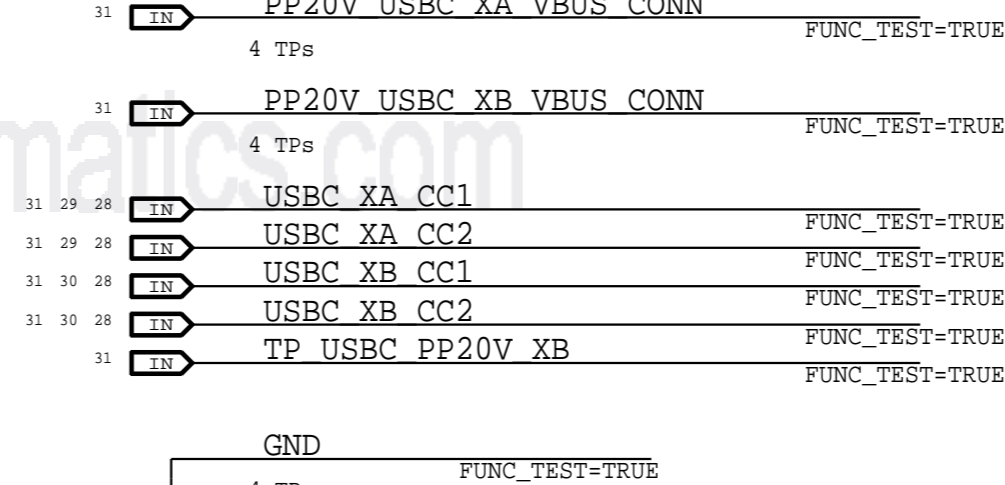
Probe Block Grid - WiPass and NAND Rack



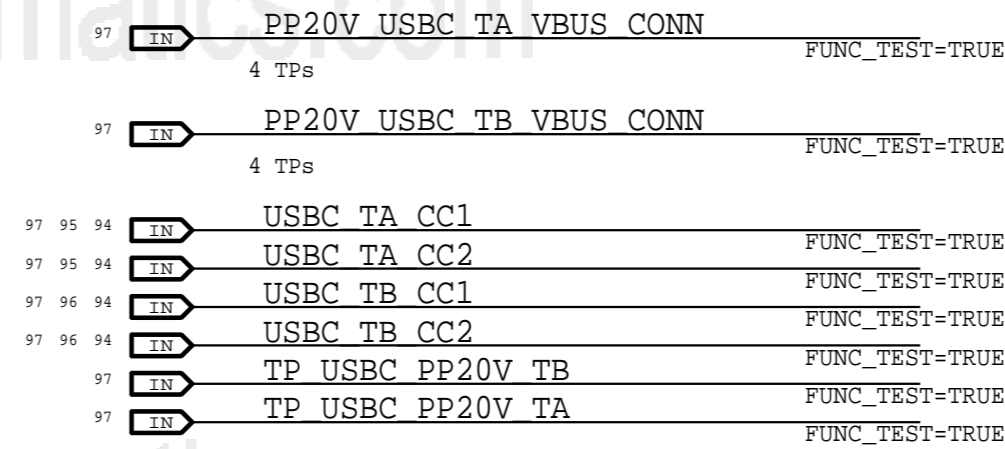
Debug LEDs



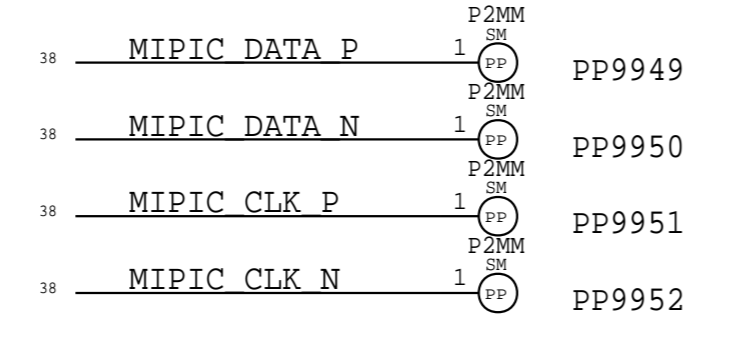
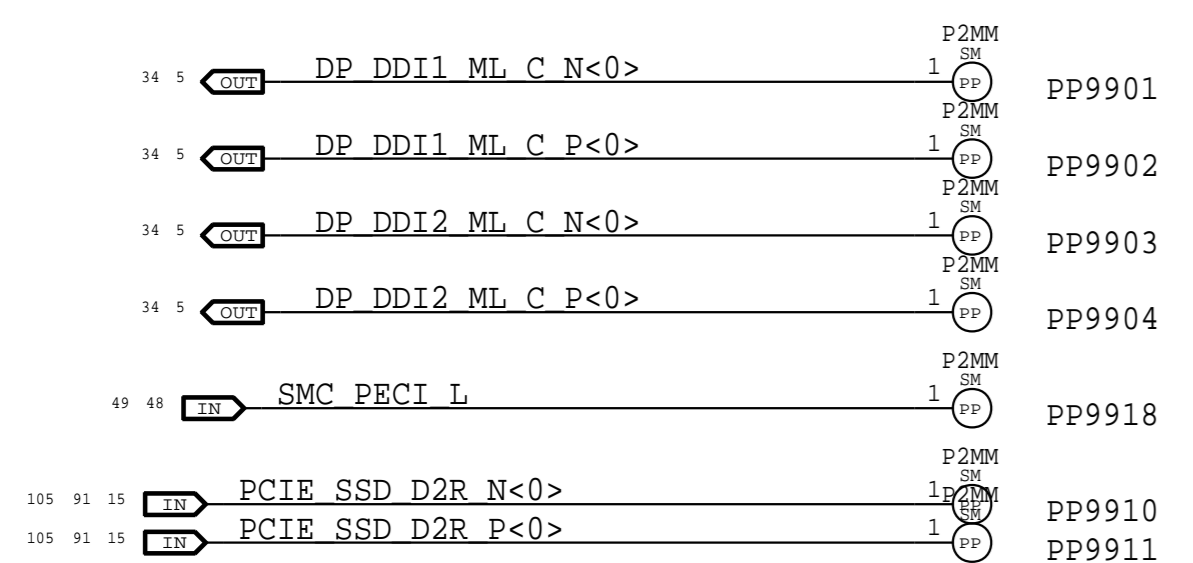
J3300 - Left USB-C Connector



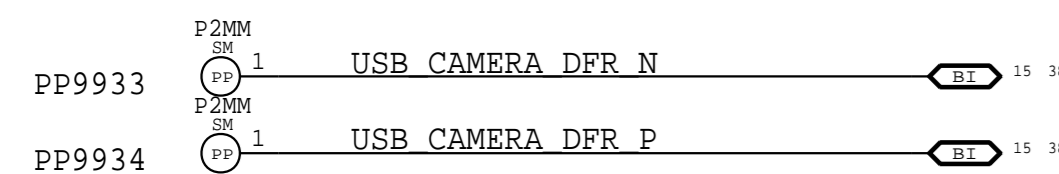
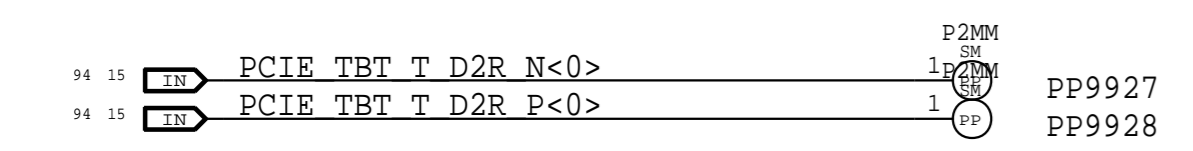
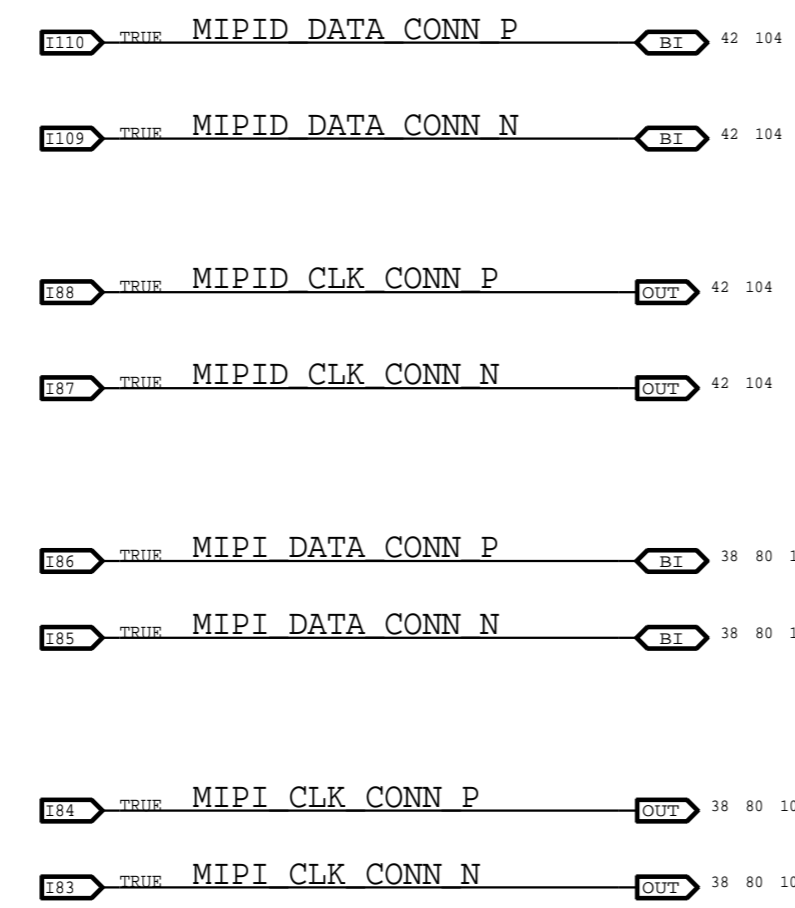
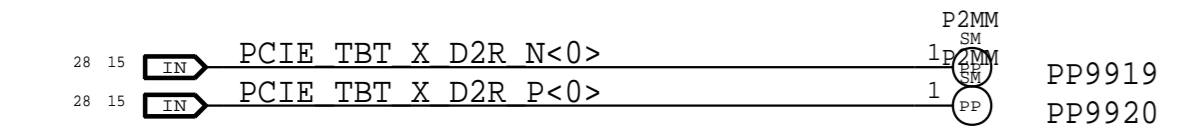
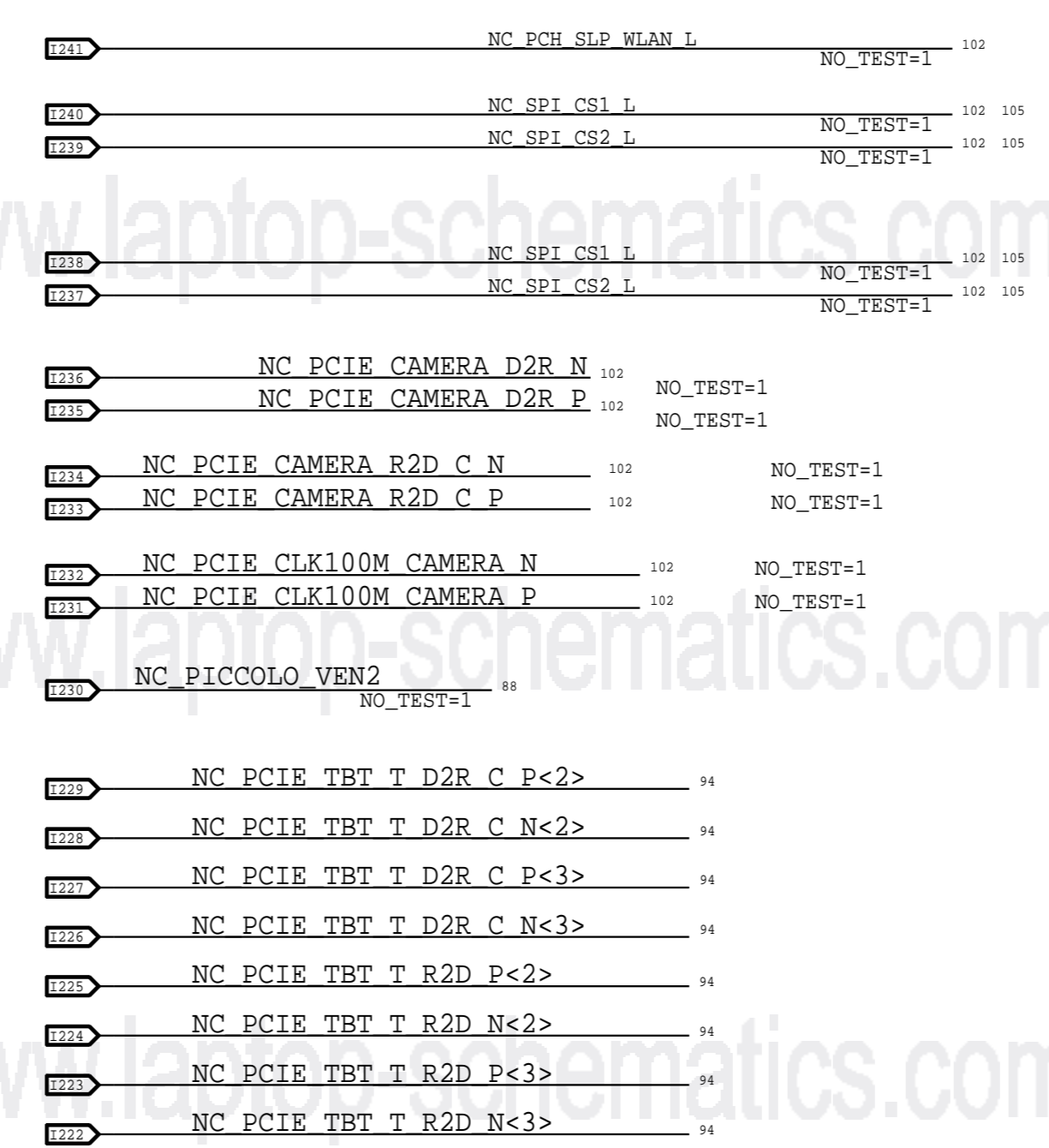
JB500 - Right USB-C Connector



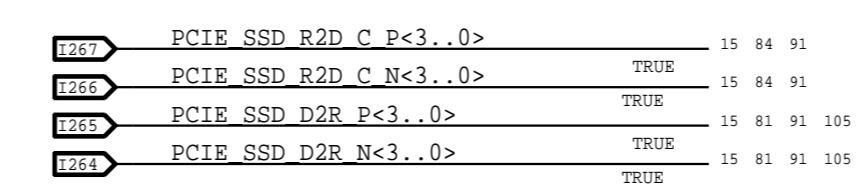
Header information including SYNC_MASTER=YHARTANTO_J44, SYNC_DATE=12/18/2012, PAGE TITLE, ICT FCT 1, Apple Inc. logo, and a table with columns for DRAWING NUMBER (051-00777), STR (D), REVISION (9.0.0), BRANCH (dvt-fab09-0), PAGE (124 OF 145), and SHEET (104 OF 119). It also contains a NOTICE OF PROPRIETARY PROPERTY.



NO_TESTS

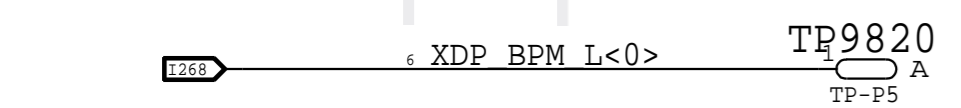
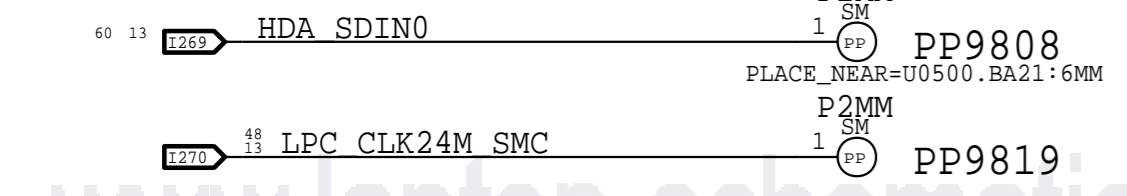
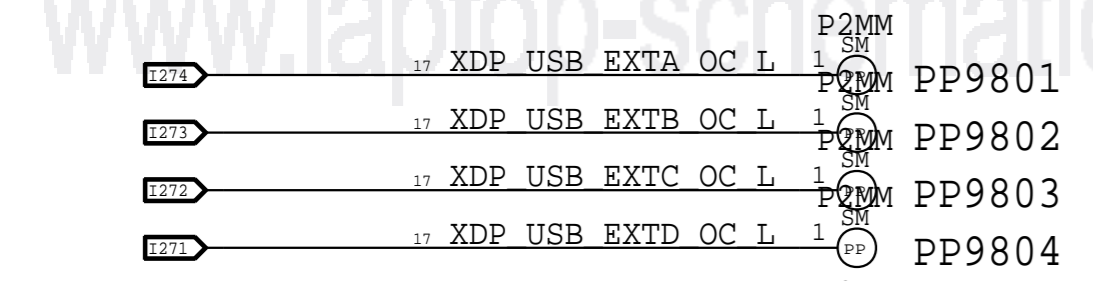
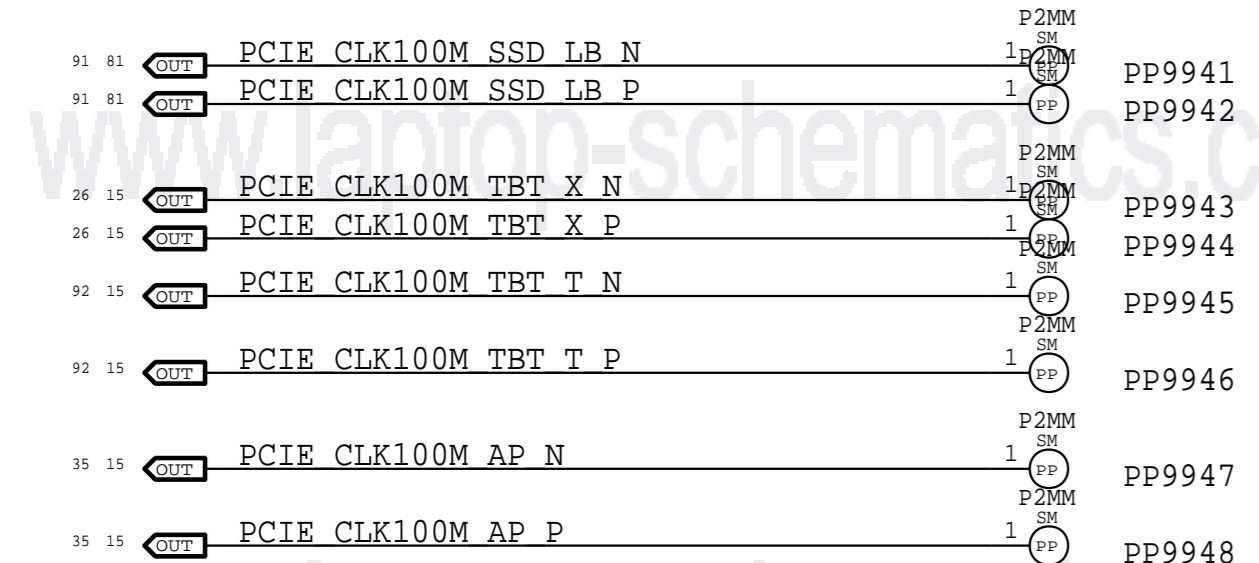
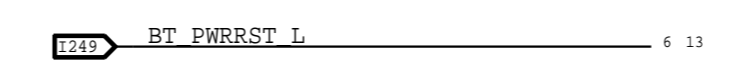


High Speed NO_TEST

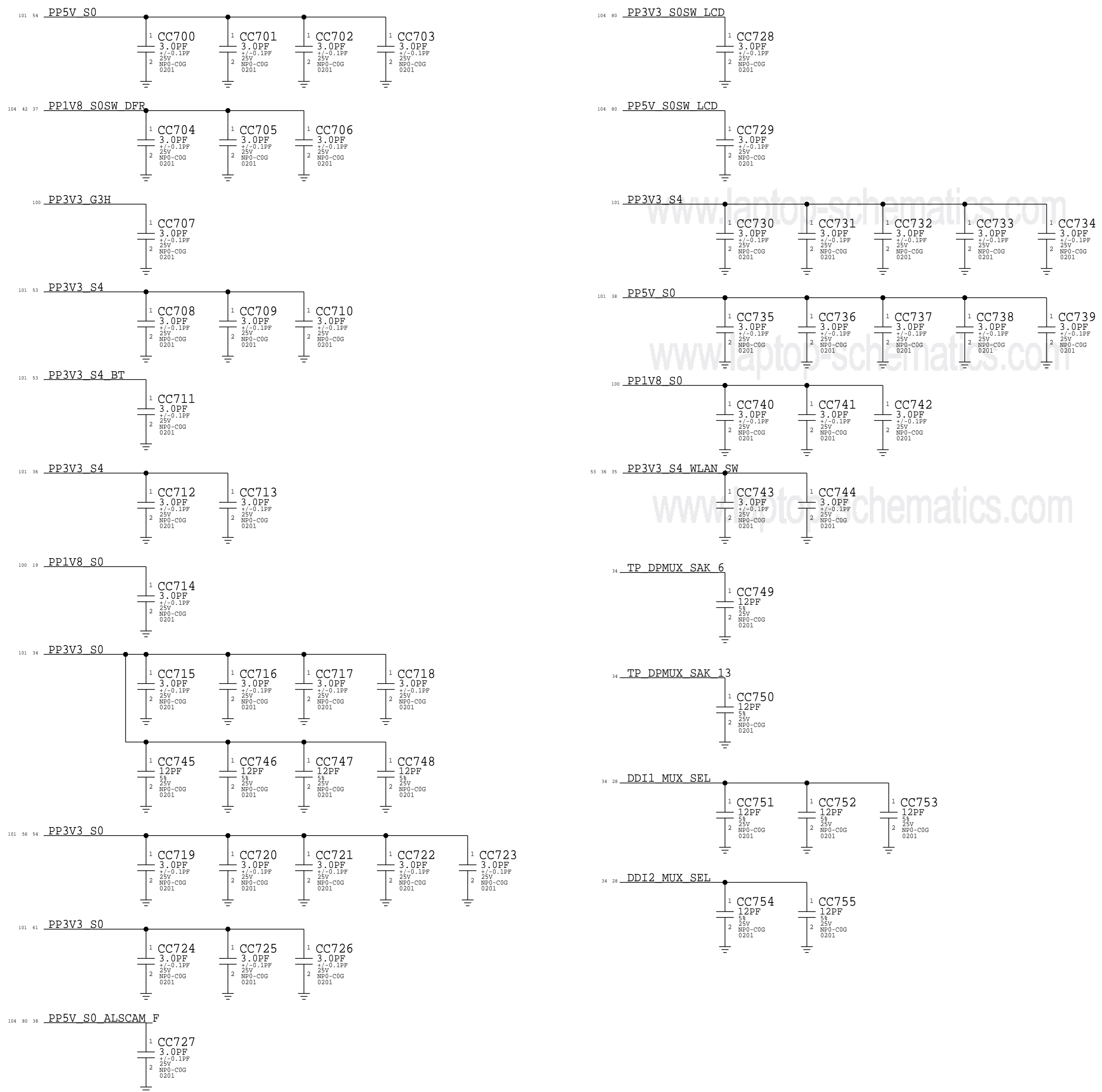


Unused nets with offpage

(Nets with offpages not used on this project)



| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=12/18/2012 | |
| PAGE TITLE | | | |
| ICT FCT 2 | | | |
| | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 125 OF 145 |
| | | SHEET | 105 OF 119 |
| | | | |



| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=01/09/2013 | |
| PAGE TITLE | | | |
| Desense Capacitors | | | |
| | DRAWING NUMBER | 051-00777 | STEP |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 127 OF 145 |
| | | SHEET | 106 OF 119 |
| | | | |

8

7

6

5

4

3

2

1

D

D

C

C


B

B

A

A

SYNC_MASTER=J79_RIO SYNC_DATE=06/18/2015

| | | | |
|---|----------------|-----------|-------------|
| PAGE TITLE | | Empty | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 129 OF 145 |
| | | SHEET | 107 OF 119 |

8

7

6

5

4

3

2

1

8

7

6

<https://shop61976717.taobao.com> QQ 53013942

5

3

2

1

J79 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

D

D

C


C

B

B

A

A

| | | | |
|---|----------------|----------------------|-----------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=12/14/2012 | |
| PAGE TITLE | | | |
| PCB Rule Definitions | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE D |
| | REVISION | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 130 OF 145 | |
| | SHEET | 108 OF 119 | |

8

7

6

5

4

3

2

1

CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |
| CPU_27P4S | * | =27P4_OHM_SE | =27P4_OHM_SE | =27P4_OHM_SE | =27P4_OHM_SE | 7 MIL | 7 MIL |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_VCCSENSE | * | 25 MIL | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_08MIL | * | 0.203 MM | ? |
| CPU_12MIL | * | 0.305 MM | ? |
| CPU_18MIL | * | 0.457 MM | ? |
| CPU_25MIL | * | 0.635 MM | ? |

CPU Signal Properties

| ELECTRICAL CONST SET | NET TYPE | |
|----------------------|----------|---------|
| | PHYSICAL | SPACING |
| | | |

www.laptop-schematics.com

| | | | |
|---|------------|----------------------|-------------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=01/13/2013 | |
| PAGE TITLE | | | |
| CPU Constraints | | | |
| | Apple Inc. | DRAWING NUMBER | 051-00777 |
| | | REVISION | 9.0.0 |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 131 OF 145 |
| | | SHEET | 109 OF 119 |

Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_40S | * | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE | =40_OHM_SE |
| MEM_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE |
| MEM_70D | * | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF | =70_OHM_DIFF |
| MEM_75D | * | =75_OHM_DIFF | =75_OHM_DIFF | =75_OHM_DIFF | =75_OHM_DIFF | =75_OHM_DIFF | =75_OHM_DIFF |
| MEM_80D | * | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF |

Spacing Rule Sets

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|-------------------|-------|----------------------|--------|
| MEM_DATA2SELF | * | =4x_DIELECTRIC | ? |
| MEM_DQS2OWNDATA | * | =6x_DIELECTRIC | ? |
| MEM_CMD2CMD | * | =6x_DIELECTRIC | ? |
| MEM_CMD2CTL | * | =6x_DIELECTRIC | ? |
| MEM_CTL2CTL | * | =6x_DIELECTRIC | ? |
| MEM_CLK2CLK | * | =12x_DIELECTRIC | ? |
| MEM_DATA2OTHERMEM | * | =16x_DIELECTRIC | ? |
| MEM_2OTHERMEM | * | =8x_DIELECTRIC | ? |
| MEM_2PWR | * | =4x_DIELECTRIC | ? |
| MEM_2GND | * | =4x_DIELECTRIC | ? |
| MEM_2OTHER | * | =12x_DIELECTRIC | ? |
| MEM_12MIL | * | 0.305 MM | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|-------------------|-------|----------------------|--------|
| MEM_DATA2SELF_B | * | =1.5x_DIELECTRIC | ? |
| MEM_DQS2OWNDATA_B | * | =1.5x_DIELECTRIC | ? |
| MEM_CMD2CMD_B | * | =1.5x_DIELECTRIC | ? |
| MEM_CMD2CTL_B | * | =1.5x_DIELECTRIC | ? |
| MEM_CTL2CTL_B | * | =1.5x_DIELECTRIC | ? |
| MEM_CLK2CLK_B | * | =1.5x_DIELECTRIC | ? |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_*_DQBYTE_* | * | * | MEM_2OTHER |
| MEM_*_DQS_* | * | * | MEM_2OTHER |
| MEM_CMD | * | * | MEM_2OTHER |
| MEM_CTL | * | * | MEM_2OTHER |
| MEM_CLK | * | * | MEM_2OTHER |
| MEM_* | MEM_* | * | MEM_2OTHERMEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_*_DQBYTE_* | =SAME | * | MEM_DATA2SELF |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|-------------------|
| MEM_*_DQBYTE_* | MEM_* | * | MEM_DATA2OTHERMEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD | MEM_CMD | * | MEM_CMD2CMD |
| MEM_CMD | MEM_CTL | * | MEM_CMD2CTL |
| MEM_CTL | MEM_CTL | * | MEM_CTL2CTL |
| MEM_CLK | MEM_CLK | * | MEM_CLK2CLK |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_A_DQS_0 | MEM_A_DQBYTE_0 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_1 | MEM_A_DQBYTE_1 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_2 | MEM_A_DQBYTE_2 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_3 | MEM_A_DQBYTE_3 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_4 | MEM_A_DQBYTE_4 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_5 | MEM_A_DQBYTE_5 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_6 | MEM_A_DQBYTE_6 | * | MEM_DQS2OWNDATA |
| MEM_A_DQS_7 | MEM_A_DQBYTE_7 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_0 | MEM_B_DQBYTE_0 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_1 | MEM_B_DQBYTE_1 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_2 | MEM_B_DQBYTE_2 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_3 | MEM_B_DQBYTE_3 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_4 | MEM_B_DQBYTE_4 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_5 | MEM_B_DQBYTE_5 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_6 | MEM_B_DQBYTE_6 | * | MEM_DQS2OWNDATA |
| MEM_B_DQS_7 | MEM_B_DQBYTE_7 | * | MEM_DQS2OWNDATA |

Memory Net Properties

| ELECTRICAL CONST SET | NET TYPE | |
|----------------------|----------|---------|
| | PHYSICAL | SPACING |
| | | |

Memory to Power Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_PWR | MEM_* | * | MEM_2PWR |
| MEM_PWR | * | * | DEFAULT |

Memory to GND Spacing


| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| GND | MEM_* | * | MEM_2GND |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| MEM_70D | BGA_MEM | MEM_80D |
| MEM_40S | BGA_MEM | MEM_45S |

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

PAGE TITLE

Memory Constraints

| | | |
|---|----------------|------|
|  Apple Inc. | DRAWING NUMBER | STEP |
| | 051-00777 | D |
| REVISION | | |
| 9.0.0 | | |
| BRANCH | | |
| dvt-fab09-0 | | |
| PAGE | | |
| 133 OF 145 | | |
| SHEET | | |
| 111 OF 119 | | |

NOTICE OF PROPRIETARY PROPERTY:
 THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:
 I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
 I1 NOT TO REPRODUCE OR COPY IT
 I2 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
 I4 ALL RIGHTS RESERVED

Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| TBT_SPI_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| TBT_SPI | * | =2X_DIELECTRIC | ? |

Thunderbolt & DisplayPort Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| TBTDP_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| TBTDP_2SAME | * | =3X_DIELECTRIC | ? |
| TBTDP_TXRX | * | =6X_DIELECTRIC | ? |
| TBTDP_2OTHER | * | =4X_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|------------|----------------------|--------|
| TBTDP_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| TBTDP_TXRX | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| TBTDP_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| TBTDP_* | * | * | TBTDP_2OTHER |
| TBTDP_* | =SAME | * | TBTDP_2SAME |
| TBTDP_TX | *_RX | * | TBTDP_TXRX |
| TBTDP_RX | *_TX | * | TBTDP_TXRX |

DisplayPort & HDMI Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DP_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| HDMI_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

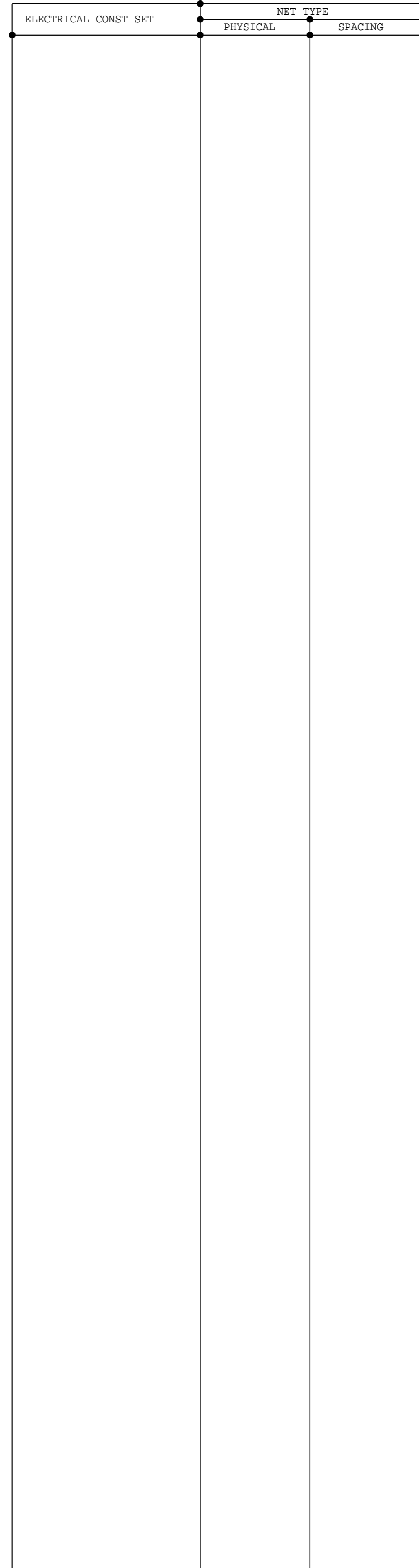
| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| DP_2SAME | * | =3X_DIELECTRIC | ? |
| DP_2OTHER | * | =4X_DIELECTRIC | ? |
| HDMICLK_2OTHER | * | =7X_DIELECTRIC | ? |
| HDMICLK_2DPHDMI | * | =4X_DIELECTRIC | ? |
| HDMIDATA_2SAME | * | =3X_DIELECTRIC | ? |
| HDMIDATA_2OTHER | * | =4X_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|------------|----------------------|--------|
| DP_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| DP_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |
| HDMICLK_2OTHER | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| HDMICLK_2DPHDMI | TOP,BOTTOM | =6X_DIELECTRIC | ? |
| HDMIDATA_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| HDMIDATA_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| HDMI_DATA | * | * | HDMIDATA_2OTHER |
| HDMI_DATA | =SAME | * | HDMIDATA_2SAME |
| HDMI_DATA | TBTDP_TX | * | HDMIDATA_2SAME |
| HDMI_DATA | TBTDP_RX | * | TBTDP_TXRX |
| HDMI_CLK | * | * | HDMICLK_2OTHER |
| HDMI_CLK | HDMI_DATA | * | HDMICLK_2DPHDMI |
| HDMI_CLK | DISPLAYPORT | * | HDMICLK_2DPHDMI |
| HDMI_CLK | TBTDP_TX | * | HDMICLK_2DPHDMI |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| DISPLAYPORT | * | * | DP_2OTHER |
| DISPLAYPORT | =SAME | * | DP_2SAME |
| DISPLAYPORT | HDMI_DATA | * | DP_2SAME |
| DISPLAYPORT | TBTDP_TX | * | DP_2SAME |
| DISPLAYPORT | TBTDP_RX | * | TBTDP_TXRX |

Thunderbolt, DP, HDMI Net Properties



| | | | |
|--|--|----------------------|------------|
| SYNC_MASTER=J79 JACK | | SYNC_DATE=05/19/2015 | |
| PAGE TITLE | | | |
| TBT DP HDMI Constraints | | | |
| | | DRAWING NUMBER | SIZE |
| | | 051-00777 | D |
| | | REVISION | |
| | | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | |
| | | dvt-fab09-0 | |
| | | PAGE | 134 OF 145 |
| | | SHEET | 112 OF 119 |

PCI Express Constraints


| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE OR LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| CLK_PCIE_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| PCIE_2SAME | * | =3X_DIELECTRIC | ? | PCIE_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| PCIE_TXRX | * | =6X_DIELECTRIC | ? | PCIE_TXRX | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| PCIE_2OTHER | * | =4X_DIELECTRIC | ? | PCIE_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |
| PCIE_2CLK | * | =7X_DIELECTRIC | ? | PCIE_2CLK | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| PCIECLK_2OTHER | * | =7X_DIELECTRIC | ? | PCIECLK_2OTHER | TOP,BOTTOM | =10X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| PCIE_* | * | * | PCIE_2OTHER |
| PCIE_* | =SAME | * | PCIE_2SAME |
| PCIE_* | CLK_* | * | PCIE_2CLK |
| CLK_PCIE | * | * | PCIECLK_2OTHER |
| PCIE_TX | *_RX | * | PCIE_TXRX |
| PCIE_RX | *_TX | * | PCIE_TXRX |

PCI Express Properties

| ELECTRICAL CONST SET | NET TYPE | |
|----------------------|----------|---------|
| | PHYSICAL | SPACING |
| | | |

| | | | |
|---|----------------|----------------------|--|
| SYNC_MASTER=J79_JACK | | SYNC_DATE=05/19/2015 | |
| PAGE TITLE | | | |
| PCIe Constraints | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | |
| | REVISION | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 135 OF 145 | |
| | SHEET | 113 OF 119 | |

USB 2 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCH_USB_RBIAIS | * | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| USB_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| USB | * | =4X_DIELECTRIC | ? | USB | TOP,BOTTOM | =6X_DIELECTRIC | ? |
| USB_RBIAIS | * | =6X_DIELECTRIC | ? | USB_RBIAIS | TOP,BOTTOM | =10X_DIELECTRIC | ? |

USB 3 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| USB3_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| USB3_2SAME | * | =3X_DIELECTRIC | ? | USB3_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| USB3_TXRX | * | =6X_DIELECTRIC | ? | USB3_TXRX | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| USB3_2OTHER | * | =4X_DIELECTRIC | ? | USB3_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| USB3_* | * | * | USB3_2OTHER |
| USB3_* | =SAME | * | USB3_2SAME |
| USB3_TX | *_RX | * | USB3_TXRX |
| USB3_RX | *_TX | * | USB3_TXRX |

System Clock Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_25M_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_25M | * | =5X_DIELECTRIC | ? |

SATA Interface Constraints (Not Used)


| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SATA_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| SATA_45SE | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| SATA_2SAME | * | =3X_DIELECTRIC | ? | SATA_2SAME | TOP,BOTTOM | =4X_DIELECTRIC | ? |
| SATA_TXRX | * | =6X_DIELECTRIC | ? | SATA_TXRX | TOP,BOTTOM | =10X_DIELECTRIC | ? |
| SATA_2OTHER | * | =4X_DIELECTRIC | ? | SATA_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| SATA_* | * | * | SATA_2OTHER |
| SATA_* | =SAME | * | SATA_2SAME |
| SATA_TX | *_RX | * | SATA_TXRX |
| SATA_RX | *_TX | * | SATA_TXRX |

USB Constraints

| ELECTRICAL CONST SET | NET TYPE | |
|----------------------|----------|---------|
| | PHYSICAL | SPACING |
| | | |

| | | | |
|--|----------------|----------------------|------|
| SYNC_MASTER=J79_JACK | | SYNC_DATE=05/21/2015 | |
| PAGE TITLE | | | |
| USB Constraints | | | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | BRANCH | dvt-fab09-0 | |
| | PAGE | 136 OF 145 | |
| | SHEET | 114 OF 119 | |

MIPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MIPI_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| MIPI_2OTHER | * | =4X_DIELECTRIC | ? | MIPI_2OTHER | TOP,BOTTOM | =6X_DIELECTRIC | ? |
| MIPI_2CLK | * | =6X_DIELECTRIC | ? | MIPI_2CLK | TOP,BOTTOM | =8X_DIELECTRIC | ? |
| MIPICKL_2OTHER | * | =7X_DIELECTRIC | ? | MIPICKL_2OTHER | TOP,BOTTOM | =10X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MIPI_DATA | * | * | MIPI_2OTHER |
| MIPI_DATA | CLK_MIPI | * | MIPI_2CLK |
| CLK_MIPI | * | * | MIPICKL_2OTHER |

Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| S2_MEM_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |
| S2_MEM_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

Spacing Rule Sets

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| S2_DATA2SELF | * | =2x_DIELECTRIC | ? | S2_DATA2SELF | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2_DQS2OWNDATA | * | =2x_DIELECTRIC | ? | S2_DQS2OWNDATA | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2_CMD2CMD | * | =2x_DIELECTRIC | ? | S2_CMD2CMD | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2_CMD2CTRL | * | =2x_DIELECTRIC | ? | S2_CMD2CTRL | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2_CTRL2CTRL | * | =2x_DIELECTRIC | ? | S2_CTRL2CTRL | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2_2OTHERMEM | * | =4x_DIELECTRIC | ? | S2_2OTHERMEM | TOP,BOTTOM | =6x_DIELECTRIC | ? |
| S2MEM_2PWR | * | =2x_DIELECTRIC | ? | S2MEM_2PWR | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2MEM_2GND | * | =2x_DIELECTRIC | ? | S2MEM_2GND | TOP,BOTTOM | =4x_DIELECTRIC | ? |
| S2MEM_2OTHER | * | =6x_DIELECTRIC | ? | S2MEM_2OTHER | TOP,BOTTOM | =10x_DIELECTRIC | ? |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET | NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|-------------------|-------------------|-----------|------------------|
| S2_MEM_DATA* | * | * | S2MEM_2OTHER | S2_MEM_DQS1 | S2_MEM_DATA1 | * | S2_DQS2OWNDATA |
| S2_MEM_DQS* | * | * | S2MEM_2OTHER | S2_MEM_DQS0 | S2_MEM_DATA0 | * | S2_DQS2OWNDATA |
| S2_MEM_CMD | * | * | S2MEM_2OTHER | | | | |
| S2_MEM_CTRL | * | * | S2MEM_2OTHER | | | | |
| S2_MEM_CLK | * | * | S2MEM_2OTHER | | | | |
| S2_MEM_DATA* | =SAME | * | S2_DATA2SELF | | | | |
| S2_MEM_CMD | S2_MEM_CMD | * | S2_CMD2CMD | | | | |
| S2_MEM_CMD | S2_MEM_CTRL | * | S2_CMD2CTRL | | | | |
| S2_MEM_CTRL | S2_MEM_CTRL | * | S2_CTRL2CTRL | | | | |
| S2_MEM_* | S2_MEM_* | * | S2_2OTHERMEM | | | | |

Memory to Power Spacing


| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| S2_MEM_PWR | S2_MEM_* | * | S2MEM_2PWR |
| S2_MEM_PWR | * | * | DEFAULT |

Memory to GND Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| GND | S2_MEM_* | * | S2MEM_2GND |

Camera Net Properties

| ELECTRICAL CONST SET | NET TYPE | |
|----------------------|----------|---------|
| | PHYSICAL | SPACING |
| | | |

| | | | |
|--|--|----------------------|------------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=01/09/2013 | |
| PAGE TITLE | | | |
|  Apple Inc. | | DRAWING NUMBER | SIZE |
| | | 051-00777 | D |
| | | REVISION | |
| | | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I1 NOT TO REPRODUCE OR COPY IT I11 NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I1V ALL RIGHTS RESERVED | | BRANCH | |
| | | dvt-fab09-0 | |
| | | PAGE | 138 OF 145 |
| | | SHEET | 116 OF 119 |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SENSE_45S | * | =1T01_DIFFPAIR | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | 0.1 MM | 0.1 MM |
| THERM_45S | * | =1T01_DIFFPAIR | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | 0.1 MM | 0.1 MM |
| DIG_AUDIO | * | =1T01_DIFFPAIR | =1T01_DIFFPAIR | =1T01_DIFFPAIR | =1T01_DIFFPAIR | 0.1 MM | 0.1 MM |
| ANL_AUDIO | * | =1T01_DIFFPAIR | 0.1 MM | 0.1 MM | 10 MM | 0.1 MM | 0.1 MM |
| ANL_AUDIO_WIDE | * | =1T01_DIFFPAIR | 0.3 MM | 0.3 MM | 10 MM | 0.1 MM | 0.1 MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SENSE | * | =2X_DIELECTRIC | ? |
| THERM | * | =2X_DIELECTRIC | ? |
| AUDIO | * | =2X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CPU_VCCSENSE | GND | * | GND_P2MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND | * | =STANDARD | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CLK_PCIE | GND | * | GND_P2MM |
| GND | PCIE_* | * | GND_P2MM |
| GND | SATA_* | * | GND_P2MM |
| USB | GND | * | GND_P2MM |
| CLK_PCIE | SB_POWER | * | PWR_P2MM |
| SB_POWER | SATA_* | * | PWR_P2MM |
| USB | SB_POWER | * | PWR_P2MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND_P2MM | * | 0.20 MM | 1000 |
| PWR_P2MM | * | 0.20 MM | 1000 |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|----------------------|--------|-----------------------|--------------------|----------------------|---------------------|----------------------|-------------------|
| MEM_45S OVERRIDE | * | OVERRIDE | OVERRIDE | 0.070 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_40S OVERRIDE | * | OVERRIDE | OVERRIDE | 0.090 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_72D OVERRIDE | * | OVERRIDE | OVERRIDE | 0.090 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| MEM_85D OVERRIDE | * | OVERRIDE | OVERRIDE | 0.090 MM OVERRIDE | 100 MIL OVERRIDE | OVERRIDE | OVERRIDE |
| PCIE_85D OVERRIDE | * | OVERRIDE | OVERRIDE | 0.090 MM OVERRIDE | 10 MM OVERRIDE | OVERRIDE | OVERRIDE |
| USB_85D | TOP | | | 0.100 MM | 500 MIL | | |
| CPU_27P4S | BOTTOM | | | 0.230 MM | 100 MIL | | |
| USB3_85D | TOP | | | 0.100 MM | 500 MIL | | |
| USB3_85D | ISL10 | | | 0.075 MM | | | 0.090 MM |
| DP_85D | ISL9 | | | 0.075 MM | | | 0.090 MM |
| PCIE_85D | ISL10 | | | 0.075 MM | | | 0.090 MM |

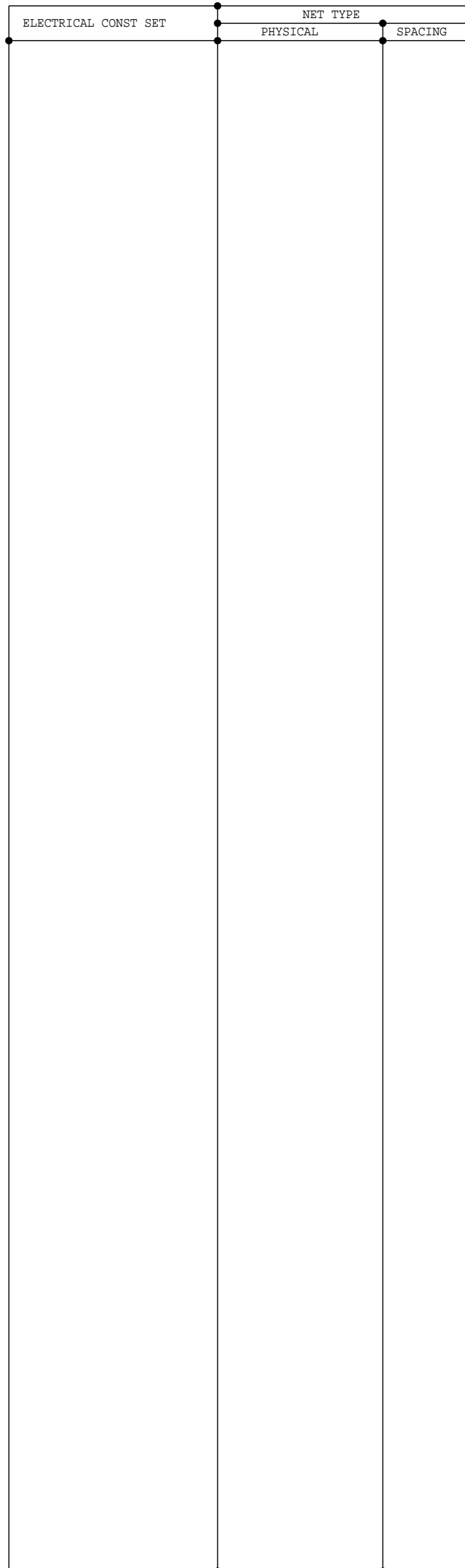
DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

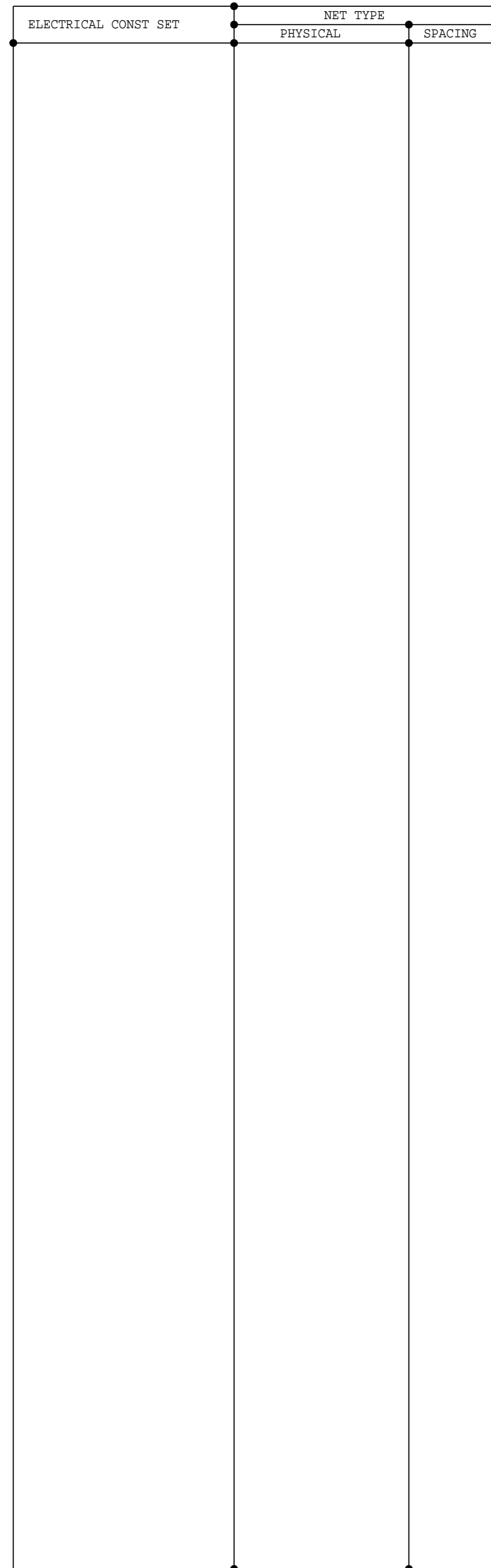
| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| DP_85D | BGA | P65_BGA |
| PCIE_85D | BGA | P65_BGA |
| CLK_PCIE_85D | BGA | P65_BGA |
| HDMI_85D | BGA | P65_BGA |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| SENSE_45S | * | SENSE_45S |
| THERM_45S | * | THERM_45S |
| DIG_AUDIO | * | DIG_AUDIO |
| ANL_AUDIO | * | ANL_AUDIO |

J79 Specific Net Properties



J79 Specific Net Properties



A

| | | | |
|---|----------------|----------------------|-------------|
| SYNC_MASTER=YHARTANTO_J44 | | SYNC_DATE=01/04/2013 | |
| PAGE TITLE | | | |
| Sensors & Audio Constraints | | | |
| | DRAWING NUMBER | 051-00777 | SIZE D |
| | REVISION | 9.0.0 | |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 139 OF 145 |
| | | SHEET | 117 OF 119 |

A

Change List:

<RDAR://COMPONENT/XXXXXX> LOHWILL SCHEMATIC | PROTO 1A



Kismet:

AFP://KISMET.APPLE.COM/KISMET-PROJECTS/LOHWILL

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

- <rdar://component/XXXXXX> MobileMac HW | Task
<rdar://component/XXXXXX> MobileMac HW | Schematic
<rdar://component/XXXXXX> MobileMac HW | New Bugs
<rdar://component/XXXXXX> MobileMac HW | Layout
<rdar://component/XXXXXX> MobileMac HW | Investigation
<rdar://component/XXXXXX> MobileMac HW | Architecture

Other Info:

- Page Allocations - <rdar://problem/19817053> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818112> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818356> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818458> 2015 Schematic Page Allocations

Table with metadata including Apple Inc. logo, drawing number 051-00777, revision 9.0.0, branch dvt-fab09-0, page 140 of 145, and sheet 118 of 119.

Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|---------------------------|
| 107800033 | 107800034 | | ALL | |
| 13880738 | 13881101 | | ALL | Samsung alt to Murata |
| 13880846 | 13880811 | | ALL | Samsung alt to Murata |
| 152800359 | 152800253 | | ALL | Chilisin alt to Cyttec |
| 37180704 | 371800077 | | ALL | NXP alt to Diodes |
| 37681053 | 37680604 | | ALL | Diodes alt to Fairchild |
| 37681106 | 37680678 | | ALL | Fairchild alt to Vishay |
| 740800027 | 74080159 | | ALL | Bourns alt to Little Fuse |
| 10780249 | 10780251 | | ALL | |
| 107800015 | 107800011 | | ALL | |
| 107800071 | 107800053 | | ALL | |
| 12880364 | 12880264 | | ALL | Kemet w/ Panasonic |
| 12880325 | 12880397 | | ALL | |
| 128800009 | 128800007 | | ALL | |
| 128800029 | 128800007 | | ALL | |
| 128800070 | 128800007 | | ALL | |
| 128800010 | 128800011 | | ALL | |
| 128800031 | 128800011 | | ALL | |
| 128800026 | 128800011 | | ALL | |
| 132800064 | 13280409 | | ALL | |
| 13880614 | 13880578 | | ALL | |
| 13880703 | 13880648 | | ALL | |
| 138800032 | 13880831 | | ALL | |
| 138800049 | 13880831 | | ALL | |
| 13880863 | 13880853 | | ALL | |
| 13880775 | 13880860 | | ALL | |
| 138800084 | 138800060 | | ALL | |
| 152800369 | 152800268 | | ALL | Cyttec w/ NEC |
| 155800188 | 15580275 | | ALL | Murata w/ Taiyo |
| 15580694 | 15580387 | | ALL | |
| 15580660 | 15580513 | | ALL | |
| 155800018 | 15580664 | | ALL | Murata w/ Taiyo |
| 155800007 | 15580667 | | ALL | |

BLC

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|---------------------|
| 197800046 | 197800036 | | ALL | Epson w/ TXC |
| 197800047 | 197800036 | | ALL | Kyocera w/ TXC |
| 197800048 | 197800036 | | ALL | Murata w/ TXC |
| 197800053 | 197800050 | | ALL | Kyocera w/ TXC |
| 197800054 | 197800050 | | ALL | NDK w/ TXC |
| 197800055 | 197800050 | | ALL | Murata w/ TXC |
| 31180596 | 31180593 | | ALL | NXP w/ Diodes |
| 10780276 | 107800020 | | ALL | Cyttec w/ TFT |
| 107800021 | 10780284 | | ALL | TFT w/ Yageo |
| 152800343 | 15281682 | | ALL | NXP w/ Diodes |
| 107800087 | 107800029 | | ALL | TFT w/ Yageo |
| 128800058 | 128800018 | | ALL | NEC w/ Rohm |
| 13880706 | 13880739 | | ALL | NEC w/ Vishay |
| 13880945 | 13880739 | | ALL | NEC w/ Rohm |
| 152800358 | 152800208 | | ALL | Murata w/ Chillisin |
| 152800400 | 152800361 | | ALL | Murata w/ Cyttec |
| 15281872 | 152800361 | | ALL | Murata w/ Cyttec |
| 155800034 | 15580706 | | ALL | Taiyo w/ Murata |

| | | | | |
|-----------|----------|--|-----|---------------|
| 353800711 | 35382073 | | ALL | On Semi w/ TI |
|-----------|----------|--|-----|---------------|

| | | | | |
|-----------|-----------|--|-----|-----------------------|
| 740800019 | 740800007 | | ALL | Bourns w/ Polytronics |
| 155800189 | 15580342 | | ALL | Murata w/ Taiyo |
| 13880714 | 13880713 | | ALL | Murata w/ Samsung |
| 13880715 | 13880732 | | ALL | Murata w/ Samsung |
| 107800086 | 107800056 | | ALL | TFT w/ Cyttec |
| 13880875 | 13880678 | | ALL | Taiyo w/ Mur&SS |
| 13880786 | 13880705 | | ALL | Murata w/ Samsung |
| 15282052 | 15281954 | | ALL | Taiyo w/ Cyttec |
| 15282015 | 15281958 | | ALL | Taiyo w/ Cyttec |
| 13880789 | 13880941 | | ALL | Murata w/ SS |
| 107800101 | 107800005 | | ALL | Cyttec w/ Yageo |
| 107800102 | 107800017 | | ALL | Cyttec w/ Yageo |
| 107800100 | 107800057 | | ALL | Cyttec w/ TFT |
| 107800103 | 107800058 | | ALL | Cyttec w/ Yageo |
| 107800104 | 107800061 | | ALL | Cyttec w/ Yageo |
| 107800105 | 107800062 | | ALL | Cyttec w/ Yageo |
| 152800403 | 152800322 | | ALL | Murata w/ Chillisin |


| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|-----------------|
| 138800104 | 13880978 | | ALL | Murata w/ Taiyo |
| 311800072 | 31180657 | | ALL | NXP w/ On Semi |
| 311800090 | 311800028 | | ALL | On Semi w/ TI |
| 353800854 | 35384342 | | ALL | TI w/ ST |
| 377800077 | 37780183 | | ALL | Infineon w/ ST |

| | | | | |
|-----------|-----------|--|-----|--------------------|
| 13880700 | 13880641 | | ALL | Murata w/ SS&Taiyo |
| 152800363 | 152800048 | | ALL | Cyttec w/ Vishay |
| 15580659 | 15580382 | | ALL | Murata w/ TDK |
| 376800146 | 37681061 | | ALL | NXP w/ Diodes |

| | | | | |
|-----------|-----------|--|-----|--|
| 128800062 | 128800067 | | ALL | |
| 128800069 | 128800067 | | ALL | |
| 132800012 | 13280401 | | ALL | |
| 13880660 | 13880684 | | ALL | |
| 13881103 | 13880719 | | ALL | |
| 138800097 | 13880750 | | ALL | |
| 138800111 | 138800036 | | ALL | |
| 155800203 | 15580894 | | ALL | |
| 197800082 | 197800081 | | ALL | |
| 311800060 | 31180273 | | ALL | |
| 311800118 | 31180489 | | ALL | |
| 31180271 | 311800008 | | ALL | |
| 311800104 | 311800091 | | ALL | |
| 31180437 | 311800112 | | ALL | |
| 335800213 | 33580888 | | ALL | |
| 343800136 | 343800135 | | ALL | |
| 343800137 | 343800135 | | ALL | |
| 343800138 | 343800135 | | ALL | |
| 353800880 | 35383452 | | ALL | |
| 353800878 | 353800599 | | ALL | |
| 353800879 | 353800754 | | ALL | |
| 353800750 | 353800877 | | ALL | |
| 371800089 | 371800085 | | ALL | |
| 37780178 | 377800031 | | ALL | |

| | | | | |
|-----------|-----------|--|-----|-----------------|
| 15580914 | 15580897 | | ALL | |
| 155800190 | 15580897 | | ALL | |
| 311800004 | 31180370 | | ALL | |
| 311800013 | 31180508 | | ALL | NXP w/ Diodes |
| 353800107 | 35383239 | | ALL | |
| 353800525 | 35384471 | | ALL | |
| 37280186 | 37280185 | | ALL | |
| 376800014 | 37680761 | | ALL | |
| 376800086 | 37680761 | | ALL | |
| 37681080 | 37680820 | | ALL | |
| 376800074 | 37680855 | | ALL | |
| 37681089 | 37681128 | | ALL | |
| 74080144 | 74080118 | | ALL | |
| 740800028 | 74080118 | | ALL | |
| 740800003 | 74080135 | | ALL | |
| 998-04070 | 998-04071 | | ALL | Hynix alt to SS |

- T208

| | | | |
|---|----------------|----------------------|-------------|
| PAGE TITLE | | Alternates BOM Table | |
|  Apple Inc. | DRAWING NUMBER | 051-00777 | SIZE |
| | REVISION | 9.0.0 | D |
| NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED | | BRANCH | dvt-fab09-0 |
| | | PAGE | 145 OF 145 |
| | | SHEET | 119 OF 119 |